NVM Express™

Base Specification

NVM Express

Revision 1.4c

March 9, 2021

Please send comments to info@nvmexpress.org

NVM Express™ base specification revision 1.4c is available for download at http://nvmexpress.org. The NVM Express base specification revision 1.4c incorporates NVM Express base specification revision 1.3, ratified on April 26, 2017 with updated figure references, along with ECN 001, ECN 002, ECN 003, ECN 004a, ECN 005, ECN 006, TP 4000a, TP 4002, TP 4003c, TP 4004b, TP 4005c, TP 4006, TP 4007a, TP 4008, TP 4014, TP 4016, TP 4018b, TP 4022, TP 4024, TP 4025, TP 4027, TP 4028a, TP 4030, TP 4031a, TP 4032, TP 4033, TP 4035, TP 4039a, TP 4042a, TP 4045, TP 4050, TP 4051, TP 4054, and TP 8002 (refer to https://nvmexpress.org/changes-in-nvme-revision-1-4 for details). It also incorporates the NVM Express base specification revision 1.4b, ratified on September 21, 2020, ECN 001, ECN 002, ECN 003, ECN 004, ECN 006, ECN 007, and ECN 008. Applied the NVM Express trademark and logo usage guidelines.

SPECIFICATION DISCLAIMER

LEGAL NOTICE:

NVM Express Workgroup
c/o VTM, Inc.
3855 SW 153rd Drive
Beaverton, OR 97003 USA
info@nvmexpress.org

Table of Contents

1 Introduction

1.1 Overview

The NVM Express™ (NVMe™) interface allows host software to communicate with a non-volatile memory subsystem. This interface is optimized for Enterprise and Client solid state drives, typically attached as a register level interface to the PCI Express interface.

Note: During development, this specification was referred to as Enterprise NVMHCI. However, the name was modified to NVM Express base specification prior to completion. This interface is targeted for use in both Client and Enterprise systems.

For an overview of changes from revision 1.3 to revision 1.4, refer to http://nvmexpress.org/changes for a document that describes the new features, including mandatory requirements for a controller to comply with revision 1.4.

1.1.1 NVMe™ over PCIe® and NVMe™ over Fabrics

The NVM Express base specification revision 1.4 and prior revisions defined a register level interface for host software to communicate with a non-volatile memory subsystem over PCI Express (NVMe™ over PCIe™). The NVMe™ over Fabrics specification defines a protocol interface and related extensions to the NVMe interface that enable operation over other interconnects (e.g., Ethernet, InfiniBand™, Fibre Channel). The NVMe over Fabrics specification has an NVMe Transport binding for each NVMe Transport (either within that specification or by reference).

In this specification, a requirement/feature may be documented as specific to NVMe over Fabrics implementations or to a particular NVMe Transport binding. In addition, support requirements for features and functionality may differ between NVMe over PCIe and NVMe over Fabrics implementations.

1.2 Scope

The specification defines a register interface for communication with a controller in an NVM subsystem. It also defines standard command sets that may be supported by a controller. There are three types of controllers with different capabilities:

a) I/O controllers;
b) discovery controllers; and
c) administrative controllers (refer to section 7.1).

In this document the generic term controller is often used instead of enumerating specific controller types when applicable controller types may be determined from the context.

1.3 Outside of Scope

The register interface and command set are specified apart from any usage model for the NVM, but rather only specifies the communication interface to the NVM subsystem. Thus, this specification does not specify whether the non-volatile memory system is used as a solid state drive, a main memory, a cache memory, a backup memory, a redundant memory, etc. Specific usage models are outside the scope, optional, and not licensed.

This interface is specified above any non-volatile memory management, like wear leveling. Erases and other management tasks for NVM technologies like NAND are abstracted.

This specification does not contain any information on caching algorithms or techniques.

The implementation or use of other published specifications referred to in this specification, even if required for compliance with the specification, are outside the scope of this specification (e.g., PCI, PCI Express, and PCI-X).

1.4 Theory of Operation

The NVM Express scalable interface is designed to address the needs of Enterprise and Client systems that utilize PCI Express based solid state drives or fabric connected devices. The interface provides optimized command submission and completion paths. It includes support for parallel operation by supporting up to 65,535 I/O Queues with up to 64 Ki - 1 outstanding commands per I/O Queue. Additionally, support has been added for many Enterprise capabilities like end-to-end data protection (compatible with SCSI Protection Information, commonly known as T10 DIF, and SNIA DIX standards), enhanced error reporting, and virtualization.

The interface has the following key attributes:

- Does not require uncacheable / MMIO register reads in the command submission or completion path;
- A maximum of one MMIO register write is necessary in the command submission path;
- Support for up to 65,535 I/O Queues, with each I/O Queue supporting up to 65,535 outstanding commands;
- Priority associated with each I/O Queue with well-defined arbitration mechanism;
- All information to complete a 4 KiB read request is included in the 64B command itself, ensuring efficient small I/O operation;
- Efficient and streamlined command set;
- Support for MSI/MSI-X and interrupt aggregation;
- Support for multiple namespaces;
- Efficient support for I/O virtualization architectures like SR-IOV;
- Robust error reporting and management capabilities; and
- Support for multi-path I/O and namespace sharing.

This specification defines a streamlined set of registers whose functionality includes:

- Indication of controller capabilities;
- Status for controller failures (command status is processed via CQ directly);
- Admin Queue configuration (I/O Queue configuration processed via Admin commands); and
- Doorbell registers for scalable number of Submission and Completion Queues.

An NVM Express controller is associated with a single PCI Function. The capabilities and settings that apply to the entire controller are indicated in the Controller Capabilities (CAP) register and the Identify Controller data structure.

A namespace is a quantity of non-volatile memory that may be formatted into logical blocks. An NVM Express controller may support multiple namespaces that are referenced using a namespace ID. Namespaces may be created and deleted using the Namespace Management and Namespace Attachment commands. The Identify Namespace data structure indicates capabilities and settings that are specific to a particular namespace. The capabilities and settings that are common to all namespaces are reported by the Identify Namespace data structure for namespace ID FFFFFFFFh.

The NVM Express interface is based on a paired Submission and Completion Queue mechanism. Commands are placed by host software into a Submission Queue. Completions are placed into the associated Completion Queue by the controller. Multiple Submission Queues may utilize the same Completion Queue. Submission and Completion Queues are allocated in memory.

An Admin Submission and associated Completion Queue exist for the purpose of controller management and control (e.g., creation and deletion of I/O Submission and Completion Queues, aborting commands, etc.). Only commands that are part of the Admin Command Set may be submitted to the Admin Submission Queue.

An I/O Command Set is used with an I/O queue pair. This specification defines one I/O Command Set, named the NVM Command Set. The host selects one I/O Command Set that is used for all I/O queue pairs.

Host software creates queues, up to the maximum supported by the controller. Typically the number of command queues created is based on the system configuration and anticipated workload. For example, on a four core processor based system, there may be a queue pair per core to avoid locking and ensure data structures are created in the appropriate processor core's cache. Figure 1 provides a graphical representation of the queue pair mechanism, showing a 1:1 mapping between Submission Queues and Completion Queues. Figure 2 shows an example where multiple I/O Submission Queues utilize the same I/O Completion Queue on Core B. Figure 1 and Figure 2 show that there is always a 1:1 mapping between the Admin Submission Queue and Admin Completion Queue.

Figure 1: Queue Pair Example, 1:1 Mapping

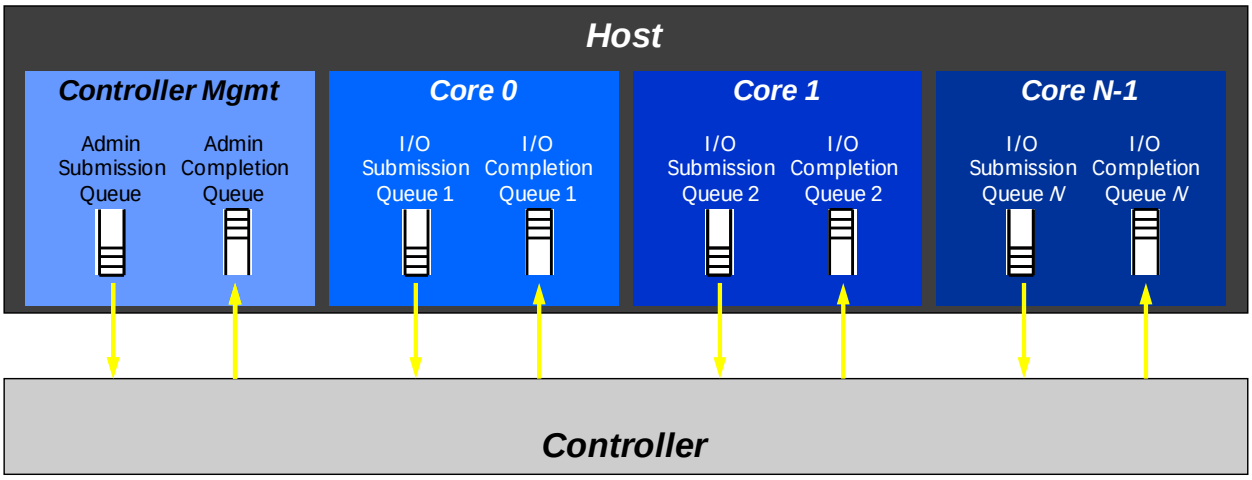
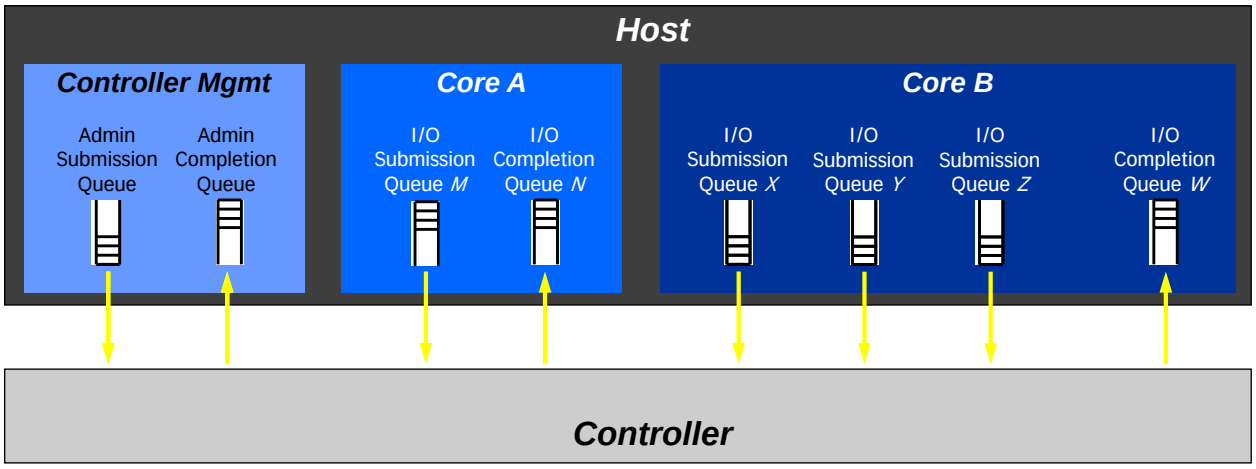


Figure 2: Queue Pair Example, *n*:1 Mapping



A Submission Queue (SQ) is a circular buffer with a fixed slot size that the host software uses to submit commands for execution by the controller. The host software updates the appropriate SQ Tail doorbell register when there are one to *n* new commands to execute. The previous SQ Tail value is overwritten in the controller when there is a new doorbell register write. The controller fetches SQ entries in order from the Submission Queue and may execute those commands in any order.

Each Submission Queue entry is a command. Commands are 64 bytes in size. The physical memory locations in memory to use for data transfers are specified using Physical Region Page (PRP) entries or Scatter Gather Lists. Each command may include two PRP entries or one Scatter Gather List (SGL)

segment. If more than two PRP entries are necessary to describe the data buffer, then a pointer to a PRP List that describes a list of PRP entries is provided. If more than one SGL segment is necessary to describe the data buffer, then the SGL segment provides a pointer to the next SGL segment.

A Completion Queue (CQ) is a circular buffer with a fixed slot size used to post status for completed commands. A completed command is uniquely identified by a combination of the associated SQ identifier and command identifier that is assigned by host software. Multiple Submission Queues may be associated with a single Completion Queue. This feature may be used where a single worker thread processes all command completions via one Completion Queue even when those commands originated from multiple Submission Queues. The CQ Head pointer is updated by host software after processing completion queue entries indicating the last free CQ slot. A Phase Tag (P) bit is defined in the completion queue entry to indicate whether an entry has been newly posted without consulting a register. This enables host software to determine whether the new entry was posted as part of the previous or current round of completion notifications. Specifically, each round through the Completion Queue entries, the controller inverts the Phase Tag bit.

1.4.1 Multi-Path I/O and Namespace Sharing

This section provides an overview of multi-path I/O and namespace sharing. Multi-path I/O refers to two or more completely independent paths between a single host and a namespace while namespace sharing refers to the ability for two or more hosts to access a common shared namespace using different NVM Express controllers. Both multi-path I/O and namespace sharing require that the NVM subsystem contain two or more controllers. NVM subsystems that support Multi-Path I/O and Namespace Sharing may also support asymmetric controller behavior (refer to section 1.4.2). Concurrent access to a shared namespace by two or more hosts requires some form of coordination between hosts. The procedure used to coordinate these hosts is outside the scope of this specification.

Figure 3 shows an NVM subsystem that contains a single NVM Express controller and a single PCI Express port. Since this is a single Function PCI Express device, the NVM Express controller shall be associated with PCI Function 0. A controller may support multiple namespaces. The controller in Figure 3 supports two namespaces labeled NS A and NS B. Associated with each controller namespace is a namespace ID, labeled as NSID 1 and NSID 2, that is used by the controller to reference a specific namespace. The namespace ID is distinct from the namespace itself and is the handle a host and controller use to specify a particular namespace in a command. The selection of a controller's namespace IDs is outside the scope of this specification. In this example namespace ID 1 is associated with namespace A and namespace ID 2 is associated with namespace B. Both namespaces are private to the controller and this configuration supports neither multi-path I/O nor namespace sharing.

Figure 3: NVM Express Controller with Two Namespaces

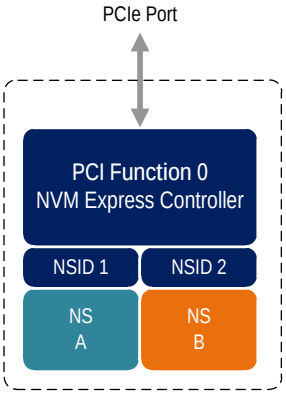
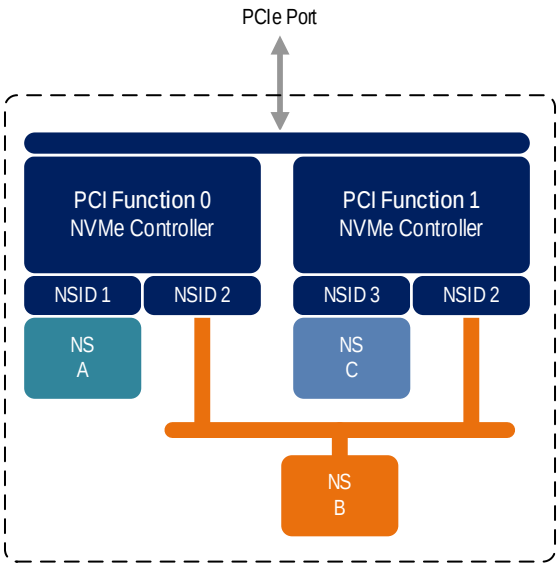


Figure 4 shows a multi-Function NVM subsystem with a single PCI Express port containing two controllers, one controller is associated with PCI Function 0 and the other controller is associated with PCI Function 1. Each controller supports a single private namespace and access to shared namespace B. The namespace ID shall be the same in all controllers that have access to a particular shared namespace. In this example both controllers use namespace ID 2 to access shared namespace B.

Figure 4: NVM Subsystem with Two Controllers and One Port

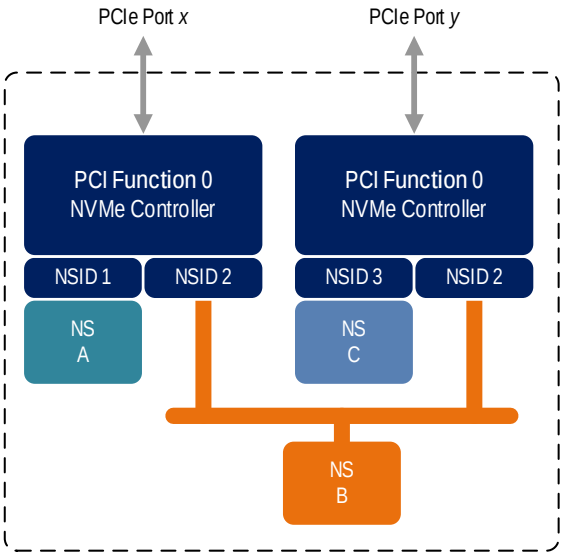


There is a unique Identify Controller data structure for each controller and a unique Identify Namespace data structure for each namespace. Controllers with access to a shared namespace return the Identify Namespace data structure associated with that shared namespace (i.e., the same data structure contents are returned by all controllers with access to the same shared namespace). There is a globally unique identifier associated with the namespace itself and may be used to determine when there are multiple paths to the same shared namespace. Refer to section 7.10.

Controllers associated with a shared namespace may operate on the namespace concurrently. Operations performed by individual controllers are atomic to the shared namespace at the write atomicity level of the controller to which the command was submitted (refer to section 6.4). The write atomicity level is not required to be the same across controllers that share a namespace. If there are any ordering requirements between commands issued to different controllers that access a shared namespace, then host software or an associated application, is required to enforce these ordering requirements.

Figure 5 illustrates an NVM subsystem with two PCI Express ports, each with an associated controller. Both controllers map to PCI Function 0 of the corresponding port. Each PCI Express port in this example is completely independent and has its own PCI Express Fundamental Reset and reference clock input. A reset of a port only affects the controller associated with that port and has no impact on the other controller, shared namespace, or operations performed by the other controller on the shared namespace. The functional behavior of this example is otherwise the same as that illustrated in Figure 4.

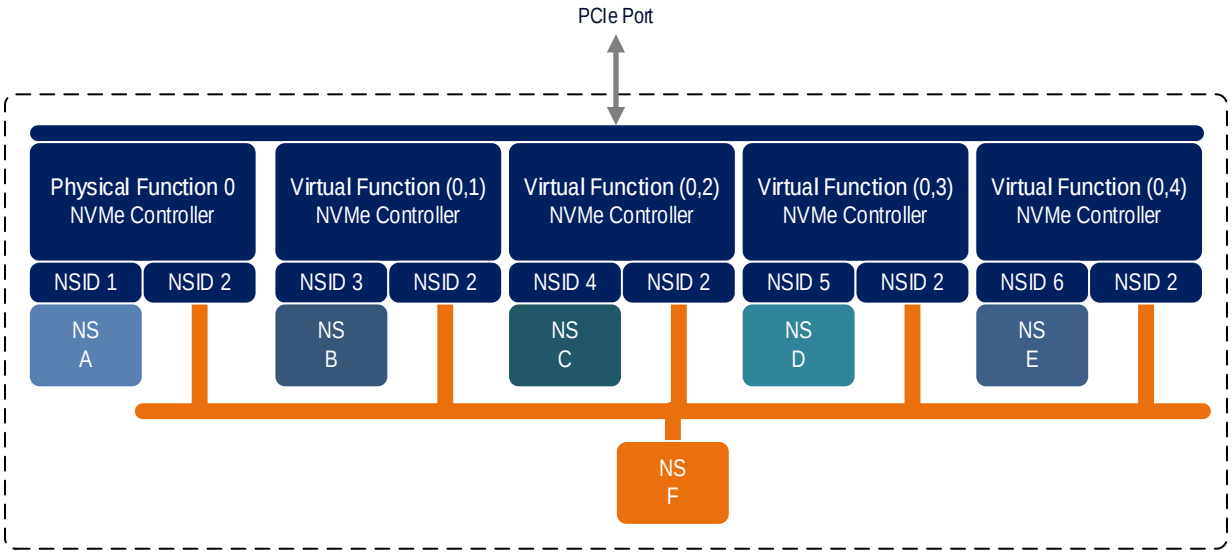
Figure 5: NVM Subsystem with Two Controllers and Two Ports



The two ports shown in Figure 5 may be associated with the same Root Complex or with different Root Complexes and may be used to implement both multi-path I/O and I/O sharing architectures. System-level architectural aspects and use of multiple ports in a PCI Express fabric are beyond the scope of this specification.

Figure 6 illustrates an NVM subsystem that supports Single Root I/O Virtualization (SR-IOV) and has one Physical Function and four Virtual Functions. An NVM Express controller is associated with each Function with each controller having a private namespace and access to a namespace shared by all controllers, labeled NS F. The behavior of the controllers in this example parallels that of the other examples in this section. Refer to section 8.5.4 for more information on SR-IOV.

Figure 6: PCI Express Device Supporting Single Root I/O Virtualization (SR-IOV)



Examples provided in this section are meant to illustrate concepts and are not intended to enumerate all possible configurations. For example, an NVM subsystem may contain multiple PCI Express ports with each port supporting SR-IOV.

1.4.2 Asymmetric Controller Behavior

Asymmetric controller behavior occurs in NVM subsystems where namespace access characteristics (e.g., performance) may vary based on:

- the internal configuration of the NVM subsystem; or
- which controller is used to access a namespace (e.g., Fabrics).

NVM subsystems that provide asymmetric controller behavior may support Asymmetric Namespace Access Reporting as described in section 8.20.

1.5 Conventions

Hardware shall return '0' for all bits and registers that are marked as reserved, and host software shall write all reserved bits and registers with the value of 0h

Inside the register sections (i.e., section 2 and section 3), the following terms and abbreviations are used:

RO	Read Only
RW	Read Write
R/W	Read Write. The value read may not be the last value written.
RWC	Read/Write '1' to clear
RWS	Read/Write '1' to set
Impl Spec	Implementation Specific – the controller has the freedom to choose its implementation.
HwInit	The default state is dependent on NVM Express controller and system configuration.
Reset	For section 2, this column indicates the value of the field after a reset. as defined by the appropriate PCI or PCI Express specifications. For section 3, this column indicates the value of the field after a Controller Level Reset as defined in section 7.3.2.

For some register fields, it is implementation specific as to whether the field is RW, RWC, or RO; this is typically shown as RW/RO or RWC/RO to indicate that if the functionality is not supported that the field is read only.

When a register field is referred to in the document, the convention used is "Register Symbol.Field Symbol". For example, the PCI command register Parity Error Response Enable bit is referred to by the name CMD.PEE. If the register field is an array of bits, the field is referred to as "Register Symbol.Field Symbol (array offset to element)".

A 0's based value is a numbering scheme in which the number 0h represents a value of 1h, 1h represents 2h, 2h represents 3h, etc. In this numbering scheme, there is no method to represent the value of 0h. Values in this specification are 1-based (i.e., the number 1h represents a value of 1h, 2h represents 2h, etc.) unless otherwise specified.

Size values are shown in binary units or decimal units. The symbols used to represent these values are as shown in Figure 7.

Figure 7: Decimal and Binary Units

Decimal		Binary	
Symbol	**Power (base-10)**	**Symbol**	**Power (base-2)**
kilo / k	10^3	kibi / Ki	2^{10}
mega / M	10^6	mebi / Mi	2^{20}
giga / G	10^9	gibi / Gi	2^{30}
tera / T	10^{12}	tebi / Ti	2^{40}
peta / P	10^{15}	pebi / Pi	2^{50}
exa / E	10^{18}	exbi / Ei	2^{60}
zetta / Z	10^{21}	zebi / Zi	2^{70}
yotta / Y	10^{24}	yobi / Yi	2^{80}

The ^ operator is used to denote the power to which that number, symbol, or expression is to be raised.

Some parameters are defined as an ASCII string. ASCII strings shall contain only code values 20h through 7Eh. For the string “Copyright”, the character “C” is the first byte, the character “o” is the second byte, etc. The string is left justified and shall be padded with spaces (ASCII character 20h) to the right if necessary. A hexadecimal ASCII string is an ASCII string that uses a subset of the code values: “0” to “9”, “A” to “F” uppercase, and “a” to “f” lowercase.

Hexadecimal (i.e., base 16) numbers are written with a lower case “h” suffix (e.g., 0FFFh, 80h). Hexadecimal numbers larger than eight digits are represented with an underscore character dividing each group of eight digits (e.g., 1E_DEADBEEFh).

Binary (i.e., base 2) numbers are written with a lower case “b” suffix (e.g., 1001b, 10b). Binary numbers larger than four digits are written with an underscore character dividing each group of four digits (e.g., 1000_0101_0010b).

All other numbers are decimal (i.e., base 10). A decimal number is represented in this specification by any sequence of digits consisting of only the Western-Arabic numerals 0 to 9 not immediately followed by a lower-case b or a lower-case h (e.g., 175). This specification uses the following conventions for representing decimal numbers:

a) the decimal separator (i.e., separating the integer and fractional portions of the number) is a period;
b) the thousands separator (i.e., separating groups of three decimal digits in a portion of the number) is a comma;
c) the thousands separator is used in only the integer portion of a number and not the fractional portion of a number; and
d) the decimal representation for a year does not include a comma (e.g., 2019 instead of 2,019).

1.6 Definitions

1.6.1 Admin Queue

The Admin Queue is the Submission Queue and Completion Queue with identifier 0. The Admin Submission Queue and corresponding Admin Completion Queue are used to submit administrative commands and receive completions for those administrative commands, respectively.

The Admin Submission Queue is uniquely associated with the Admin Completion Queue.

1.6.2 administrative controller

A controller that exposes capabilities that allow a host to manage an NVM subsystem. An administrative controller does not implement I/O Queues, provide access to data or metadata associated with user data on a non-volatile memory storage medium, or support namespaces attached to the administrative controller (i.e., there are never any active NSIDs).

1.6.3 arbitration burst

The maximum number of commands that may be launched at one time from a Submission Queue that is using round robin or weighted round robin with urgent priority class arbitration.

1.6.4 arbitration mechanism

The method used to determine which Submission Queue is selected next to launch commands for execution by the controller. Three arbitration mechanisms are defined including round robin, weighted round robin with urgent priority class, and vendor specific. Refer to section 4.13.

1.6.5 cache

A data storage area used by the NVM subsystem, that is not accessible to a host, and that may contain a subset of user data stored in the non-volatile media or may contain user data that is not committed to non-volatile media.

1.6.6 candidate command

A candidate command is a submitted command which has been transferred into the controller and the controller deems ready for processing.

1.6.7 command completion

A command is completed when the controller has completed processing the command, has updated status information in the completion queue entry, and has posted the completion queue entry to the associated Completion Queue.

1.6.8 command submission

For NVMe over PCIe implementations, a command is submitted when a Submission Queue Tail Doorbell write has completed that moves the Submission Queue Tail Pointer value past the Submission Queue slot in which the command was placed.

For NVMe over Fabrics implementations, refer to section 1.4.14 in the NVMe over Fabrics specification.

1.6.9 controller

A controller is the interface between a host and an NVM subsystem. There are three types of controllers:

a) I/O controllers;
b) discovery controllers; and
c) administrative controllers.

A controller executes commands submitted by a host on a Submission Queue and posts a completion on a Completion Queue. All controllers implement one Admin Submission Queue and one Admin Completion Queue. Depending on the controller type, a controller may also implement one or more I/O Submission

Queues and I/O Completion Queues. When PCI Express is used as the transport, then a controller is a PCI Express function.

1.6.10 directive

A method of host and NVM subsystem or controller information exchange. Information may be transmitted using the Directive Send and Directive Receive commands. A subset of I/O commands may include a Directive Type field and a Directive Specific field to communicate more information that is specific to the associated I/O command. Refer to section 9.

1.6.11 discovery controller

A controller that exposes capabilities that allow a host to retrieve a Discovery Log Page. A discovery controller does not implement I/O Queues or provide access to a non-volatile memory storage medium. Refer to the NVMe over Fabrics specification for more information.

1.6.12 emulated controller

An NVM Express controller that is defined in software. An emulated controller may or may not have an underlying physical NVMe controller (e.g., physical PCIe function).

1.6.13 Endurance Group

A portion of NVM in the NVM subsystem whose endurance is managed as a group. Refer to section 8.17.

1.6.14 extended LBA

An extended LBA is a larger LBA that is created when metadata associated with the LBA is transferred contiguously with the LBA data. Refer to Figure 453.

1.6.15 firmware slot

A firmware slot is a location in the NVM subsystem used to store a firmware image. The NVM subsystem stores from one to seven firmware images.

1.6.16 host

An entity that interfaces to an NVM subsystem through one or more controllers and submits commands to Submission Queues and retrieves command completions from Completion Queues.

1.6.17 host-accessible memory

Memory that the host is able to access (e.g., host memory, Controller Memory Buffer (CMB), Persistent Memory Region (PMR))

1.6.18 host memory

Memory that may be read and written by both a host and a controller and that is not exposed by a controller (i.e., Controller Memory Buffer or Persistent Memory Region). Host memory may be implemented inside or outside a host (e.g., a memory region exposed by a device that is neither the host nor controller).

1.6.19 I/O command

An I/O command is a command submitted to an I/O Submission Queue.

1.6.20 I/O Completion Queue

An I/O Completion Queue is a Completion Queue that is used to indicate command completions and is associated with one or more I/O Submission Queues. I/O Completion Queue identifiers are from 1 to 65535.

1.6.21 I/O controller

A controller that implements I/O queues and is intended to be used to access a non-volatile memory storage medium.

1.6.22 I/O Submission Queue

An I/O Submission Queue is a Submission Queue that is used to submit I/O commands for execution by the controller (e.g., Read, Write for the NVM command set). I/O Submission Queue identifiers are from 1 to 65,535.

1.6.23 LBA range

A collection of contiguous logical blocks specified by a starting LBA and number of logical blocks.

1.6.24 logical block

The smallest addressable data unit for Read and Write commands.

1.6.25 logical block address (LBA)

The address of a logical block, referred to commonly as LBA.

1.6.26 metadata

Metadata is contextual information related to particular data. The host may include metadata to be stored by the NVM subsystem if storage space is provided by the controller. Metadata may include Protection Information (refer to section 8.3).

1.6.27 namespace

A quantity of non-volatile memory that may be formatted into logical blocks. When formatted, a namespace of size n is a collection of logical blocks with logical block addresses from 0 to (n-1).

1.6.28 Namespace ID (NSID)

An identifier used by a controller to provide access to a namespace or the name of the field in the SQE that contains the namespace identifier (refer to Figure 106). Refer to section 6.1 for the definitions of valid NSID, invalid NSID, active NSID, inactive NSID, allocated NSID, and unallocated NSID.

1.6.29 NVM

NVM is an acronym for non-volatile memory.

1.6.30 NVM Set

A portion of NVM from an Endurance Group. Refer to section 4.9.

1.6.31 NVM subsystem

An NVM subsystem includes one or more controllers, zero or more namespaces, and one or more ports. An NVM subsystem may include a non-volatile memory storage medium and an interface between the controller(s) in the NVM subsystem and non-volatile memory storage medium.

1.6.32 primary controller

An NVM Express controller that supports the Virtualization Management command. An NVM subsystem may contain multiple primary controllers. Secondary controller(s) in an NVM subsystem depend on a primary controller for dynamic resource management (refer to section 8.5).

A PCI Express SR-IOV Physical Function that supports the NVM Express interface and the Virtualization Enhancements capability is an example of a primary controller (refer to section 8.5.4).

1.6.33 private namespace

A namespace that is only able to be attached to one controller at a time. A host may determine whether a namespace is a private namespace or may be a shared namespace by the value of the Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC) field in the Identify Namespace data structure.

1.6.34 Runtime D3 (Power Removed)

In Runtime D3 (RTD3) main power is removed from the controller. Auxiliary power may or may not be provided. For PCI Express, RTD3 is the $D3_{cold}$ power state (refer to section 8.4.4).

1.6.35 sanitize operation

Process by which all user data in the NVM subsystem is altered such that recovery of the previous user data from any cache or the non-volatile media is not possible.

1.6.36 secondary controller

An NVM Express controller that depends on a primary controller in an NVM subsystem for management of some controller resources (refer to section 8.5).

A PCI Express SR-IOV Virtual Function that supports the NVM Express interface and receives resources from a primary controller is an example of a secondary controller (refer to section 8.5.4).

1.6.37 shared namespace

A namespace that may be attached to two or more controllers in an NVM subsystem concurrently. A host may determine whether a namespace is a private namespace or may be a shared namespace by the value of the Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC) field in the Identify Namespace data structure.

1.6.38 user data

Data stored in a namespace that is composed of data that the host may store and later retrieve including metadata if supported.

1.7 Keywords

Several keywords are used to differentiate between different levels of requirements.

1.7.1 mandatory

A keyword indicating items to be implemented as defined by this specification.

1.7.2 may

A keyword that indicates flexibility of choice with no implied preference.

1.7.3 optional

A keyword that describes features that are not required by this specification. However, if any optional feature defined by the specification is implemented, the feature shall be implemented in the way defined by the specification.

1.7.4 R

“R” is used as an abbreviation for “reserved” when the figure or table does not provide sufficient space for the full word “reserved”.

1.7.5 reserved

A keyword referring to bits, bytes, words, fields, and opcode values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this or other specifications. A reserved bit, byte, word, field, or register shall be cleared to 0h, or in accordance with a future extension to this specification. The recipient of a command or a register write is not required to check reserved bits, bytes, words, or fields. Receipt of reserved coded values in defined fields in commands shall be reported as an error. Writing a reserved coded value into a controller register field produces undefined results.

1.7.6 shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to the specification.

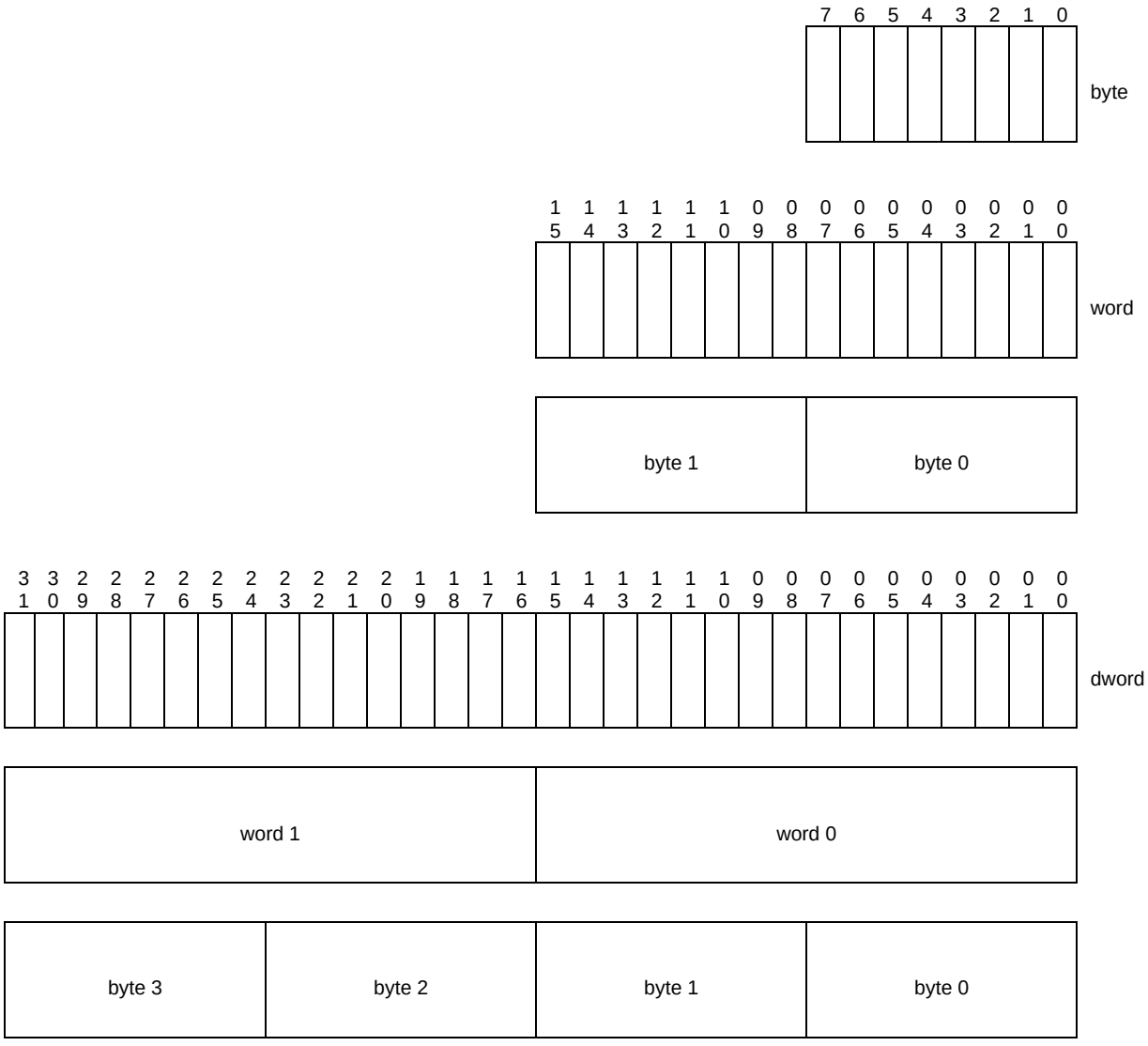
1.7.7 should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

1.8 Byte, Word, and Dword Relationships

Figure 8 illustrates the relationship between bytes, words and dwords. A qword (quadruple word) is a unit of data that is four times the size of a word; it is not illustrated due to space constraints. Unless otherwise specified, this specification specifies data in a little endian format.

Figure 8: Byte, Word, and Dword Relationships



1.9 References

INCITS 514-2014, Information technology – SCSI Block Commands - 3 (SBC-3). Available from http://webstore.ansi.org.

INCITS 529-2018, Information technology – ATA/ATAPI Command Set - 4 (ACS-4). Available from http://webstore.ansi.org.

ISO 8601, Data elements and interchange formats – Information interchange – Representations of dates and times. Available from http://www.iso.org.

JEDEC JESD218B-01: Solid State Drive (SSD) Requirements and Endurance Test Method standard. Available from http://www.jedec.org.

NVM Express over Fabrics Specification, Revision 1.0. Available from http://www.nvmexpress.org.

NVM Express Management Interface Specification, Revision 1.0. Available from http://www.nvmexpress.org.

PCI Local Bus Specification, revision 3.0. Available from http://www.pcisig.com.

PCI Express® Base Specification, Revision 4.0. Available from http://www.pcisig.com.

PCI Bus Power Management Interface Specification Revision 1.2. Available from http://www.pcisig.com.

PCI Single Root I/O Virtualization and Sharing Specification, revision 1.1. Available from http://www.pcisig.com/specifications/iov/single_root/.

PCI Firmware Specification Revision 3.2. Available from http://www.pcisig.com.

PCI Code and ID Assignment Specification Revision 1.11, 24 January, 2019. Available from http://www.pcisig.com.

RFC 4122, P. Leach, M. Mealling, and R. Salz, “A Universally Unique Identifier (UUID) URN Namespace”, July 2005. Available from https://www.ietf.org/rfc.html.

RFC 6234, Eastlake 3rd, D. and T. Hansen, "US Secure Hash Algorithms (SHA and SHA-based HMAC and HKDF)", May 2011. Available from https://www.ietf.org/rfc.html.

UEFI Specification Version 2.7A, September 2017. Available from http://uefi.org.

Advanced Configuration and Power Interface (ACPI) Specification, Version 6.2 Errata A, September 2017. Available from http://www.uefi.org.

TCG Storage Architecture Core Specification, Version 2.01 Revision 1.00. Available from http://www.trustedcomputinggroup.org.

TCG Storage Interface Interactions Specification (SIIS), Version 1.08 Revision 1.00. Available from http://www.trustedcomputinggroup.org.

1.10 References Under Development

INCITS 506-201x, SCSI Block Commands - 4 (SBC-4). Available from http://www.t10.org.

2 System Bus (PCI Express) Registers

This section describes the PCI Express register values when the PCI Express is the system bus used. Other system buses may be used in an implementation. If a system bus is used that is not a derivative of PCI, then this section is not applicable (n/a).

This section details how the PCI Header, PCI Capabilities, and PCI Express Extended Capabilities should be constructed for an NVM Express controller. The fields shown are duplicated from the appropriate PCI or PCI Express specifications. The PCI documents are the normative specifications for these registers and this section details additional requirements for an NVM Express controller.

Figure 9: PCI Express Registers

Start	End	Name	Type
00h	3Fh	PCI Header	
PMCAP	PMCAP+7h	PCI Power Management Capability	PCI Capability
MSICAP	MSICAP+9h	Message Signaled Interrupt Capability	PCI Capability
MSIXCAP	MSIXCAP+Bh	MSI-X Capability	PCI Capability
PXCAP	PXCAP+29h	PCI Express Capability	PCI Capability
AERCAP	AERCAP+47h	Advanced Error Reporting Capability	PCI Express Extended Capability

MSI-X is the recommended interrupt mechanism to use. However, some systems may not support MSI-X, as a result, devices may choose to support both the MSI Capability and the MSI-X Capability.

It is recommended that implementations support the Advanced Error Reporting Capability to enable more robust error handling.

2.1 PCI Header

Figure 10: PCI Header

Start	End	Symbol	Name
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built-In Self Test (Optional)
10h	13h	MLBAR (BAR0)	Memory Register Base Address, lower 32-bits <BAR0>
14h	17h	MUBAR (BAR1)	Memory Register Base Address, upper 32-bits <BAR1>
18h	1Bh	BAR2	Refer to section 2.1.12
1Ch	1Fh	BAR3	Vendor Specific
20h	23h	BAR4	Vendor Specific
24h	27h	BAR5	Vendor Specific
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address (Optional)
34h	34h	CAP	Capabilities Pointer
35h	3Bh	R	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant (Optional)
3Fh	3Fh	MLAT	Maximum Latency (Optional)

2.1.1 Offset 00h: ID - Identifiers

Figure 11: Offset 00h: ID - Identifiers

Bits	Type	Reset	Description
31:16	RO	Impl Spec	**Device ID (DID):** Indicates the device number assigned by the vendor. Specific to each implementation.
15:00	RO	Impl Spec	**Vendor ID (VID):** Indicates the company vendor, assigned by the PCI SIG.

2.1.2 Offset 04h: CMD - Command

Figure 12: Offset 04h: CMD - Command

Bits	Type	Reset	Description
15:11	RO	0h	Reserved
10	RW	0b	**Interrupt Disable (ID):** Disables the controller from generating pin-based INTx# interrupts. This bit does not have any effect on MSI or MSI-X operation.
09	RO	0b	**Fast Back-to-Back Enable (FBE):** Not supported by the NVM Express interface.
08	RW/RO	0b	**SERR# Enable (SEE):** Controls error reporting.
07	RO	0b	Hardwired to 0.
06	RW/RO	0b	**Parity Error Response Enable (PEE):** When set to '1', the controller shall generate PERR# when a data parity error is detected. If parity is not supported, then this bit is read-only '0'.
05	RO	0b	**VGA Palette Snooping Enable (VGA):** Not supported by NVM Express.
04	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not supported by the NVM Express interface.
03	RO	0b	**Special Cycle Enable (SCE):** Not supported by NVM Express.
02	RW	0b	**Bus Master Enable (BME):** Enables the controller to act as a master for data transfers. When set to '1', bus master activity is allowed. When cleared to '0', the controller is not allowed to issue any Memory or I/O Requests.
01	RW	0b	**Memory Space Enable (MSE):** Controls access to the controller's register memory space.
00	RW	0b	**I/O Space Enable (IOSE):** Controls access to the controller's target I/O space.

2.1.3 Offset 06h: STS - Device Status

Figure 13: Offset 06h: STS – Device Status

Bits	Type	Reset	Description
15	RWC	0b	**Detected Parity Error (DPE):** Set to '1' by hardware when the controller detects a parity error on its interface.
14	RWC/RO	0b	**Signaled System Error (SSE):** Refer to the PCI SIG specifications.
13	RWC	0b	**Received Master-Abort (RMA):** Set to '1' by hardware when the controller receives a master abort to a cycle it generated.
12	RWC	0b	**Received Target Abort (RTA):** Set to '1' by hardware when the controller receives a target abort to a cycle it generated.
11	RO	0b	**Signaled Target-Abort (STA):** Not supported by the NVM Express interface.
10:09	RO	Impl Spec	**DEVSEL# Timing (DEVT):** Controls the device select time for the controller's PCI interface. This field is not applicable to PCI Express implementations.
08	RWC	0b	**Master Data Parity Error Detected (DPD):** Set to '1' by hardware when the controller, as a master, either detects a parity error or sees the parity error line asserted, and the Parity Error Response Enable bit (CMD.PEE) is set to '1'.

Figure 13: Offset 06h: STS – Device Status

Bits	Type	Reset	Description
07	RO	Impl Spec	**Fast Back-to-Back Capable (FBC):** Indicates whether the controller accepts fast back-to-back cycles. This bit is not applicable to PCI Express implementations.
06	RO	0b	Reserved
05	RO	Impl Spec	**66 MHz Capable (C66):** Indicates whether the controller may operate at 66 MHz. This bit is not applicable to PCI Express implementations.
04	RO	1b	**Capabilities List (CL):** Indicates the presence of a capabilities list. The controller shall support the PCI Power Management capability as a minimum.
03	RO	0	**Interrupt Status (IS):** Indicates the interrupt status of the device ('1' = asserted).
02:00	RO	000b	Reserved

2.1.4 Offset 08h: RID - Revision ID

Figure 14: Offset 08h: RID - Revision ID

Bits	Type	Reset	Description
07:00	RO	Impl Spec	**Revision ID (RID):** Indicates stepping of the controller hardware.

2.1.5 Offset 09h: CC - Class Code

Fields in the Class Code register are described in the PCI Code and ID Assignment Specification.

Figure 15: Offset 09h: CC - Class Code

Bits	Type	Reset	Description
23:16	RO	01h	**Base Class Code (BCC):** Indicates the base class code as a mass storage controller.
15:08	RO	08h	**Sub Class Code (SCC):** Indicates the sub class code as a Non-Volatile Memory controller.
07:00	RO	02h or 03h	**Programming Interface (PI):** This field specifies the controller uses the NVM Express programming interface. I/O Controllers shall report 02h and Administrative controllers shall report 03h as defined by the PCI Code and ID Assignment Specification.

2.1.6 Offset 0Ch: CLS – Cache Line Size

Figure 16: Offset 0Ch: CLS – Cache Line Size

Bits	Type	Reset	Description
07:00	RW	00h	**Cache Line Size (CLS):** Cache Line Size register is set by the system firmware or operating system to the system cache size.

2.1.7 Offset 0Dh: MLT – Master Latency Timer

Figure 17: Offset 0Dh: MLT – Master Latency Timer

Bits	Type	Reset	Description
07:00	RO	00h	**Master Latency Timer (MLT):** Indicates the number of clocks the controller is allowed to act as a master on PCI. For a PCI Express device, this register does not apply and shall be hardwired to '0'.

2.1.8 Offset 0Eh: HTYPE – Header Type

Figure 18: Offset 0Eh: HTYPE – Header Type

Bits	Type	Reset	Description
07	RO	Impl Spec	**Multi-Function Device (MFD):** Indicates whether the controller is part of a multi-function device.
06:00	RO	00h	**Header Layout (HL):** Indicates that the controller uses a target device layout.

2.1.9 Offset 0Fh: BIST – Built-In Self Test (Optional)

The following register is optional, but if implemented, shall look as follows. When not implemented, it shall be read-only 0h.

Figure 19: Offset 0Fh: BIST – Built-In Self Test (Optional)

Bits	Type	Reset	Description
07	RO	Impl Spec	**BIST Capable (BC):** Indicates whether the controller has a BIST function.
06	RW	0b	**Start BIST (SB):** Host software sets this bit to '1' to invoke BIST. The controller clears this bit to '0' when BIST is complete.
05:04	RO	00b	Reserved
03:00	RO	0h	**Completion Code (CC):** Indicates the completion code status of BIST. A non-zero value indicates a failure.

2.1.10 Offset 10h: MLBAR (BAR0) – Memory Register Base Address, lower 32-bits

This register allocates space for the memory registers defined in section 3.

Figure 20: Offset 10h: MLBAR (BAR0) – Memory Register Base Address, lower 32-bits

Bits	Type	Reset	Description
31:14	RW	0h	**Base Address (BA):** Base address of register memory space. For controllers that support a larger number of doorbell registers or have vendor specific space following the doorbell registers, more bits are allowed to be RO such that more memory space is consumed.
13:04	RO	0h	Reserved
03	RO	0b	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
02:01	RO	Impl Spec	**Type (TP):** Indicates where this range may be mapped. It is recommended to support mapping anywhere in 64-bit address space.
00	RO	0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

2.1.11 Offset 14h: MUBAR (BAR1) – Memory Register Base Address, upper 32-bits

This register specifies the upper 32-bit address of the memory registers defined in section 3.

Figure 21: Offset 14h: MUBAR (BAR1) – Memory Register Base Address, upper 32-bits

Bits	Type	Reset	Description
31:00	RW	0h	**Base Address (BA):** Upper 32-bits (bits 63:32) of the memory register base address.

Note: NVM Express implementations that reside behind PCI compliant bridges, such as PCI Express Endpoints, are restricted to having 32-bit assigned base address registers due to limitations on the maximum address that may be specified in the bridge for non-prefetchable memory. Refer to the PCI Bridge 1.2 specification for more information on this restriction.

2.1.12 Offset 18h: BAR2 – Index/Data Pair Register Base Address or Vendor Specific (Optional)

If this register is configured as I/O space, then this register specifies the Index/Data Pair base address and is configured as shown in Figure 22. These registers are used to access the memory registers defined in section 3 using I/O based accesses.

Figure 22: Offset 18h: BAR2 – Index/Data Pair Register Base Address or Vendor Specific (Optional)

Bits	Type	Reset	Description
31:03	RW	0h	**Base Address (BA):** Base address of Index/Data Pair registers that is 8 bytes in size.
02:01	RO	00b	Reserved
00	RO	1b	**Resource Type Indicator (RTE):** Indicates a request for register I/O space.

If this register is configured as memory space (Resource Type Indicator is cleared to '0'), then the BAR2 register is vendor specific. Vendor specific space may also be allocated at the end of the memory registers defined in section 3.

2.1.13 Offset 1Ch to 1Fh: BAR3 – Vendor Specific

The BAR3 register is vendor specific. Vendor specific space may also be allocated at the end of the memory registers defined in section 3.

2.1.14 Offset 20h to 23h: BAR4 – Vendor Specific

The BAR4 register is vendor specific. Vendor specific space may also be allocated at the end of the memory registers defined in section 3.

2.1.15 Offset 24h to 27h: BAR5 – Vendor Specific

The BAR5 register is vendor specific. Vendor specific space may also be allocated at the end of the memory registers defined in section 3.

2.1.16 Offset 28h: CCPTR – CardBus CIS Pointer

Figure 23: Offset 28h: CCPTR – CardBus CIS Pointer

Bits	Type	Reset	Description
31:00	RO	0h	Not supported by the NVM Express interface.

2.1.17 Offset 2Ch: SS - Subsystem Identifiers

Figure 24: Offset 2Ch: SS - Subsystem Identifiers

Bits	Type	Reset	Description
31:16	RO	HwInit	**Subsystem ID (SSID):** Indicates the sub-system identifier.
15:00	RO	HwInit	**Subsystem Vendor ID (SSVID):** Indicates the sub-system vendor identifier.

2.1.18 Offset 30h: EROM – Expansion ROM (Optional)

If the register is not implemented, it shall be read-only 0h.

Figure 25: Offset 30h: EROM – Expansion ROM (Optional)

Bits	Type	Reset	Description
31:00	RW	Impl Spec	**ROM Base Address (RBA):** Indicates the base address of the controller's expansion ROM. Not supported for integrated implementations.

2.1.19 Offset 34h: CAP – Capabilities Pointer

Figure 26: Offset 34h: CAP – Capabilities Pointer

Bits	Type	Reset	Description
7:0	RO	Impl Spec	**Capability Pointer (CP):** Indicates the first capability pointer offset.

2.1.20 Offset 3Ch: INTR - Interrupt Information

Figure 27: Offset 3Ch: INTR - Interrupt Information

Bits	Type	Reset	Description
15:08	RO	Impl Spec	**Interrupt Pin (IPIN):** This indicates the interrupt pin the controller uses.
07:00	RW	0h	**Interrupt Line (ILINE):** Host software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

2.1.21 Offset 3Eh: MGNT – Minimum Grant

Figure 28: Offset 3Eh: MGNT – Minimum Grant

Bits	Type	Reset	Description
07:00	RO	0h	**Grant (GNT):** Not supported by the NVM Express interface.

2.1.22 Offset 3Fh: MLAT – Maximum Latency

Figure 29: Offset 3Fh: MLAT – Maximum Latency

Bits	Type	Reset	Description
07:00	RO	0h	**Latency (LAT):** Not supported by the NVM Express interface.

2.2 PCI Power Management Capabilities

Refer to section 3.1.5 for requirements when the PCI power management state changes.

Figure 30: PCI Power Management Capabilities

Start	End	Symbol	Name
PMCAP	PMCAP+1h	PID	PCI Power Management Capability ID
PMCAP+2h	PMCAP+3h	PC	PCI Power Management Capabilities
PMCAP+4h	PMCAP+5h	PMCS	PCI Power Management Control and Status

2.2.1 Offset PMCAP: PID - PCI Power Management Capability ID

Figure 31: Offset PMCAP: PID - PCI Power Management Capability ID

Bits	Type	Reset	Description
15:08	RO	Impl Spec	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This may be a capability pointer (such as Message Signaled Interrupts) or may be the last item in the list.
07:00	RO	1h	**Cap ID (CID):** Indicates that this pointer is a PCI Power Management capability.

2.2.2 Offset PMCAP + 2h: PC – PCI Power Management Capabilities

Figure 32: Offset PMCAP + 2h: PC – PCI Power Management Capabilities

Bits	Type	Reset	Description
15:11	RO	0h	**PME_Support (PSUP):** Not supported by the NVM Express interface.
10	RO	0b	**D2_Support (D2S):** Indicates support for the D2 power management state. Not recommended for implementation.
09	RO	0b	**D1_Support (D1S):** Indicates support for the D1 power management state. Not recommended for implementation.
08:06	RO	000b	**Aux_Current (AUXC):** Not supported by the NVM Express interface.
05	RO	Impl Spec	**Device Specific Initialization (DSI):** Indicates whether device specific initialization is required.
04	RO	0b	Reserved
03	RO	0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
02:00	RO	Impl Spec	**Version (VS):** Indicates support for revision 1.2 or higher revisions of the PCI Power Management Specification.

2.2.3 Offset PMCAP + 4h: PMCS – PCI Power Management Control and Status

Figure 33: Offset PMCAP + 4h: PMCS – PCI Power Management Control and Status

Bits	Type	Reset	Description
15	RWC	0b	**PME Status (PMES):** Refer to the PCI SIG specifications.
14:13	RO	00b	**Data Scale (DSC):** Refer to the PCI SIG specifications.
12:09	RO / RW	0h	**Data Select (DSE):** If PME is not supported, then this field is read only '0'. Refer to the PCI SIG specifications.
08	RO / RW	0b	**PME Enable (PMEE):** If PME is not supported, then this bit is read only '0'. Refer to the PCI SIG specifications.
07:04	RO	0h	Reserved
03	RO	1b	**No Soft Reset (NSFRST):** A value of '1' indicates that the controller transitioning from D3hot to D0 because of a power state command does not perform an internal reset.
02	RO	0b	Reserved
01:00	RW	00b	**Power State (PS):** This field is used both to determine the current power state of the controller and to set a new power state. The values are: 00b – D0 state 01b – D1 state 10b – D2 state 11b – $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the register I/O and memory spaces are not. Additionally, interrupts are blocked.

2.3 Message Signaled Interrupt Capability (Optional)

Figure 34: Message Signaled Interrupt Capability (Optional)

Start	End	Symbol	Name
MSICAP	MSICAP+1h	MID	Message Signaled Interrupt Capability ID
MSICAP+2h	MSICAP+3h	MC	Message Signaled Interrupt Message Control
MSICAP+4h	MSICAP+7h	MA	Message Signaled Interrupt Message Address
MSICAP+8h	MSICAP+Bh	MUA	Message Signaled Interrupt Upper Address
MSICAP+Ch	MSICAP+Dh	MD	Message Signaled Interrupt Message Data
MSICAP+10h	MSICAP+13h	MMASK	Message Signaled Interrupt Mask Bits (Optional)
MSICAP+14h	MSICAP+17h	MPEND	Message Signaled Interrupt Pending Bits (Optional)

2.3.1 Offset MSICAP: MID – Message Signaled Interrupt Identifiers

Figure 35: Offset MSICAP: MID – Message Signaled Interrupt Identifiers

Bits	Type	Reset	Description
15:08	RO	Impl Spec	**Next Pointer (NEXT):** Indicates the next item in the list. This may be a capability pointer or may be the last item in the list.
07:00	RO	5h	**Capability ID (CID):** Capabilities ID indicates this is a Message Signaled Interrupt (MSI) capability.

2.3.2 Offset MSICAP + 2h: MC – Message Signaled Interrupt Message Control

Figure 36: Offset MSICAP + 2h: MC – Message Signaled Interrupt Message Control

Bits	Type	Reset	Description
15:09	RO	0h	Reserved
08	RO	Impl Spec	**Per-Vector Masking Capable (PVM):** Specifies whether controller supports MSI per-vector masking.
07	RO	1b	**64 Bit Address Capable (C64):** Specifies whether the controller is capable of generating 64-bit messages. NVM Express controllers shall be 64-bit capable.
06:04	RW	000b	**Multiple Message Enable (MME):** Indicates the number of messages the controller should assert. Controllers that only support single message MSI may implement this field as read-only.
03:01	RO	Impl Spec	**Multiple Message Capable (MMC):** Indicates the number of messages the controller is requesting.
00	RW	0b	**MSI Enable (MSIE):** If set to '1', MSI is enabled. If cleared to '0', MSI operation is disabled.

2.3.3 Offset MSICAP + 4h: MA – Message Signaled Interrupt Message Address

Figure 37: Offset MSICAP + 4h: MA – Message Signaled Interrupt Message Address

Bits	Type	Reset	Description
31:02	RW	0h	**Address (ADDR):** Lower 32 bits of the system specified message address, always dword aligned.
01:00	RO	00b	Reserved

2.3.4 Offset MSICAP + 8h: MUA – Message Signaled Interrupt Upper Address

Figure 38: Offset MSICAP + 8h: MUA – Message Signaled Interrupt Upper Address

Bits	Type	Reset	Description
31:00	RW	0h	**Upper Address (UADDR):** Upper 32 bits of the system specified message address. This register is required when the MSI Capability is supported by the controller.

2.3.5 Offset MSICAP + Ch: MD – Message Signaled Interrupt Message Data

Figure 39: Offset MSICAP + Ch: MD – Message Signaled Interrupt Message Data

Bits	Type	Reset	Description
15:00	RW	0h	**Data (DATA):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

2.3.6 Offset MSICAP + 10h: MMASK – Message Signaled Interrupt Mask Bits (Optional)

Figure 40: Offset MSICAP + 10h: MMASK – Message Signaled Interrupt Mask Bits (Optional)

Bits	Type	Reset	Description
31:00	RW	0h	**Mask Bits (MASK):** For each Mask bit that is set to '1', the function is prohibited from sending the associated message.

2.3.7 Offset MSICAP + 14h: MPEND – Message Signaled Interrupt Pending Bits (Optional)

Figure 41: Offset MSICAP + 14h: MPEND – Message Signaled Interrupt Pending Bits (Optional)

Bits	Type	Reset	Description
31:00	RO	0h	**Pending Bits (PEND):** For each Pending bit that is set to '1', the function has a pending associated message.

2.4 MSI-X Capability (Optional)

Figure 42: MSI-X Capability (Optional)

Start	End	Symbol	Name
MSIXCAP	MSIXCAP+1h	MXID	MSI-X Capability ID
MSIXCAP+2h	MSIXCAP+3h	MXC	MSI-X Message Control
MSIXCAP+4h	MSIXCAP+7h	MTAB	MSI-X Table Offset and Table BIR
MSIXCAP+8h	MSIXCAP+Bh	MPBA	MSI-X PBA Offset and PBA BIR

Note: It is recommended that the host allocate a unique MSI-X vector for each Completion Queue.

The Table BIR and PBA BIR data structures may be allocated in either BAR0-1 or BAR4-5 in implementations. These tables should be 4 KiB aligned. The memory page(s) that comprise the Table BIR and PBA BIR shall not include other registers/structures. It is recommended that these structures be allocated in BAR0-1 following the Submission Queue and Completion Queue Doorbell registers. Refer to the PCI reference for more information on allocation requirements for these data structures.

2.4.1 Offset MSIXCAP: MXID – MSI-X Identifiers

Figure 43: Offset MSIXCAP: MXID – MSI-X Identifiers

Bits	Type	Reset	Description
15:08	RO	Impl Spec	**Next Pointer (NEXT):** Indicates the next item in the list. This may be a capability pointer or may be the last item in the list.
07:00	RO	11h	**Capability ID (CID):** Capabilities ID indicates this is an MSI-X capability.

2.4.2 Offset MSIXCAP + 2h: MXC – MSI-X Message Control

Figure 44: Offset MSIXCAP + 2h: MXC – MSI-X Message Control

Bits	Type	Reset	Description
15	RW	0b	**MSI-X Enable (MXE):** If set to '1' and the MSI Enable bit in the MSI Message Control register is cleared to '0', the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin (if implemented). If cleared to '0', the function is prohibited from using MSI-X to request service.
14	RW	0b	**Function Mask (FM):** If set to '1', all of the vectors associated with the function are masked, regardless of their per vector Mask bit states. If cleared to '0', each vector's Mask bit determines whether the vector is masked or not. Setting to '1' or clearing to '0' the MSI-X Function Mask bit has no effect on the state of the per vector Mask bits.
13:11	RO	000b	Reserved
10:00	RO	Impl Spec	**Table Size (TS):** This value indicates the size of the MSI-X Table as the value *n*, which is encoded as *n* - 1. For example, a returned value of 3h corresponds to a table size of 4.

2.4.3 Offset MSIXCAP + 4h: MTAB – MSI-X Table Offset / Table BIR

Figure 45: Offset MSIXCAP + 4h: MTAB – MSI-X Table Offset / Table BIR

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:03</td><td>RO</td><td>Impl Spec</td><td>Table Offset (TO): Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower three Table BIR bits are masked off (cleared to 000b) by system software to form a 32-bit qword-aligned offset.</td></tr>
<tr><td>02:00</td><td>RO</td><td>Impl Spec</td><td>Table BIR (TBIR): This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into system memory.
<table>
<tr><th>BIR Value</th><th>BAR Offset</th></tr>
<tr><td>0h</td><td>10h</td></tr>
<tr><td>1h</td><td>n/a</td></tr>
<tr><td>2h</td><td>n/a</td></tr>
<tr><td>3h</td><td>Reserved</td></tr>
<tr><td>4h</td><td>20h</td></tr>
<tr><td>5h</td><td>24h</td></tr>
<tr><td>6h</td><td>Reserved</td></tr>
<tr><td>7h</td><td>Reserved</td></tr>
</table>
For a 64-bit Base Address register, the Table BIR indicates the lower dword. With PCI-to-PCI bridges, BIR values 2h to 5h are also reserved.</td></tr>
</table>

2.4.4 Offset MSIXCAP + 8h: MPBA – MSI-X PBA Offset / PBA BIR

Figure 46: Offset MSIXCAP + 8h: MPBA – MSI-X PBA Offset / PBA BIR

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:03</td><td>RO</td><td>Impl Spec</td><td>PBA Offset (PBAO): Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower three PBA BIR bits are masked off (cleared to 000b) by software to form a 32-bit qword-aligned offset.</td></tr>
<tr><td>02:00</td><td>RO</td><td>Impl Spec</td><td>PBA BIR (PBIR): This field indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into system memory.
<table>
<tr><th>BIR Value</th><th>BAR Offset</th></tr>
<tr><td>0h</td><td>10h</td></tr>
<tr><td>1h</td><td>n/a</td></tr>
<tr><td>2h</td><td>n/a</td></tr>
<tr><td>3h</td><td>Reserved</td></tr>
<tr><td>4h</td><td>20h</td></tr>
<tr><td>5h</td><td>24h</td></tr>
<tr><td>6h</td><td>Reserved</td></tr>
<tr><td>7h</td><td>Reserved</td></tr>
</table></td></tr>
</table>

2.5 PCI Express Capability

The PCI Express Capability definitions below are based on the PCI Express 2.1 Base specification. Implementations may choose to base the device on a specification beyond the PCI Express 2.1 Base specification. In all cases, the PCI Express Base specification is the normative reference for the PCI Express Capability registers.

Note: TLP poisoning is a mandatory capability for PCI Express implementations. There are optional features of TLP poisoning, such as TLP poisoning for a transmitter. When an NVM Express controller has an error on a transmission to the host (e.g., error for a Read command), the error should be indicated as part of the NVM Express command status and not via TLP poisoning.

Figure 47: PCI Express Capability

Start	End	Symbol	Name
PXCAP	PXCAP+1h	PXID	PCI Express Capability ID
PXCAP+2h	PXCAP+3h	PXCAP	PCI Express Capabilities
PXCAP+4h	PXCAP+7h	PXDCAP	PCI Express Device Capabilities
PXCAP+8h	PXCAP+9h	PXDC	PCI Express Device Control
PXCAP+Ah	PXCAP+Bh	PXDS	PCI Express Device Status
PXCAP+Ch	PXCAP+Fh	PXLCAP	PCI Express Link Capabilities
PXCAP+10h	PXCAP+11h	PXLC	PCI Express Link Control
PXCAP+12h	PXCAP+13h	PXLS	PCI Express Link Status
PXCAP+24h	PXCAP+27h	PXDCAP2	PCI Express Device Capabilities 2
PXCAP+28h	PXCAP+29h	PXDC2	PCI Express Device Control 2

2.5.1 Offset PXCAP: PXID – PCI Express Capability ID

Figure 48: Offset PXCAP: PXID – PCI Express Capability ID

Bits	Type	Reset	Description
15:8	RO	Impl Spec	**Next Pointer (NEXT):** Indicates the next item in the list. This may be a capability pointer or may be the last item in the list.
7:0	RO	10h	**Capability ID (CID):** Indicates that this capability structure is a PCI Express capability.

2.5.2 Offset PXCAP + 2h: PXCAP – PCI Express Capabilities

Figure 49: Offset PXCAP + 2h: PXCAP – PCI Express Capabilities

Bits	Type	Reset	Description
15:14	RO	00b	Reserved
13:9	RO	Impl Spec	**Interrupt Message Number (IMN):** This field indicates the MSI/MSI-X vector that is used for the interrupt message generated in association with any of the status bits of this Capability structure. There are no status bits that generate interrupts defined in this capability within this specification, thus this field is not used.
8	RO	0b	**Slot Implemented (SI):** Not applicable for PCI Express Endpoint devices.
7:4	RO	0h	**Device/Port Type (DPT):** Indicates the specific type of this PCI Express function. This device shall be indicated as a PCI Express Endpoint.
3:0	RO	2h	**Capability Version (VER):** Indicates that this capability structure is a PCI Express capability structure.

2.5.3 Offset PXCAP + 4h: PXDCAP – PCI Express Device Capabilities

Figure 50: Offset PXCAP + 4h: PXDCAP – PCI Express Device Capabilities

Bits	Type	Reset	Description
31:29	RO	000b	Reserved
28	RO	1b	**Function Level Reset Capability (FLRC):** A value of '1' indicates the Function supports the optional Function Level Reset mechanism. NVM Express controllers shall support Function Level Reset.
27:26	RO	00b	**Captured Slot Power Limit Scale (CSPLS):** Specifies the scale used for the Slot Power Limit Value.
25:18	RO	0h	**Captured Slot Power Limit Value (CSPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by the slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field.
17:16	RO	00b	Reserved
15	RO	1b	**Role-based Error Reporting (RER):** When set to '1', indicates that the Function implements role-based error reporting. This functionality is required.
14:12	RO	000b	Reserved
11:9	RO	Impl Spec	**Endpoint L1 Acceptable Latency (L1L):** This field indicates the acceptable latency that the Endpoint is able to withstand due to a transition from the L1 state to the L0 state.
08:06	RO	Impl Spec	**Endpoint L0s Acceptable Latency (L0SL):** This field indicates the acceptable total latency that the Endpoint is able to withstand due to the transition from L0s state to the L0 state.
05	RO	Impl Spec	**Extended Tag Field Supported (ETFS):** This bit indicates the maximum supported size of the Tag field as a Requester.
04:03	RO	Impl Spec	**Phantom Functions Supported (PFS):** This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions allowed by logically combining unclaimed Function Numbers with the Tag identifier.
02:00	RO	Impl Spec	**Max_Payload_Size Supported (MPS):** This field indicates the maximum payload size that the function may support for TLPs.

2.5.4 Offset PXCAP + 8h: PXDC – PCI Express Device Control

Figure 51: Offset PXCAP + 8h: PXDC – PCI Express Device Control

Bits	Type	Reset	Description
15	RW	0b	**Initiate Function Level Reset:** A write of '1' initiates Function Level Reset to the Function. The value read by software from this bit shall always '0'.
14:12	RW/ RO	Impl Spec	**Max_Read_Request_Size (MRRS):** This field sets the maximum Read Request size for the Function as a Requester. The Function shall not generate Read Requests with size exceeding the set value.
11	RW/ RO	Impl Spec	**Enable No Snoop (ENS):** If this bit is set to '1', the Function is permitted to set the No Snoop bit in the Requestor Attributes of transactions it initiates that do not require hardware enforced cache coherency. This bit may be hardwired to '0' if a Function would never set the No Snoop attribute in transactions it initiates.
10	RW/ RO	0b	**AUX Power PM Enable (APPME):** If this bit is set to '1', enables a Function to draw AUX power independent of PME AUX power. Functions that do not implement this capability hardware this bit to '0'.
09	RW/ RO	0b	**Phantom Functions Enable (PFE):** If this bit is set to '1', enables a Function to use unclaimed Functions as Phantom Functions to extend the number of outstanding transaction identifiers. If this bit is cleared to '0', the Function is not allowed to use Phantom Functions.
08	RW/ RO	0b	**Extended Tag Enable (ETE):** If this bit is set to '1', enables a Function to use an 8-bit Tag field as a Requester. If this bit is cleared to '0', the Function is restricted to a 5-bit Tag field.
07:05	RW/ RO	000b	**Max_Payload_Size (MPS):** This field sets the maximum TLP payload size for the Function. As a receiver, the Function shall handle TLPs as large as the set value. As a transmitter, the Function shall not generate TLPs exceeding the set value. Functions that support only the 128 byte max payload size are permitted to hardwire this field to 0h.
04	RW/ RO	Impl Spec	**Enable Relaxed Ordering (ERO):** If this bit is set to '1', the Function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering.
03	RW	0b	**Unsupported Request Reporting Enable (URRE):** This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending error messages.
02	RW	0b	**Fatal Error Reporting Enable (FERE):** This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending ERR_FATAL messages.
01	RW	0b	**Non-Fatal Error Reporting Enable (NFERE):** This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending ERR_NONFATAL messages.
00	RW	0b	**Correctable Error Reporting Enable (CERE):** This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending ERR_COR messages.

2.5.5 Offset PXCAP + Ah: PXDS – PCI Express Device Status

Figure 52: Offset PXCAP + Ah: PXDS – PCI Express Device Status

Bits	Type	Reset	Description
15:06	RO	0h	Reserved
05	RO	0b	**Transactions Pending (TP):** When set to '1' this bit indicates that the Function has issued non-posted requests that have not been completed. This bit is cleared to '0' only when all outstanding non-posted requests have completed or have been terminated by the completion timeout mechanism. This bit shall also be cleared to '0' upon completion of a Function Level Reset.
04	RO	Impl Spec	**AUX Power Detected (APD):** Functions that require AUX power report this bit as set to '1' if AUX power is detected by the Function.
03	RWC	0b	**Unsupported Request Detected (URD):** When set to '1' this bit indicates that the Function received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.

Figure 52: Offset PXCAP + Ah: PXDS – PCI Express Device Status

Bits	Type	Reset	Description
02	RWC	0b	**Fatal Error Detected (FED):** When set to '1' this bit indicates that the status of fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.
01	RWC	0b	**Non-Fatal Error Detected (NFED):** When set to '1' this bit indicates that the status of non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.
00	RWC	0b	**Correctable Error Detected (CED):** When set to '1' this bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled in the Device Control register.

2.5.6 Offset PXCAP + Ch: PXLCAP – PCI Express Link Capabilities

Figure 53: Offset PXCAP + Ch: PXLCAP – PCI Express Link Capabilities

Bits	Type	Reset	Description
31:24	RO	HwInit	**Port Number (PN):** This field specifies the PCI Express port number for this device.
23	RO	0b	Reserved
22	RO	HwInit	**ASPM Optionality Compliance (AOC):** This bit specifies Active State Power Management (ASPM) support.
21	RO	0b	**Link Bandwidth Notification Capability (LBNC):** Not applicable to Endpoints.
20	RO	0b	**Data Link Layer Link Active Reporting Capable (DLLLA):** Not applicable to Endpoints.
19	RO	0b	**Surprise Down Error Reporting Capable (SDERC):** Not applicable to Endpoints.
18	RO	Impl Spec	**Clock Power Management (CPM):** If this bit is set to '1', the component tolerates the removal of any reference clock(s) via the "clock request" (CLKREQ#) mechanism when the Link is in the L1 and L2/L3 Ready Link states. If this bit is cleared to '0', the component does not have this capability and that reference clock(s) shall not be removed in these Link states.
17:15	RO	Impl Spec	**L1 Exit Latency (L1EL):** This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete transition from L1 to L0.
14:12	RO	Impl Spec	**L0s Exit Latency (L0SEL):** This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete transition from L0s to L0.
11:10	RO	Impl Spec	**Active State Power Management Support (ASPMS):** This field indicates the level of ASPM supported on the given PCI Express Link.
09:04	RO	Impl Spec	**Maximum Link Width (MLW):** This field indicates the maximum Link width (x*n* – corresponding to *n* lanes) implemented by the component.
03:00	RO	Impl Spec	**Supported Link Speeds (SLS):** This field indicates the supported Link speed(s) of the associated port.

2.5.7 Offset PXCAP + 10h: PXLC – PCI Express Link Control

Figure 54: Offset PXCAP + 10h: PXLC – PCI Express Link Control

Bits	Type	Reset	Description
15:10	RO	0h	Reserved
09	RW/ RO	0b	**Hardware Autonomous Width Disable (HAWD):** When set to '1', disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Components that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to '0'.

Figure 54: Offset PXCAP + 10h: PXLC – PCI Express Link Control

Bits	Type	Reset	Description
08	RW	0b	**Enable Clock Power Management (ECPM):** When cleared to '0', clock power management is disabled and the device shall hold the CLKREQ# signal low. When set to '1', the device is permitted to use the CLKREQ# signal to power manage the Link clock according to the protocol defined for mini PCI Express.
07	RW	0b	**Extended Synch (ES):** When set to '1', this bit forces the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the Link enters the L0 state and resumes communication.
06	RW	0b	**Common Clock Configuration (CCC):** When set to '1', this bit indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. When cleared to '0' this component and the component at the opposite end of this Link are operating with asynchronous reference clocks.
05:04	RO	00b	Reserved: These bits are reserved on Endpoints.
03	RW	0b	**Read Completion Boundary (RCB):** Indicate the RCB value of the root port.
02	RO	0b	Reserved
01:00	RW	00b	**Active State Power Management Control (ASPMC):** This field controls the level of ASPM executed on the PCI Express Link.

2.5.8 Offset PXCAP + 12h: PXLS – PCI Express Link Status

Figure 55: Offset PXCAP + 12h: PXLS – PCI Express Link Status

Bits	Type	Reset	Description
15:13	RO	000b	Reserved
12	RO	Impl Spec	**Slot Clock Configuration:** If this bit is set to '1', it indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of a reference on the connector, this bit shall be cleared to '0'.
11:10	RO	00b	Reserved
09:04	RO	n/a	**Negotiated Link Width (NLW):** This field indicates the negotiated Link width. This field is undefined when the Link is not up.
03:00	RO	n/a	**Current Link Speed (CLS):** This field indicates the negotiated Link speed. This field is undefined when the Link is not up.

2.5.9 Offset PXCAP + 24h: PXDCAP2 – PCI Express Device Capabilities 2

Figure 56: Offset PXCAP + 24h: PXDCAP2 – PCI Express Device Capabilities 2

Bits	Type	Reset	Description
31:24	RO	0h	Reserved
23:22	RO	Impl Spec	**Max End-End TLP Prefixes (MEETP):** Indicates the maximum number of End-End TLP Prefixes supported by this Function. TLPs received by this Function that contain more End-End TLP Prefixes than are supported shall be handled as Malformed TLPs.
21	RO	Impl Spec	**End-End TLP Prefix Supported (EETPS):** Indicates whether End-End TLP Prefix support is offered by a Function. If cleared to '0', there is no support. If set to '1', the Function supports receiving TLPs containing End-End TLP Prefixes.
20	RO	Impl Spec	**Extended Fmt Field Supported (EFFS):** If set to '1', the Function supports the 3-bit definition of the Fmt field. If cleared to '0', the Function supports a 2-bit definition of the Fmt field.
19:18	RO	Impl Spec	**OBFF Supported (OBFFS):** This field indicates the level of support for OBFF.
17:14	RO	0h	Reserved

Figure 56: Offset PXCAP + 24h: PXDCAP2 – PCI Express Device Capabilities 2

Bits	Type	Reset	Description
13:12	RO	Impl Spec	**TPH Completer Supported (TPHCS):** Defined encodings are listed in the following table. **Value** / **Definition** 00b – TPH and Extended TPH Completer not supported 01b – TPH Completer supported; Extended TPH Completer not supported 10b – Reserved 11b – Both TPH and Extended TPH Completer supported
11	RO	Impl Spec	**Latency Tolerance Reporting Supported (LTRS):** If set to '1', then the latency tolerance reporting mechanism is supported.
10	RO	0b	**No RO-enabled PR-PR Passing (NPRPR):** Not applicable to the NVM Express interface.
09	RO	Impl Spec	**128-bit CAS Completer Supported (128CCS):** This bit shall be set to '1' if the Function supports this optional capability.
08	RO	Impl Spec	**64-bit AtomicOp Completer Supported (64AOCS):** Includes FetchAdd, Swap, and CAS AtomicOps. This bit shall be set to '1' if the Function supports this optional capability.
07	RO	Impl Spec	**32-bit AtomicOp Completer Supported (32AOCS):** Includes FetchAdd, Swap, and CAS AtomicOps. This bit shall be set to '1' if the Function supports this optional capability.
06	RO	0b	**AtomicOp Routing Supported (AORS):** Not applicable to the NVM Express interface.
05	RO	0b	**ARI Forwarding Supported (ARIFS):** Not applicable for the NVM Express interface.
04	RO	1b	**Completion Timeout Disable Supported (CTDS):** A value of '1' indicates support for the Completion Timeout Disable mechanism. The Completion Timeout Disable mechanism is required for Endpoints that issue requests on their own behalf.
03:00	RO	Impl Spec	**Completion Timeout Ranges Supported (CTRS):** This field indicates device function support for the optional Completion Timeout programmability mechanism.

2.5.10 Offset PXCAP + 28h: PXDC2 – PCI Express Device Control 2

Figure 57: Offset PXCAP + 28h: PXDC2 – PCI Express Device Control 2

Bits	Type	Reset	Description
31:15	RO	0h	Reserved
14:13	RW	Impl Spec	**OBFF Enable (OBFFE):** This field controls the capabilities enabled for OBFF.
12:11	RO	00b	Reserved
10	RW	0b	**Latency Tolerance Reporting Mechanism Enable (LTRME):** When set to '1', enables the LTR mechanism. When cleared to '0', the LTR mechanism is disabled.
09:05	RO	0h	Reserved
04	RW	0b	**Completion Timeout Disable (CTD):** When set to '1', this bit disables the Completion Timeout mechanism.
03:00	RW/RO	Impl Spec	**Completion Timeout Value:** Specifies the completion timeout value. If this feature is not supported in PXDCAP2, then this field is read only 0h.

2.6 Advanced Error Reporting Capability (Optional)

The Advanced Error Reporting definitions below are based on the PCI Express 2.1 Base specification. Implementations may choose to base the device on a specification beyond the PCI Express 2.1 Base specification. In all cases, the PCI Express Base specification is the normative reference for the Advanced Error Reporting registers.

Figure 58: Advanced Error Reporting Capability (Optional)

Start	End	Symbol	Name
AERCAP	AERCAP+3h	AERID	AER Capability ID
AERCAP+4h	AERCAP+7h	AERUCES	AER Uncorrectable Error Status Register
AERCAP+8h	AERCAP+Bh	AERUCEM	AER Uncorrectable Error Mask Register
AERCAP+Ch	AERCAP+Fh	AERUCESEV	AER Uncorrectable Error Severity Register
AERCAP+10h	AERCAP+13h	AERCES	AER Correctable Error Status Register
AERCAP+14h	AERCAP+17h	AERCEM	AER Correctable Error Mask Register
AERCAP+18h	AERCAP+1Bh	AERCC	AER Advanced Error Capabilities and Control Reg.
AERCAP+1Ch	AERCAP+2Bh	AERHL	AER Header Log Register
AERCAP+38h	AERCAP+47h	AERTLP	AER TLP Prefix Log Register (Optional)

2.6.1 Offset AERCAP: AERID – AER Capability ID

Figure 59: Offset AERCAP: AERID – AER Capability ID

Bits	Type	Reset	Description
31:20	RO	Impl Spec	**Next Pointer (NEXT):** Indicates the next item in the list. This may be a capability pointer or may be the last item in the list.
19:16	RO	Impl Spec	**Capability Version (CVER):** Indicates the version of the capability structure. Reset value may be 1h or 2h.
15:0	RO	1h	**Capability ID (CID):** Indicates that this capability structure is an Advanced Error Reporting capability.

2.6.2 Offset AERCAP + 4: AERUCES – AER Uncorrectable Error Status Register

This register indicates the error detection status of the individual errors on the controller. These bits are sticky – they are neither initialized nor modified during a hot reset or Function Level Reset (FLR).

Figure 60: Offset AERCAP + 4: AERUCES – AER Uncorrectable Error Status Register

Bits	Type	Reset	Description
31:26	RO	0h	Reserved
25	RWC/RO	0b	TLP Prefix Blocked Error Status (TPBES) (Optional)
24	RWC/RO	0b	AtomicOp Egress Blocked Status (AOEBS) (Optional)
23	RWC/RO	0b	MC Blocked TLP Status (MCBTS) (Optional)
22	RWC/RO	0b	Uncorrectable Internal Error Status (UIES) (Optional)
21	RWC/RO	0b	ACS Violation Status (ACSVS) (Optional)
20	RWC	0b	Unsupported Request Error Status (URES)
19	RWC/RO	0b	ECRC Error Status (ECRCES) (Optional)
18	RWC	0b	Malformed TLP Status (MTS)
17	RWC/RO	0b	Receiver Overflow Status (ROS) (Optional)
16	RWC	0b	Unexpected Completion Status (UCS)
15	RWC/RO	0b	Completer Abort Status (CAS) (Optional)
14	RWC	0b	Completion Timeout Status (CTS)
13	RWC/RO	0b	Flow Control Protocol Error Status (FCPES) (Optional)
12	RWC	0b	Poisoned TLP Status (PTS)
11:05	RO	0h	Reserved
04	RWC	0b	Data Link Protocol Error Status (DLPES)
03:00	RO	0h	Reserved

2.6.3 Offset AERCAP + 8: AERUCEM – AER Uncorrectable Error Mask Register

This register controls the reporting of the individual errors by the controller. A masked error is not reported in the Header Log register (AERHL), does not updated the First Error Pointer (AERCC.FEP), and is not reported to the host. These bits are sticky – they are neither initialized nor modified during a hot reset or FLR.

Figure 61: Offset AERCAP + 8: AERUCEM – AER Uncorrectable Error Mask Register

Bits	Type	Reset	Description
31:26	RO	0h	Reserved
25	RW/RO	0b	TLP Prefix Blocked Error Mask (TPBEM) (Optional)
24	RW/RO	0b	AtomicOp Egress Blocked Mask (AOEBM) (Optional)
23	RW/RO	0b	MC Blocked TLP Mask (MCBTM) (Optional)
22	RW/RO	1b	Uncorrectable Internal Error Mask (UIEM) (Optional)
21	RW/RO	0b	ACS Violation Mask (ACSVM) (Optional)
20	RW	0b	Unsupported Request Error Mask (UREM)
19	RW/RO	0b	ECRC Error Mask (ECRCEM) (Optional)
18	RW	0b	Malformed TLP Mask (MTM)
17	RW/RO	0b	Receiver Overflow Mask (ROM) (Optional)
16	RW	0b	Unexpected Completion Mask (UCM)
15	RW/RO	0b	Completer Abort Mask (CAM) (Optional)
14	RW	0b	Completion Timeout Mask (CTM)
13	RW/RO	0b	Flow Control Protocol Error Mask (FCPEM) (Optional)
12	RW	0b	Poisoned TLP Mask (PTM)
11:05	RO	0h	Reserved
04	RW	0b	Data Link Protocol Error Mask (DLPEM)
03:00	RO	0h	Reserved

2.6.4 Offset AERCAP + Ch: AERUCESEV – AER Uncorrectable Error Severity Register

This register controls whether an individual error is reported as a non-fatal or a fatal error. An error is reported as fatal when the corresponding error bit in the severity register is set to ‘1’. If the bit is cleared to ‘0’, the corresponding error is considered non-fatal. These bits are sticky – they are neither initialized nor modified during a hot reset or FLR.

Figure 62: Offset AERCAP + Ch: AERUCESEV – AER Uncorrectable Error Severity Register

Bits	Type	Reset	Description
31:26	RO	0h	Reserved
25	RW/RO	0b	TLP Prefix Blocked Error Severity (TPBESEV) (Optional)
24	RW/RO	0b	AtomicOp Egress Blocked Severity (AOEBSEV) (Optional)
23	RW/RO	0b	MC Blocked TLP Severity (MCBTSEV) (Optional)
22	RW/RO	1b	Uncorrectable Internal Error Severity (UIESEV) (Optional)
21	RW/RO	0b	ACS Violation Severity (ACSVSEV) (Optional)
20	RW	0b	Unsupported Request Error Severity (URESEV)
19	RW/RO	0b	ECRC Error Severity (ECRCESEV) (Optional)
18	RW	1b	Malformed TLP Severity (MTSEV)
17	RW/RO	1b	Receiver Overflow Severity (ROSEV) (Optional)
16	RW	0b	Unexpected Completion Severity (UCSEV)
15	RW/RO	0b	Completer Abort Severity (CASEV) (Optional)
14	RW	0b	Completion Timeout Severity (CTSEV)
13	RW/RO	1b	Flow Control Protocol Error Severity (FCPESEV) (Optional)
12	RW	0b	Poisoned TLP Severity (PTSEV)
11:05	RO	0h	Reserved
04	RW	1b	Data Link Protocol Error Severity (DLPESEV)
03:00	RO	0h	Reserved

2.6.5 Offset AERCAP + 10h: AERCES – AER Correctable Error Status Register

This register reports error status of individual correctable error sources from the controller. These bits are sticky – they are neither initialized nor modified during a hot reset or FLR.

Figure 63: Offset AERCAP + 10h: AERCES – AER Correctable Error Status Register

Bits	Type	Reset	Description
31:16	RO	0h	Reserved
15	RWC/RO	0b	Header Log Overflow Status (HLOS) (Optional)
14	RWC/RO	0b	Corrected Internal Error Status (CIES) (Optional)
13	RWC	0b	Advisory Non-Fatal Error Status (ANFES)
12	RWC	0b	Replay Timer Timeout Status (RTS)
11:09	RO	000b	Reserved
08	RWC	0b	REPLAY_NUM Rollover Status (RRS)
07	RWC	0b	Bad DLLP Status (BDS)
06	RWC	0b	Bad TLP Status (BTS)
05:01	RO	0h	Reserved
00	RWC	0b	Receiver Error Status (RES)

2.6.6 Offset AERCAP + 14h: AERCEM – AER Correctable Error Mask Register

This register controls the reporting of the individual correctable errors by the controller. A masked error is not reported to the host. These bits are sticky – they are neither initialized nor modified during a hot reset or FLR.

Figure 64: Offset AERCAP + 14h: AERCEM – AER Correctable Error Mask Register

Bits	Type	Reset	Description
31:16	RO	0h	Reserved
15	RW/RO	1b	Header Log Overflow Mask (HLOM) (Optional)
14	RW/RO	1b	Corrected Internal Error Mask (CIEM) (Optional)
13	RW	1b	Advisory Non-Fatal Error Mask (ANFEM)
12	RW	0b	Replay Timer Timeout Mask (RTM)
11:09	RO	000b	Reserved
08	RW	0b	REPLAY_NUM Rollover Mask (RRM)
07	RW	0b	Bad DLLP Mask (BDM)
06	RW	0b	Bad TLP Mask (BTM)
05:01	RO	0h	Reserved
00	RW	0b	Receiver Error Mask (REM)

2.6.7 Offset AERCAP + 18h: AERCC – AER Capabilities and Control Register

Figure 65: Offset AERCAP + 18h: AERCC – AER Capabilities and Control Register

Bits	Type	Reset	Description
31:12	RO	0h	Reserved
11	RO	0b	**TLP Prefix Log Present (TPLP):** If set to '1' and FEP is valid, this indicates that the TLP Prefix Log register contains valid information. This bit is sticky – it is neither initialized nor modified during a hot reset or FLR.
10	RW/RO	0b	**Multiple Header Recording Enable (MHRE):** If this bit is set to '1', this enables the controller to generate more than one error header. This bit is sticky – it is neither initialized nor modified during a hot reset or FLR. If the controller does not implement the associated mechanism, then this bit is cleared to '0'.
09	RW/RO	Impl Spec	**Multiple Header Recording Capable (MHRC):** If this bit is set to '1', indicates that the controller is capable of generating more than one error header.

Figure 65: Offset AERCAP + 18h: AERCC – AER Capabilities and Control Register

Bits	Type	Reset	Description
08	RW/RO	0b	**ECRC Check Enable (ECE):** If this bit is set to '1', indicates that the ECRC checking is enabled. This bit is sticky – it is neither initialized nor modified during a hot reset or FLR. If the controller does not implement the associated mechanism, then this bit is cleared to '0'.
07	RO	Impl Spec	**ECRC Check Capable (ECC):** If this bit is set to '1', indicates that the controller is capable of checking ECRC.
06	RW/RO	0b	**ECRC Generation Enable (EGE):** If this bit is set to '1', indicates that the ECRC generation is enabled. This bit is sticky – it is neither initialized nor modified during a hot reset or FLR. If the controller does not implement the associated mechanism, then this bit is cleared to '0'.
05	RO	Impl Spec	**ECRC Generation Capable (EGC):** If this bit is set to '1', indicates that the controller is capable of generating ECRC.
04:00	RO	0h	**First Error Pointer (FEP):** This field identifies the bit position of the first error reported in the AERUCES register. This field is sticky – it is neither initialized nor modified during a hot reset or FLR.

2.6.8 Offset AERCAP + 1Ch: AERHL – AER Header Log Register

This register contains the header for the TLP corresponding to a detected error. This register is sticky – it is neither initialized nor modified during a hot reset or FLR.

Figure 66: Offset AERCAP + 1Ch: AERHL – AER Header Log Register

Byte	Type	Reset	Description
0	RO	0h	Header Byte 3 (HB3)
1	RO	0h	Header Byte 2 (HB2)
2	RO	0h	Header Byte 1 (HB1)
3	RO	0h	Header Byte 0 (HB0)
4	RO	0h	Header Byte 7 (HB7)
5	RO	0h	Header Byte 6 (HB6)
6	RO	0h	Header Byte 5 (HB5)
7	RO	0h	Header Byte 4 (HB4)
8	RO	0h	Header Byte 11 (HB11)
9	RO	0h	Header Byte 10 (HB10)
10	RO	0h	Header Byte 9 (HB9)
11	RO	0h	Header Byte 8 (HB8)
12	RO	0h	Header Byte 15 (HB15)
13	RO	0h	Header Byte 14 (HB14)
14	RO	0h	Header Byte 13 (HB13)
15	RO	0h	Header Byte 12 (HB12)

2.6.9 Offset AERCAP + 38h: AERTLP – AER TLP Prefix Log Register (Optional)

This register contains the End-End TLP prefix(es) for the TLP corresponding to a detected error. This register is sticky – it is neither initialized nor modified during a hot reset or FLR.

Figure 67: Offset AERCAP + 38h: AERTLP – AER TLP Prefix Log Register (Optional)

Byte	Type	Reset	Description
0	RO	0h	First TLP Prefix Log Byte 3 (TPL1B3)
1	RO	0h	First TLP Prefix Log Byte 2 (TPL1B2)
2	RO	0h	First TLP Prefix Log Byte 1 (TPL1B1)
3	RO	0h	First TLP Prefix Log Byte 0 (TPL1B0)
4	RO	0h	Second TLP Prefix Log Byte 3 (TPL2B3)
5	RO	0h	Second TLP Prefix Log Byte 2 (TPL2B2)

Figure 67: Offset AERCAP + 38h: AERTLP – AER TLP Prefix Log Register (Optional)

Byte	Type	Reset	Description
6	RO	0h	Second TLP Prefix Log Byte 1 (TPL2B1)
7	RO	0h	Second TLP Prefix Log Byte 0 (TPL2B0)
8	RO	0h	Third TLP Prefix Log Byte 3 (TPL3B3)
9	RO	0h	Third TLP Prefix Log Byte 2 (TPL3B2)
10	RO	0h	Third TLP Prefix Log Byte 1 (TPL3B1)
11	RO	0h	Third TLP Prefix Log Byte 0 (TPL3B0)
12	RO	0h	Fourth TLP Prefix Log Byte 3 (TPL4B3)
13	RO	0h	Fourth TLP Prefix Log Byte 2 (TPL4B2)
14	RO	0h	Fourth TLP Prefix Log Byte 1 (TPL4B1)
15	RO	0h	Fourth TLP Prefix Log Byte 0 (TPL4B0)

2.7 Other Capability Pointers

Though not mentioned in this specification, other capability pointers may be necessary, depending upon the implementation. Examples would be the PCI-X capability for PCI-X implementations, and potentially the vendor specific capability pointer.

These capabilities are beyond the scope of this specification.

3 Controller Registers

Controller registers are located in the MLBAR/MUBAR registers (PCI BAR0 and BAR1) that shall be mapped to a memory space that supports in-order access and variable access widths. For many computer architectures, specifying the memory space as uncacheable produces this behavior. The host shall not issue locked accesses. The host shall access a register using the width specified for that register or using aligned 32-bit accesses. Violation of either of these host requirements results in undefined behavior.

Accesses that target any portion of two or more registers are not supported.

All reserved registers and all reserved bits within registers are read-only and return 0h when read. Software shall not rely on 0h being returned.

3.1 Register Definition

Figure 68 describes the register map for the controller.

The Vendor Specific address range starts after the last doorbell supported by the controller and continues to the end of the BAR0/1 supported range. The start of the Vendor Specific address range starts at the same location and is not dependent on the number of allocated doorbells.

Figure 68: Register Definition

Start	End	Symbol	Description
0h	7h	CAP	Controller Capabilities
8h	Bh	VS	Version
Ch	Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	NSSR	NVM Subsystem Reset (Optional)
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	3Bh	CMBLOC	Controller Memory Buffer Location (Optional)
3Ch	3Fh	CMBSZ	Controller Memory Buffer Size (Optional)
40h	43h	BPINFO	Boot Partition Information (Optional)
44h	47h	BPRSEL	Boot Partition Read Select (Optional)
48h	4Fh	BPMBL	Boot Partition Memory Buffer Location (Optional)
50h	57h	CMBMSC	Controller Memory Buffer Memory Space Control (Optional)
58h	5Bh	CMBSTS	Controller Memory Buffer Status (Optional)
5Ch	DFFh	Reserved	Reserved
E00h	E03h	PMRCAP	Persistent Memory Capabilities
E04h	E07h	PMRCTL	Persistent Memory Region Control (Optional)
E08h	E0Bh	PMRSTS	Persistent Memory Region Status (Optional)
E0Ch	E0Fh	PMREBS	Persistent Memory Region Elasticity Buffer Size (Optional)
E10h	E13h	PMRSWTP	Persistent Memory Region Sustained Write Throughput (Optional)
E14h	E17h	PMRMSCL	Persistent Memory Region Controller Memory Space Control Lower (Optional)
E18h	E1Bh	PMRMSCU	Persistent Memory Region Controller Memory Space Control Upper (Optional)
E1Ch	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)

Figure 68: Register Definition

Start	End	Symbol	Description
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
1000h + (2 * (4 << CAP.DSTRD))	1003h + (2 * (4 << CAP.DSTRD))	SQ1TDBL	Submission Queue 1 Tail Doorbell
1000h + (3 * (4 << CAP.DSTRD))	1003h + (3 * (4 << CAP.DSTRD))	CQ1HDBL	Completion Queue 1 Head Doorbell
1000h + (4 * (4 << CAP.DSTRD))	1003h + (4 * (4 << CAP.DSTRD))	SQ2TDBL	Submission Queue 2 Tail Doorbell
1000h + (5 * (4 << CAP.DSTRD))	1003h + (5 * (4 << CAP.DSTRD))	CQ2HDBL	Completion Queue 2 Head Doorbell
…	…	…	…
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDBL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQyHDBL	Completion Queue y Head Doorbell
			Vendor Specific (Optional)

3.1.1 Offset 0h: CAP – Controller Capabilities

This register indicates basic capabilities of the controller to host software.

Figure 69: Offset 0h: CAP – Controller Capabilities

Bits	Type	Reset	Description
63: 58	RO	0h	Reserved
57	RO	Impl Spec	**Controller Memory Buffer Supported (CMBS):** If set to ‘1’, this bit indicates that the controller supports the Controller Memory Buffer, and that addresses supplied by the host are permitted to reference the Controller Memory Buffer only if the host has enabled the Controller Memory Buffer’s controller memory space. If the controller supports the Controller Memory Buffer, this bit shall be set to ‘1’.
56	RO	Impl Spec	**Persistent Memory Region Supported (PMRS):** This bit indicates whether the Persistent Memory Region is supported. This bit is set to ‘1’ if the Persistent Memory Region is supported. This bit is cleared to ‘0’ if the Persistent Memory Region is not supported.
55:52	RO	Impl Spec	**Memory Page Size Maximum (MPSMAX):** This field indicates the maximum host memory page size that the controller supports. The maximum memory page size is (2 ^ (12 + MPSMAX)). The host shall not configure a memory page size in CC.MPS that is larger than this value.
51:48	RO	Impl Spec	**Memory Page Size Minimum (MPSMIN):** This field indicates the minimum host memory page size that the controller supports. The minimum memory page size is (2 ^ (12 + MPSMIN)). The host shall not configure a memory page size in CC.MPS that is smaller than this value.
47:46	RO	00b	Reserved
45	RO	Impl Spec	**Boot Partition Support (BPS):** This bit indicates whether the controller supports Boot Partitions. If this bit is set to '1‘, the controller supports Boot Partitions. If this bit is cleared to ‘0‘, the controller does not support Boot Partitions. Refer to section 8.13.

Figure 69: Offset 0h: CAP – Controller Capabilities

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>44:37</td><td>RO</td><td>Impl Spec</td><td>Command Sets Supported (CSS): This field indicates the I/O Command Set(s) that the controller supports. If a bit is set to ‘1’, then the corresponding I/O Command Set is supported. If a bit is cleared to ‘0’, then the corresponding I/O Command Set is not supported. Bit 44 is set to ‘1’ if no I/O Command Set is supported.

<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>37</td><td>NVM command set</td></tr>
<tr><td>38</td><td>Reserved</td></tr>
<tr><td>39</td><td>Reserved</td></tr>
<tr><td>40</td><td>Reserved</td></tr>
<tr><td>41</td><td>Reserved</td></tr>
<tr><td>42</td><td>Reserved</td></tr>
<tr><td>43</td><td>Reserved</td></tr>
<tr><td>44</td><td>No I/O Command Set is supported (i.e., only the Admin Command Set is supported)</td></tr>
</table></td></tr>
<tr><td>36</td><td>RO</td><td>Impl Spec</td><td>NVM Subsystem Reset Supported (NSSRS): This bit indicates whether the controller supports the NVM Subsystem Reset feature defined in section 7.3.1. This bit is set to '1' if the controller supports the NVM Subsystem Reset feature. This bit is cleared to ‘0' if the controller does not support the NVM Subsystem Reset feature.</td></tr>
<tr><td>35:32</td><td>RO</td><td>Impl Spec</td><td>Doorbell Stride (DSTRD): Each Submission Queue and Completion Queue Doorbell register is 32-bits in size. This register indicates the stride between doorbell registers. The stride is specified as (2 ^ (2 + DSTRD)) in bytes. A value of 0h indicates a stride of 4 bytes, where the doorbell registers are packed without reserved space between each register. Refer to section 8.6.</td></tr>
<tr><td>31:24</td><td>RO</td><td>Impl Spec</td><td>Timeout (TO): This is the worst case time that host software shall wait for CSTS.RDY to transition from:

a) ‘0’ to ‘1’ after CC.EN transitions from ‘0’ to ‘1’; or
b) ‘1’ to ‘0’ after CC.EN transitions from ‘1’ to ‘0’.

This worst case time may be experienced after events such as an abrupt shutdown or activation of a new firmware image; typical times are expected to be much shorter. This field is in 500 millisecond units.</td></tr>
<tr><td>23:19</td><td>RO</td><td>0h</td><td>Reserved</td></tr>
<tr><td>18:17</td><td>RO</td><td>Impl Spec</td><td>Arbitration Mechanism Supported (AMS): This field is bit significant and indicates the optional arbitration mechanisms supported by the controller. If a bit is set to ‘1’, then the corresponding arbitration mechanism is supported by the controller. Refer to section 4.13 for arbitration details.

<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>17</td><td>Weighted Round Robin with Urgent Priority Class</td></tr>
<tr><td>18</td><td>Vendor Specific</td></tr>
</table>
The round robin arbitration mechanism is not listed since all controllers shall support this arbitration mechanism.</td></tr>
<tr><td>16</td><td>RO</td><td>Impl Spec</td><td>Contiguous Queues Required (CQR): This bit is set to ‘1’ if the controller requires that I/O Submission Queues and I/O Completion Queues are required to be physically contiguous. This bit is cleared to ‘0’ if the controller supports I/O Submission Queues and I/O Completion Queues that are not physically contiguous. If this bit is set to ‘1’, then the Physically Contiguous bit (CDW11.PC) in the Create I/O Submission Queue and Create I/O Completion Queue commands shall be set to ‘1’.</td></tr>
</table>

Figure 69: Offset 0h: CAP – Controller Capabilities

Bits	Type	Reset	Description
15:00	RO	Impl Spec	**Maximum Queue Entries Supported (MQES):** This field indicates the maximum individual queue size that the controller supports. For NVMe over PCIe implementations, this value applies to the I/O Submission Queues and I/O Completion Queues that the host creates. For NVMe over Fabrics implementations, this value applies to only the I/O Submission Queues that the host creates. This is a 0's based value. The minimum value is 1h, indicating two entries.

3.1.2 Offset 8h: VS – Version

This register indicates the major, minor, and tertiary version of the NVM Express base specification that the controller implementation supports. Valid versions of the specification are: 1.0, 1.1, 1.2, 1.2.1, 1.3, and 1.4.

3.1.2.1 VS Value for 1.0 Compliant Controllers

Figure 70: VS Value for 1.0 Compliant Controllers

Bits	Type	Reset	Description
31:16	RO	1h	**Major Version Number (MJR):** Indicates the major version is "1".
15:08	RO	0h	**Minor Version Number (MNR):** Indicates the minor version is "0".
07:00	RO	0h	Reserved

3.1.2.2 VS Value for 1.1 Compliant Controllers

Figure 71: VS Value for 1.1 Compliant Controllers

Bits	Type	Reset	Description
31:16	RO	1h	**Major Version Number (MJR):** Indicates the major version is "1".
15:08	RO	1h	**Minor Version Number (MNR):** Indicates the minor version is "1".
07:00	RO	0h	Reserved

3.1.2.3 VS Value for 1.2 Compliant Controllers

Figure 72: VS Value for 1.2 Compliant Controllers

Bits	Type	Reset	Description
31:16	RO	1h	**Major Version Number (MJR):** Indicates the major version is "1".
15:08	RO	2h	**Minor Version Number (MNR):** Indicates the minor version is "2".
07:00	RO	0h	Reserved

3.1.2.4 VS Value for 1.2.1 Compliant Controllers

Figure 73: VS Value for 1.2.1 Compliant Controllers

Bits	Type	Reset	Description
31:16	RO	1h	**Major Version Number (MJR):** Indicates the major version is "1".
15:08	RO	2h	**Minor Version Number (MNR):** Indicates the minor version is "2".
07:00	RO	1h	**Tertiary Version Number (TER):** Indicates the tertiary version is "1".

3.1.2.5 VS Value for 1.3 Compliant Controllers

Figure 74: VS Value for 1.3 Compliant Controllers

Bits	Type	Reset	Description
31:16	RO	1h	**Major Version Number (MJR):** Indicates the major version is “1”.
15:08	RO	3h	**Minor Version Number (MNR):** Indicates the minor version is “3”.
07:00	RO	0h	**Tertiary Version Number (TER):** Indicates the tertiary version is “0”.

3.1.2.6 VS Value for 1.4 Compliant Controllers

Figure 75: VS Value for 1.4 Compliant Controllers

Bits	Type	Reset	Description
31:16	RO	1h	**Major Version Number (MJR):** Indicates the major version is “1”.
15:08	RO	4h	**Minor Version Number (MNR):** Indicates the minor version is “4”.
07:00	RO	0h	**Tertiary Version Number (TER):** Indicates the tertiary version is “0”.

3.1.3 Offset Ch: INTMS – Interrupt Mask Set

This register is used to mask interrupts when using pin-based interrupts, single message MSI, or multiple message MSI. When using MSI-X, the interrupt mask table defined as part of MSI-X should be used to mask interrupts. Host software shall not access this register when configured for MSI-X; any accesses when configured for MSI-X is undefined. For interrupt behavior requirements, refer to section 7.5.

Figure 76: Offset Ch: INTMS – Interrupt Mask Set

Bits	Type	Reset	Description
31:00	RWS	0h	**Interrupt Vector Mask Set (IVMS):** This field is bit significant. If a ‘1’ is written to a bit, then the corresponding interrupt vector is masked from generating an interrupt or reporting a pending interrupt in the MSI Capability Structure. Writing a ‘0’ to a bit has no effect. When read, this field returns the current interrupt mask value within the controller (not the value of this register). If a bit has a value of a ‘1’, then the corresponding interrupt vector is masked. If a bit has a value of ‘0’, then the corresponding interrupt vector is not masked.

3.1.4 Offset 10h: INTMC – Interrupt Mask Clear

This register is used to unmask interrupts when using pin-based interrupts, single message MSI, or multiple message MSI. When using MSI-X, the interrupt mask table defined as part of MSI-X should be used to unmask interrupts. Host software shall not access this register when configured for MSI-X; any accesses when configured for MSI-X is undefined. For interrupt behavior requirements, refer to section 7.5.

Figure 77: Offset 10h: INTMC – Interrupt Mask Clear

Bits	Type	Reset	Description
31:00	RWC	0h	**Interrupt Vector Mask Clear (IVMC):** This field is bit significant. If a ‘1’ is written to a bit, then the corresponding interrupt vector is unmasked. Writing a ‘0’ to a bit has no effect. When read, this field returns the current interrupt mask value within the controller (not the value of this register). If a bit has a value of a ‘1’, then the corresponding interrupt vector is masked, If a bit has a value of ‘0’, then the corresponding interrupt vector is not masked.

3.1.5 Offset 14h: CC – Controller Configuration

This register modifies settings for the controller. Host software shall set the Arbitration Mechanism (CC.AMS), the Memory Page Size (CC.MPS), and the Command Set (CC.CSS) to valid values prior to enabling the controller by setting CC.EN to '1'. Attempting to create an I/O queue before initializing the I/O Completion Queue Entry Size (CC.IOCQES) and the I/O Submission Queue Entry Size (CC.IOSQES) should cause a controller to abort a Create I/O Completion Queue command or a Create I/O Submission Queue command with a status code of Invalid Queue Size.

Figure 78: Offset 14h: CC – Controller Configuration

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:24</td><td>RO</td><td>0h</td><td>Reserved</td></tr>
<tr><td>23:20</td><td>RW/RO</td><td>0h</td><td>I/O Completion Queue Entry Size (IOCQES): This field defines the I/O Completion Queue entry size that is used for the selected I/O Command Set. The required and maximum values for this field are specified in the CQES field in the Identify Controller data structure in Figure 251 for each I/O Command Set. The value is in bytes and is specified as a power of two (2^n).

If any I/O Completion Queues exist, then write operations that change the value in this field produce undefined results.

If the controller does not support I/O queues, then this field shall be read-only with a value of 0h.</td></tr>
<tr><td>19:16</td><td>RW/RO</td><td>0h</td><td>I/O Submission Queue Entry Size (IOSQES): This field defines the I/O Submission Queue entry size that is used for the selected I/O Command Set. The required and maximum values for this field are specified in the SQES field in the Identify Controller data structure in Figure 251 for each I/O Command Set. The value is in bytes and is specified as a power of two (2^n).

If any I/O Submission Queues exist, then write operations that change the value in this field produce undefined results.

If the controller does not support I/O queues, then this field shall be read-only with a value of 0h.</td></tr>
<tr><td>15:14</td><td>RW</td><td>00b</td><td>Shutdown Notification (SHN): This field is used to initiate shutdown processing when a shutdown is occurring, (i.e., a power down condition is expected). For a normal shutdown notification, it is expected that the controller is given time to process the shutdown notification. For an abrupt shutdown notification, the host may not wait for shutdown processing to complete before power is lost.

The shutdown notification values are defined as:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>No notification; no effect</td></tr>
<tr><td>01b</td><td>Normal shutdown notification</td></tr>
<tr><td>10b</td><td>Abrupt shutdown notification</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table>

This field should be written by host software prior to any power down condition and prior to any change of the PCI power management state. It is recommended that this field also be written prior to a warm reboot. To determine when shutdown processing is complete, refer to CSTS.SHST. Refer to section 7.6.2 for additional shutdown processing details.

Other fields in the CC register (including the EN bit) may be modified as part of updating this field to 01b or 10b.</td></tr>
</table>

Figure 78: Offset 14h: CC – Controller Configuration

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>13:11</td><td>RW</td><td>000b</td><td>Arbitration Mechanism Selected (AMS): This field selects the arbitration mechanism to be used. This value shall only be changed when EN is cleared to ‘0’. Host software shall only set this field to supported arbitration mechanisms indicated in CAP.AMS. If this field is set to an unsupported value, the behavior is undefined.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>Round Robin</td></tr>
<tr><td>001b</td><td>Weighted Round Robin with Urgent Priority Class</td></tr>
<tr><td>010b to 110b</td><td>Reserved</td></tr>
<tr><td>111b</td><td>Vendor Specific</td></tr>
</table></td></tr>
<tr><td>10:07</td><td>RW</td><td>0h</td><td>Memory Page Size (MPS): This field indicates the host memory page size. The memory page size is (2 ^ (12 + MPS)). Thus, the minimum host memory page size is 4 KiB and the maximum host memory page size is 128 MiB. The value set by host software shall be a supported value as indicated by the CAP.MPSMAX and CAP.MPSMIN fields. This field describes the value used for PRP entry size. This field shall only be modified when EN is cleared to ‘0’.</td></tr>
<tr><td>06:04</td><td>RW</td><td>000b</td><td>I/O Command Set Selected (CSS): This field specifies the I/O Command Set that is selected. Host software shall only select a supported I/O Command Set, as indicated in CAP.CSS. This field shall only be changed when the controller is disabled (CC.EN is cleared to ‘0’). The I/O Command Set selected shall be used for all I/O Submission Queues.

If bit 44 is set to ‘1’ in the Command Sets Supported (CSS) field, then the value 111b indicates that only the Admin Command Set is supported and that no I/O Command Set or I/O Command Set Specific Admin commands are supported. When only the Admin Command Set is supported, any command submitted on an I/O Submission Queue and any I/O Command Set Specific Admin command submitted on the Admin Submission Queue is completed with status Invalid Command Opcode. If bit 44 is cleared to ‘0’ in the Command Sets Supported (CSS) field, then the value of 111b is reserved.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>NVM Command Set</td></tr>
<tr><td>001b to 110b</td><td>Reserved</td></tr>
<tr><td>111b</td><td>Admin Command Set only</td></tr>
</table></td></tr>
<tr><td>03:01</td><td>RO</td><td>000b</td><td>Reserved</td></tr>
</table>

Figure 78: Offset 14h: CC – Controller Configuration

Bits	Type	Reset	Description
00	RW	0b	**Enable (EN):** When set to ‘1’, then the controller shall process commands based on Submission Queue Tail doorbell writes. When cleared to ‘0’, then the controller shall not process commands nor post completion queue entries to Completion Queues. When this bit transitions from ‘1’ to ‘0’, the controller is reset (i.e., a Controller Reset). That reset deletes all I/O Submission Queues and I/O Completion Queues, resets the Admin Submission Queue and Completion Queue, and brings the hardware to an idle state. That reset does not affect PCI Express registers (including MMIO MSI-X registers), nor the Admin Queue registers (AQA, ASQ, or ACQ). All other controller registers defined in this section and internal controller state (e.g., Feature values defined in section 5.21.1 that are not persistent across power states) are reset to their default values. The controller shall ensure that there is no data loss for commands that have had corresponding completion queue entries posted to an I/O Completion Queue prior to that Controller Reset. Refer to section 7.3. When this bit is cleared to ‘0’, the CSTS.RDY bit is cleared to ‘0’ by the controller once the controller is ready to be re-enabled. When this bit is set to ‘1’, the controller sets CSTS.RDY to ‘1’ when it is ready to process commands. CSTS.RDY may be set to ‘1’ before namespace(s) are ready to be accessed. Setting this bit from a ‘0’ to a ‘1’ when CSTS.RDY is a ‘1’ or clearing this bit from a '1' to a '0' when CSTS.RDY is cleared to '0' has undefined results. The Admin Queue registers (AQA, ASQ, and ACQ) shall only be modified when EN is cleared to ‘0’.

3.1.6 Offset 1Ch: CSTS – Controller Status

Figure 79: Offset 1Ch: CSTS – Controller Status

Bits	Type	Reset	Description
31:06	RO	0h	Reserved
05	RO	0b	**Processing Paused (PP):** This bit indicates whether the controller is processing commands. If this bit is cleared to ‘0’, then the controller is processing commands normally. If this bit is set to ‘1’, then the controller has temporarily stopped processing commands in order to handle an event (e.g., firmware activation). This bit is only valid when CC.EN = ‘1’.
04	RWC	HwInit	**NVM Subsystem Reset Occurred (NSSRO):** The initial value of this bit is set to '1' if the last occurrence of an NVM Subsystem Reset occurred while power was applied to the NVM subsystem. The initial value of this bit is cleared to '0' following an NVM Subsystem Reset due to application of power to the NVM subsystem. This bit is only valid if the controller supports the NVM Subsystem Reset feature defined in section 7.3.1 as indicated by CAP.NSSRS set to ‘1’. The reset value of this bit is cleared to '0' if an NVM Subsystem Reset causes activation of a new firmware image.

Figure 79: Offset 1Ch: CSTS – Controller Status

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>03:02</td><td>RO</td><td>00b</td><td>Shutdown Status (SHST): This field indicates the status of shutdown processing that is initiated by the host setting the CC.SHN field.

The shutdown status values are defined as:

<table><tr><th>Value</th><th>Definition</th></tr><tr><td>00b</td><td>Normal operation (no shutdown has been requested)</td></tr><tr><td>01b</td><td>Shutdown processing occurring</td></tr><tr><td>10b</td><td>Shutdown processing complete</td></tr><tr><td>11b</td><td>Reserved</td></tr></table>
To start executing commands on the controller after a shutdown operation (CSTS.SHST set to 10b), a Controller Reset (CC.EN cleared to ‘0’) is required. If host software submits commands to the controller without issuing a Controller Reset, the behavior is undefined.</td></tr>
<tr><td>01</td><td>RO</td><td>HwInit</td><td>Controller Fatal Status (CFS): This bit is set to ’1’ when a fatal controller error occurred that could not be communicated in the appropriate Completion Queue. This bit is cleared to ‘0’ when a fatal controller error has not occurred. Refer to section 10.5.

The reset value of this bit is set to '1' when a fatal controller error is detected during controller initialization.</td></tr>
<tr><td>00</td><td>RO</td><td>0b</td><td>Ready (RDY): This bit is set to ‘1’ when the controller is ready to accept Submission Queue Tail doorbell writes after CC.EN is set to ‘1’. This bit shall be cleared to ‘0’ when CC.EN is cleared to ‘0’ once the controller is ready to be re-enabled. Commands shall not be submitted to the controller until this bit is set to ‘1’ after the CC.EN bit is set to ‘1’. Failure to follow this requirement produces undefined results. Host software shall wait a minimum of CAP.TO seconds for this bit to be set to ‘1’ after setting CC.EN to ‘1’ from a previous value of ‘0’.</td></tr>
</table>

3.1.7 Offset 20h: NSSR – NVM Subsystem Reset

This optional register provides host software with the capability to initiate an NVM Subsystem Reset. Support for this register is indicated by the state of the NVM Subsystem Reset Supported (CAP.NSSRS) field. If the register is not supported, then the address range occupied by the register is reserved. Refer to section 7.3.1.

Figure 80: Offset 20h: NSSR – NVM Subsystem Reset

Bits	Type	Reset	Description
31:00	RW	0h	**NVM Subsystem Reset Control (NSSRC):** A write of the value 4E564D65h ("NVMe") to this field initiates an NVM Subsystem Reset. A write of any other value has no functional effect on the operation of the NVM subsystem. This field shall return the value 0h when read.

3.1.8 Offset 24h: AQA – Admin Queue Attributes

This register defines the attributes for the Admin Submission Queue and Admin Completion Queue. The Queue Identifier for the Admin Submission Queue and Admin Completion Queue is 0h. The Admin Submission Queue’s priority is determined by the arbitration mechanism selected, refer to section 4.13. The Admin Submission Queue and Admin Completion Queue are required to be in physically contiguous memory.

Note: It is recommended that UEFI be used during boot operations. In low memory environments (like Option ROMs in legacy BIOS environments) there may not be sufficient available memory to allocate the

necessary Submission and Completion Queues. In these types of conditions, low memory operation of the controller is vendor specific.

Figure 81: Offset 24h: AQA – Admin Queue Attributes

Bits	Type	Reset	Description
31:28	RO	0h	Reserved
27:16	RW	0h	**Admin Completion Queue Size (ACQS):** Defines the size of the Admin Completion Queue in entries. Refer to section 4.1.3. Enabling a controller while this field is cleared to 0h produces undefined results. The minimum size of the Admin Completion Queue is two entries. The maximum size of the Admin Completion Queue is 4,096 entries. This is a 0's based value.
15:12	RO	0h	Reserved
11:00	RW	0h	**Admin Submission Queue Size (ASQS):** Defines the size of the Admin Submission Queue in entries. Refer to section 4.1.3. Enabling a controller while this field is cleared to 0h produces undefined results. The minimum size of the Admin Submission Queue is two entries. The maximum size of the Admin Submission Queue is 4,096 entries. This is a 0's based value.

3.1.9 Offset 28h: ASQ – Admin Submission Queue Base Address

This register defines the base memory address of the Admin Submission Queue.

Figure 82: Offset 28h: ASQ – Admin Submission Queue Base Address

Bits	Type	Reset	Description
63:12	RW	Impl Spec	**Admin Submission Queue Base (ASQB):** This field specifies the 52 most significant bits of the 64-bit physical address for the Admin Submission Queue. This address shall be memory page aligned (based on the value in CC.MPS). All Admin commands, including creation of I/O Submission Queues and I/O Completions Queues shall be submitted to this queue. For the definition of Submission Queues, refer to section 4.1.
11:00	RO	0h	Reserved

3.1.10 Offset 30h: ACQ – Admin Completion Queue Base Address

This register defines the base memory address of the Admin Completion Queue.

Figure 83: Offset 30h: ACQ – Admin Completion Queue Base Address

Bit	Type	Reset	Description
63:12	RW	Impl Spec	**Admin Completion Queue Base (ACQB):** This field specifies the 52 most significant bits of the 64-bit physical address for the Admin Completion Queue. This address shall be memory page aligned (based on the value in CC.MPS). All completion queue entries for the commands submitted to the Admin Submission Queue shall be posted to this Completion Queue. This queue is always associated with interrupt vector 0. For the definition of Completion Queues, refer to section 4.1.
11:00	RO	0h	Reserved

3.1.11 Offset 38h: CMBLOC – Controller Memory Buffer Location

This optional register defines the location of the Controller Memory Buffer (refer to section 4.7). If the controller does not support the Controller Memory Buffer (CAP.CMBS), this register is reserved. If the controller supports the Controller Memory Buffer and CMBMSC.CRE is cleared to '0', this register shall be cleared to 0h.

Figure 84: Offset 38h: CMBLOC – Controller Memory Buffer Location

Bits	Type	Reset	Description
31:12	RO	Impl Spec	**Offset (OFST):** Indicates the offset of the Controller Memory Buffer in multiples of the Size Unit specified in CMBSZ.
11:09	RO	000b	Reserved
08	RO	Impl Spec	**CMB Queue Dword Alignment (CQDA):** If this bit is set to '1', CDW11.PC is set to '1'; and the address pointer specifies Controller Memory Buffer, then, the address pointer in a Create I/O Submission Queue command (refer to Figure 155) or a Create I/O Completion Queue command (refer to Figure 151) shall be Dword aligned. If this bit is cleared to '0', then the I/O Submission Queues and I/O Completion Queues contained in the Controller Memory Buffer are aligned as defined by the PRP1 field of a Create I/O Submission Queue command (refer to Figure 155) or a Create I/O Completion Queue command (refer to Figure 151).
07	RO	Impl Spec	**CMB Data Metadata Mixed Memory Support (CDMMMS):** If this bit is set to '1', then the restriction on data and metadata use of Controller Buffer Memory by a command as defined in section 4.7 is not enforced. If this bit is cleared to '0', then the restriction on data and metadata use of Controller Buffer Memory by a command as defined in section 4.7 is enforced.
06	RO	Impl Spec	**CMB Data Pointer and Command Independent Locations Support (CDPCILS):** If this bit is set to '1', then the restriction that the PRP Lists and SGLs shall not be located in the Controller Buffer Memory if the command that they are associated with is not located in the Controller Buffer Memory is not enforced (refer to section 4.7). If this bit is cleared to '0', then that restriction is enforced.
05	RO	Impl Spec	**CMB Data Pointer Mixed Locations Support (CDPMLS):** If this bit is set to '1', then the restriction that for a particular PRP List or SGL associated with a single command, all memory that is associated with that particular PRP List or SGL shall reside in either the Controller Memory Buffer or outside the Controller Memory Buffer, is not enforced (refer to section 4.7). If this bit is cleared to '0', then that restriction is enforced.
04	RO	Impl Spec	**CMB Queue Physically Discontiguous Support (CQPDS):** If this bit is set to '1', then the restriction that for all queues in the Controller Memory Buffer, the queue shall be physically contiguous, is not enforced (refer to section 4.7). If this bit is cleared to '0', then that restriction is enforced.
03	RO	Impl Spec	**CMB Queue Mixed Memory Support (CQMMS):** If this bit is set to '1', then for a particular queue placed in the Controller Memory Buffer, the restriction that all memory associated with that queue shall reside in the Controller Memory Buffer is not enforced (refer to section 4.7). If this bit is cleared to '0', then that requirement is enforced.
02:00	RO	Impl Spec	**Base Indicator Register (BIR):** Indicates the Base Address Register (BAR) that contains the Controller Memory Buffer. For a 64-bit BAR, the BAR for the lower 32-bits of the address is specified. Values 000b, 010b, 011b, 100b, and 101b are valid. The address specified by the BAR shall be 4 KiB aligned.

3.1.12 Offset 3Ch: CMBSZ – Controller Memory Buffer Size

This optional register defines the size of the Controller Memory Buffer (refer to section 4.7). If the controller does not support the Controller Memory Buffer feature or if the controller supports the Controller Memory Buffer (CAP.CMBS) and CMBMSC.CRE is cleared to '0', then this register shall be cleared to 0h.

Figure 85: Offset 3Ch: CMBSZ – Controller Memory Buffer Size

Bits	Type	Reset	Description
31:12	RO	Impl Spec	**Size (SZ):** Indicates the size of the Controller Memory Buffer available for use by the host. The size is in multiples of the Size Unit. If the Offset + Size exceeds the length of the indicated BAR, the size available to the host is limited by the length of the BAR.

Figure 85: Offset 3Ch: CMBSZ – Controller Memory Buffer Size

Bits	Type	Reset	Description
11:08	RO	Impl Spec	**Size Units (SZU):** Indicates the granularity of the Size field. 0h: 4 KiB 1h: 64 KiB 2h: 1 MiB 3h: 16 MiB 4h: 256 MiB 5h: 4 GiB 6h: 64 GiB 7h to Fh: Reserved
07:05	RO	000b	Reserved
04	RO	Impl Spec	**Write Data Support (WDS):** If this bit is set to '1', then the controller supports data and metadata in the Controller Memory Buffer for commands that transfer data from the host to the controller (e.g., Write). If this bit is cleared to '0', then data and metadata for commands that transfer data from the host to the controller shall not be transferred from the Controller Memory Buffer.
03	RO	Impl Spec	**Read Data Support (RDS):** If this bit is set to '1', then the controller supports data and metadata in the Controller Memory Buffer for commands that transfer data from the controller to the host (e.g., Read). If this bit is cleared to '0', then data and metadata for commands that transfer data from the controller to the host shall not be transferred to the Controller Memory Buffer.
02	RO	Impl Spec	**PRP SGL List Support (LISTS):** If this bit is set to '1', then the controller supports PRP Lists in the Controller Memory Buffer. If this bit is set to '1' and SGLs are supported by the controller, then the controller supports Scatter Gather Lists in the Controller Memory Buffer. If this bit is set to '1', then the Submission Queue Support bit shall be set to '1'. If this bit is cleared to '0', then PRP Lists and SGLs shall not be placed in the Controller Memory Buffer.
01	RO	Impl Spec	**Completion Queue Support (CQS):** If this bit is set to '1', then the controller supports Admin and I/O Completion Queues in the Controller Memory Buffer. If this bit is cleared to '0', then Completion Queues shall not be placed in the Controller Memory Buffer.
00	RO	Impl Spec	**Submission Queue Support (SQS):** If this bit is set to '1', then the controller supports Admin and I/O Submission Queues in the Controller Memory Buffer. If this bit is cleared to '0', then Submission Queues shall not be placed in the Controller Memory Buffer.

3.1.13 Offset 40h: BPINFO – Boot Partition Information

This optional register defines the characteristics of Boot Partitions (refer to section 8.13). If the controller does not support the Boot Partitions feature, then this register shall be cleared to 0h.

Figure 86: Offset 40h: BPINFO – Boot Partition Information

Bits	Type	Reset	Description
31	RO	Impl Spec	**Active Boot Partition ID (ABPID):** This bit indicates the identifier of the active Boot Partition.
30:26	RO	0h	Reserved

Figure 86: Offset 40h: BPINFO – Boot Partition Information

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>25:24</td><td>RO</td><td>00b</td><td>Boot Read Status (BRS): This field indicates the status of Boot Partition read operations initiated by the host writing to the BPRSEL.BPID field. Refer to section 8.13.

The boot read status values are defined as:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>No Boot Partition read operation requested</td></tr>
<tr><td>01b</td><td>Boot Partition read in progress</td></tr>
<tr><td>10b</td><td>Boot Partition read completed successfully</td></tr>
<tr><td>11b</td><td>Error completing Boot Partition read</td></tr>
</table>

If host software writes the BPRSEL.BPID field, this field transitions to 01b. After successfully completing a Boot Partition read operation (i.e., transferring the contents to the boot memory buffer), the controller sets this field to 10b. If there is an error completing a Boot Partition read operation, this field is set to 11b, and the contents of the boot memory buffer are undefined.</td></tr>
<tr><td>23:15</td><td>RO</td><td>0h</td><td>Reserved</td></tr>
<tr><td>14:00</td><td>RO</td><td>Impl Spec</td><td>Boot Partition Size (BPSZ): This field defines the size of each Boot Partition in multiples of 128 KiB. Both Boot Partitions are the same size.</td></tr>
</table>

3.1.14 Offset 44h: BPRSEL – Boot Partition Read Select

This optional register is used to initiate the transfer of a data in the Boot Partition (refer to section 8.13) from the controller to the host. If the controller does not support the Boot Partitions feature, then this register shall be cleared to 0h.

If the host attempts to read beyond the end of a Boot Partition (i.e., the Boot Partition Read Offset plus Boot Partition Read Size, is greater than the Boot Partition Size in bytes), the controller shall not transfer data and report an error in the BPINFO.BRS field.

Figure 87: Offset 44h: BPRSEL – Boot Partition Read Select

Bits	Type	Reset	Description
31	RW	0b	**Boot Partition Identifier (BPID):** This bit specifies the Boot Partition identifier for the Boot Partition read operation.
30	RO	0b	Reserved
29:10	RW	0h	**Boot Partition Read Offset (BPROF):** This field selects the offset into the Boot Partition, in 4 KiB units, that the controller copies into the Boot Partition Memory Buffer.
09:00	RW	0h	**Boot Partition Read Size (BPRSZ):** This field selects the read size in multiples of 4 KiB to copy into the Boot Partition Memory Buffer.

3.1.15 Offset 48h: BPMBL – Boot Partition Memory Buffer Location (Optional)

This optional register specifies the memory buffer that is used as the destination for data when a Boot Partition is read (refer to section 8.13). If the controller does not support the Boot Partitions feature, then this register shall be cleared to 0h.

Figure 88: Offset 48h: BPMBL – Boot Partition Memory Buffer Location (Optional)

Bits	Type	Reset	Description
63:12	RW	0h	**Boot Partition Memory Buffer Base Address (BMBBA):** This field specifies the 52 most significant bits of the 64-bit physical address for the Boot Partition Memory Buffer.
11:00	RO	0h	Reserved

3.1.16 Offset 50h: CMBMSC – Controller Memory Buffer Memory Space Control

This optional register specifies how the controller references the Controller Memory Buffer with host-supplied addresses. If the controller supports the Controller Memory Buffer (CAP.CMBS), this register is mandatory. Otherwise, this register is reserved.

This register shall be reset by neither Controller Reset nor Function Level Reset, but it shall be reset by all other Controller Level Resets.

Figure 89: Offset 50h: CMBMSC – Controller Memory Buffer Memory Space Control

Bits	Type	Reset	Description
63:12	RW	0h	**Controller Base Address (CBA):** This field specifies the 52 most significant bits of the 64-bit base address for the Controller Memory Buffer's controller address range. The Controller Memory Buffer's controller base address and its size determine its controller address range. The specified address shall be valid only under the following conditions: a) no part of the Controller Memory Buffer's controller address range is greater than $2^{64} - 1$; and b) if the Persistent Memory Region's controller memory space is enabled, then the Controller Memory Buffer's controller address range does not overlap the Persistent Memory Region's controller address range.
11:02	RO	0h	Reserved
01	RW	0b	**Controller Memory Space Enable (CMSE):** This bit specifies whether addresses supplied by the host are permitted to reference the Controller Memory Buffer. If CMBSMSC.CRE is cleared to '0' this bit has no effect, and the Controller Memory Buffer's controller memory space is not enabled. If this bit is set to '1' and the controller base address is valid, then the Controller Memory Buffer's controller memory spaced is enabled. Otherwise, the controller memory space is not enabled. If the Controller Memory Buffer's controller memory space is enabled, then addresses supplied by the host that fall within the Controller Memory Buffer's controller address range shall reference the Controller Memory Buffer. If the Controller Memory Buffer's controller memory space is not enabled, then no address supplied by the host shall reference the Controller Memory Buffer. Instead, such addresses shall reference memory spaces other than the Controller Memory Buffer.
00	RW	0b	**Capabilities Registers Enabled (CRE):** This bit specifies whether the CMBLOC and CMBSZ registers are enabled. If this bit is set to '1', then CMBLOC is defined as shown in Figure 84 and CMBSZ is defined as shown in Figure 85. If this bit is cleared to '0', then CMBSZ and CMBLOC are cleared to 0h.

3.1.17 Offset 58h: CMBSTS – Controller Memory Buffer Status

This optional register indicates the status of the Controller Memory Buffer. If the controller supports the Controller Memory Buffer (CAP.CMBS), this register is mandatory. Otherwise, this register is reserved.

Figure 90: Offset 58h: CMBSTS – Controller Memory Buffer Status

Bits	Type	Reset	Description
31:01	RO	0h	Reserved
00	RO	0b	**Controller Base Address Invalid (CBAI):** This bit indicates whether the controller has failed to enable the Controller Memory Buffer's controller memory space because CMBMSC.CBA is invalid. If CMBMSC.CRE and CMBMSC.CMSE are set to '1', and CMBMSC.CBA is invalid, this bit shall be set to '1'. Otherwise, this bit shall be cleared to '0'.

3.1.18 Offset E00h: PMRCAP – Persistent Memory Region Capabilities

This register indicates capabilities of the Persistent Memory Region. If the controller does not support the Persistent Memory Region feature, then this register shall be cleared to 0h.

Figure 91: Offset E00h: PMRCAP – Persistent Memory Region Capabilities

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:25</td><td>RO</td><td>0h</td><td>Reserved</td></tr>
<tr><td>24</td><td>RO</td><td>Impl Spec</td><td>Controller Memory Space Supported (CMSS): If set to ‘1’, this bit indicates that addresses supplied by the host are permitted to reference the Persistent Memory Region only if the host has enabled the Persistent Memory Region’s controller memory space.

If the controller supports referencing the Persistent Memory Region with host-supplied addresses, this bit shall bet set to ‘1’. Otherwise, this bit shall be cleared to ‘0’.</td></tr>
<tr><td>23:16</td><td>RO</td><td>Impl Spec</td><td>Persistent Memory Region Timeout (PMRTO): This field contains the minimum amount of time that host software should wait for the Persistent Memory Region to become ready or not ready after PMRCTL.EN is modified. The time in this field is expressed in Persistent Memory Region time units (refer to PMRCAP.PMRTU).</td></tr>
<tr><td>15:14</td><td>RO</td><td>00b</td><td>Reserved</td></tr>
<tr><td>13:10</td><td>RO</td><td>Impl Spec</td><td>Persistent Memory Region Write Barrier Mechanisms (PMRWBM): This field lists mechanisms that may be used to ensure that previous writes to the Persistent Memory Region have completed and are persistent when the Persistent Memory Region is ready and operating normally. A bit in this field is set to ‘1’ if the corresponding mechanism to ensure persistence is supported. A bit in this field is cleared to ‘0’ if the corresponding mechanism to ensure persistence is not supported.

At least one bit in this field shall be set to ‘1’.
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>0</td><td>The completion of a memory read from any Persistent Memory Region address ensures that all prior writes to the Persistent Memory Region have completed and are persistent.</td></tr>
<tr><td>1</td><td>The completion of a read to the PMRSTS register shall ensure that all prior writes to the Persistent Memory Region have completed and are persistent.</td></tr>
<tr><td>3:2</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>9:8</td><td>RO</td><td>Impl Spec</td><td>Persistent Memory Region Time Units (PMRTU): Indicates Persistent Memory Region time units.
<table>
<tr><th>Value</th><th>Persistent Memory Region Time Units</th></tr>
<tr><td>00b</td><td>500 milliseconds</td></tr>
<tr><td>01b</td><td>minutes</td></tr>
<tr><td>10b to 11b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>7:5</td><td>RO</td><td>Impl Spec</td><td>Base Indicator Register (BIR): This field indicates the Base Address Register (BAR) that specifies the address and size of the Persistent Memory Region. Values 010b, 011b, 100b, and 101b are valid.</td></tr>
<tr><td>4</td><td>RO</td><td>Impl Spec</td><td>Write Data Support (WDS): If this bit is set to ‘1’, then the controller supports data and metadata in the Persistent Memory Region for commands that transfer data from the host to the controller (e.g., Write). If this bit is cleared to ‘0’, then data and metadata for commands that transfer data from the host to the controller shall not be transferred to the Persistent Memory Region.

If PMRCAP.CMSS is cleared to ‘0’, this bit shall be cleared to ‘0’.</td></tr>
</table>

Figure 91: Offset E00h: PMRCAP – Persistent Memory Region Capabilities

Bits	Type	Reset	Description
3	RO	Impl Spec	**Read Data Support (RDS):** If this bit is set to '1', then the controller supports data and metadata in the Persistent Memory Region for commands that transfer data from the controller to the host (e.g., Read). If this bit is cleared to '0', then all data and metadata for commands that transfer data from the controller to the host shall not be transferred from the Persistent Memory Region. If PMRCAP.CMSS is cleared to '0', this bit shall be cleared to '0'.
2:0	RO	000b	Reserved

3.1.19 Offset E04h: PMRCTL – Persistent Memory Region Control

This optional register controls the operation of the Persistent Memory Region. If the controller does not support the Persistent Memory Region feature, then this register shall be cleared to 0h.

Figure 92: Offset E04h: PMRCTL – Persistent Memory Region Control

Bits	Type	Reset	Description
31:1	RO	0h	Reserved
0	RW	0b	**Enable (EN):** When set to '1', then the Persistent Memory Region is ready to process PCI Express memory read and write requests once PMRSTS.NRDY is cleared to '0'. When cleared to '0', then the Persistent Memory Region is disabled and PMRSTS.NRDY shall be set to '1' once the Persistent Memory Region is ready to be re-enabled.

3.1.20 Offset E08h: PMRSTS – Persistent Memory Region Status

This optional register provides the status of the Persistent Memory Region. If the controller does not support the Persistent Memory Region feature, then this register shall be cleared to 0h.

Figure 93: Offset E08h: PMRSTS – Persistent Memory Region Status

Bits	Type	Reset	Description
31:13	RO	0h	Reserved
12	RO	0b	**Controller Base Address Invalid (CBAI):** This field indicates whether the controller has failed to enable the Persistent Memory Region's controller memory space because the controller 64-bit base address specified by PMRMSCU.CBA and PMRMSCL.CBA is invalid. If PMRCAP.CMSS is set to '1', PMRMSCL.CMSE is set to '1', and the controller 64-bit base address specified by PMRMSCU.CBA and PMRMSCL.CBA is invalid, this bit shall be set to '1'. Otherwise, this bit shall be cleared to '0'.

Figure 93: Offset E08h: PMRSTS – Persistent Memory Region Status

<table>
<tr><th>Bits</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>11:9</td><td>RO</td><td>000b</td><td>Health Status (HSTS): If the Persistent Memory Region is ready, then this field indicates the health status of the Persistent Memory Region. This field is always cleared to 000b when the Persistent Memory Region is not ready.

The health status values are defined as:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>Normal Operation: The Persistent Memory Region is operating normally.</td></tr>
<tr><td>001b</td><td>Restore Error: The Persistent Memory Region is operating normally and is persistent; however, the contents of the Persistent Memory Region may not have been restored correctly (i.e., may not contain the contents prior to the last power cycle, NVM Subsystem Reset, Controller Level Reset, or Persistent Memory Region disable).</td></tr>
<tr><td>010b</td><td>Read Only: The Persistent Memory Region is read only. PCI Express memory write requests do not update the Persistent Memory Region. PCI Express memory read requests to the Persistent Memory Region return correct data.</td></tr>
<tr><td>011b</td><td>Unreliable: The Persistent Memory Region has become unreliable. PCI Express memory reads may return invalid data or generate poisoned PCI Express TLP(s). Persistent Memory Region memory writes may not update memory or may update memory with undefined data. The Persistent Memory Region may also have become non-persistent.</td></tr>
<tr><td>100b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>8</td><td>RO</td><td>0b</td><td>Not Ready (NRDY): This bit indicates if the Persistent Memory Region is ready for use. If this bit is cleared to ‘0’ and the PMRCTL.EN is set to ‘1’, then the Persistent Memory Region is ready to accept and process PCI Express memory read and write requests. If this bit is set to ‘1’ or the PMRCTL.EN bit is cleared to ‘0’, then the Persistent Memory Region is not ready to process PCI Express memory read and write requests.</td></tr>
<tr><td>7:0</td><td>RO</td><td>0h</td><td>Error (ERR): When the Persistent Memory Region is ready and operating normally, this field indicates whether previous memory writes to the Persistent Memory Region have completed without error. If this field is cleared to 0h, then previous writes to the Persistent Memory Region have completed without error and that the values written are persistent. A non-zero value in this field indicates the occurrence of an error that may have caused one or more of the previous writes to not have completed successfully. The meaning of any particular non-zero value is vendor specific.

Once this field takes on a non-zero value, it maintains a non-zero value until the PCI Function is reset.</td></tr>
</table>

3.1.21 Offset E0Ch: PMREBS – Persistent Memory Region Elasticity Buffer Size

This optional register identifies to the host the size of the PMR elasticity buffer. A value of 0h in this register indicates to the host that no information regarding the presence or size of a PMR elasticity buffer is available.

Figure 94: Offset E0Ch: PMREBS – Persistent Memory Region Elasticity Buffer Size

Bits	Type	Reset	Description
31:8	RO	Impl Spec	**PMR Elasticity Buffer Size Base (PMRWBZ):** Indicates the size of the PMR elasticity buffer. The actual size of the PMR elasticity buffer is equal to the value in this field multiplied by the value specified by the PMR Elasticity Buffer Size Units field.
7:5	RO	000b	Reserved

Figure 94: Offset E0Ch: PMREBS – Persistent Memory Region Elasticity Buffer Size

Bits	Type	Reset	Description
4	RO	Impl Spec	**Read Bypass Behavior:** If a memory read does not conflict with any memory write in the PMR Elasticity Buffer (i.e., if the set of memory addresses specified by a read is disjoint from the set of memory addresses specified by all writes in the PMR Elasticity Buffer), and this bit is: a) set to '1', then memory reads not conflicting with memory writes in the PMR Elasticity Buffer shall bypass those memory writes; and b) cleared to '0', then memory reads not conflicting with memory writes in the PMR Elasticity Buffer may bypass those memory writes.
3:0	RO	Impl Spec	**PMR Elasticity Buffer Size Units (PMRSZU):** Indicates the granularity of the PMR Elasticity Buffer Size field. Value: 0h – Definition: Bytes Value: 1h – Definition: 1 KiB Value: 2h – Definition: 1 MiB Value: 3h – Definition: 1 GiB Value: 4h to Fh – Definition: Reserved

3.1.22 Offset E10h: PMRSWTP – Persistent Memory Region Sustained Write Throughput

This optional register identifies to the host the maximum PMR sustained write throughput. A value of 0h in this register indicates to the host that no information regarding the PMR sustained write throughput is available.

Figure 95: Offset E10h: PMRSWTP – Persistent Memory Region Sustained Write Throughput

Bits	Type	Reset	Description
31:8	RO	Impl Spec	**PMR Sustained Write Throughput (PMRSWTV):** Indicates the sustained write throughput of the PMR at the maximum PCIe TLP payload size, as specified in the Max_Payload_Size (MPS) field of the PCI Express Device Control (PXDC) register. The actual sustained write throughput of the PMR is equal to the value in this field multiplied by the units specified by the PMR Sustained Write Throughput Units field.
7:4	RO	0h	Reserved
3:0	RO	Impl Spec	**PMR Sustained Write Throughput Units (PMRSWTU):** Indicates the granularity of the PMR Sustained Write Throughput field. Value: 0h – Definition: Bytes per second Value: 1h – Definition: 1 KiB / s Value: 2h – Definition: 1 MiB / s Value: 3h – Definition: 1 GiB / s Value: 7h to Fh – Definition: Reserved

3.1.23 Offset E14h: PMRMSCL – Persistent Memory Region Memory Space Control Lower

This optional register and the PMRMSCU register specify how the controller references the Persistent Memory Region with host-supplied addresses. If the controller supports the Persistent Memory Region's controller memory space (PMRCAP.CMSS), this register is mandatory. Otherwise, this register is reserved. The host shall access this register with aligned 32-bit accesses.

This register shall not be reset by Controller Reset.

Figure 96: Offset E14h: PMRMSCL – Persistent Memory Region Memory Space Control Lower

Bits	Type	Reset	Description
31:12	RW	0h	**Controller Base Address (CBA):** This field specifies the 20 least significant bits of the 52 most significant bits of the 64-bit base address for the Persistent Memory Region's controller address range. The Persistent Memory Region's controller base address and its size determine its controller address range. The 64-bit base address specified by this field and PMRMSCU.CBA when the CMSE bit is set to '1' shall be valid only under the following conditions: a) no part of the Persistent Memory Region's controller address range is greater than $2^{64} - 1$; and b) if the Controller Memory Buffer's controller memory space is enabled, then the Persistent Memory Region's controller address range does not overlap the Controller Memory Buffer's controller address range.
11:02	RO	0h	Reserved
01	RW	0b	**Controller Memory Space Enable (CMSE):** This bit specifies whether addresses supplied by the host are permitted to reference the Persistent Memory Region. If this bit is set to '1' and the controller base address is valid, then the Persistent Memory Region's controller memory space is enabled. Otherwise, the controller memory space is not enabled. If the Persistent Memory Region's controller memory space is enabled, then addresses supplied by the host that fall within the Persistent Memory Region's controller address range shall reference the Persistent Memory Region. If the Persistent Memory Region's controller memory space is not enabled, then no address supplied by the host shall reference the Persistent Memory Region. Instead, such addresses shall reference memory spaces other than the Persistent Memory Region.
00	RO	0b	Reserved

3.1.24 Offset E18h: PMRMSCU – Persistent Memory Region Memory Space Control Upper

This optional register and the PMRMSCL register specify how the controller references the Persistent Memory Region with host-supplied addresses. If the controller supports the Persistent Memory Region's controller memory space (PMRCAP.CMSS), this register is mandatory. Otherwise, this register is reserved. The host shall access this register with aligned 32-bit accesses.

This register shall not be reset by Controller Reset.

Figure 97: Offset E18h: PMRMSCU – Persistent Memory Region Memory Space Control Upper

Bits	Type	Reset	Description
31:00	RW	0h	**Controller Base Address (CBA):** This field specifies the 32 most significant bits of the 52 most significant bits of the 64-bit base address for the Persistent Memory Region's controller address range. The Persistent Memory Region's controller base address and its size determine its controller address range.

3.1.25 Offset (1000h + ((2y) * (4 << CAP.DSTRD))): SQyTDBL – Submission Queue y Tail Doorbell

This register defines the doorbell register that updates the Tail entry pointer for Submission Queue y. The value of y is equivalent to the Queue Identifier. This indicates to the controller that new commands have been submitted for processing.

The host should not read the doorbell registers. If a doorbell register is read, the value returned is vendor specific. Writing to a non-existent Submission Queue Tail Doorbell has undefined results.

Figure 98: Offset (1000h + ((2y) * (4 << CAP.DSTRD))): SQyTDBL – Submission Queue y Tail Doorbell

Bits	Type	Reset	Description
31:16	RO	0h	Reserved
15:00	RW	0h	**Submission Queue Tail (SQT):** Indicates the new value of the Submission Queue Tail entry pointer. This value shall overwrite any previous Submission Queue Tail entry pointer value provided. The difference between the last SQT write and the current SQT write indicates the number of commands added to the Submission Queue. Note: Submission Queue rollover needs to be accounted for.

3.1.26 Offset (1000h + ((2y + 1) * (4 << CAP.DSTRD))): CQyHDBL – Completion Queue y Head Doorbell

This register defines the doorbell register that updates the Head entry pointer for Completion Queue y. The value of y is equivalent to the Queue Identifier. This indicates Completion Queue entries that have been processed by host software.

The host should not read the doorbell registers. If a doorbell register is read, the value returned is vendor specific. Writing to a non-existent Completion Queue Head Doorbell has undefined results.

Host software should ensure it continues to process completion queue entries within Completion Queues regardless of whether there are entries available in a particular or any Submission Queue.

Figure 99: Offset (1000h + ((2y + 1) * (4 << CAP.DSTRD))): CQyHDBL – Completion Queue y Head Doorbell

Bits	Type	Reset	Description
31:16	RO	0h	Reserved
15:00	RW	0h	**Completion Queue Head (CQH):** Indicates the new value of the Completion Queue Head entry pointer. This value shall overwrite any previous Completion Queue Head value provided. The difference between the last CQH write and the current CQH entry pointer write indicates the number of entries that are now available for re-use by the controller in the Completion Queue. Note: Completion Queue rollover needs to be accounted for.

3.2 Index/Data Pair registers (Optional)

Index/Data Pair registers provide host software with a mechanism to access the NVM Express memory mapped registers using I/O space based registers. If supported, these registers are located in BAR2. On PC based platforms, host software (BIOS, Option ROMs, OSes) written to operate in 'real-mode' (8086 mode) are unable to access registers in a PCI Express function's address space, if the address space is memory mapped and mapped above 1 MiB.

The Index/Data Pair mechanism allows host software to access all of the memory mapped NVM Express registers using indirect I/O addressing in lieu of direct memory mapped access.

Note: UEFI drivers do not encounter the 1 MiB limitation, and thus when using EFI there is no requirement for the Index/Data Pair mechanism. Thus, this feature is optional for the controller to support and may be obsoleted as UEFI becomes pervasive.

3.2.1 Restrictions

Host software shall not alternate between Index/Data Pair based access and direct memory mapped access methods. After using direct memory mapped access to the controller registers, the Index/Data Pair mechanism shall not be used.

3.2.2 Register Definition

The following registers describe the registers necessary to implement Index/Data Pair.

Figure 100: Register Definition

Start	End	Symbol	Description
0h	3h	IDX	Index register
4h	7h	DAT	Data register

3.2.3 Offset 0h: IDX – Index Register

Figure 101: Offset 0h: IDX – Index Register

Bit	Type	Reset	Description
31:02	RW	0h	**Index (IDX):** This register selects the dword offset of the memory mapped NVM Express register to be accessed within the MLBAR/MUBAR registers (PCI BAR0 and BAR1). Host software shall not set this to a value beyond the maximum register offset implemented.
01:00	RO	00b	Reserved

3.2.4 Offset 4h: DAT – Data Register

Figure 102: Offset 4h: DAT – Data Register

Bits	Type	Reset	Description
31:00	RW	n/a	**Data (DAT):** This register is a “window” through which data is read or written to the memory mapped register pointed to by the Index register. A physical register is not implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the reset value is the same as the reset value of the register that the Index register is currently pointing to.

4 Data Structures

This section describes data structures used by the NVM Express.

4.1 Submission Queue & Completion Queue Definition

Sections 4.1, 4.1.1, and 4.1.2 apply to NVMe over PCIe implementations only. For NVMe over Fabrics implementations, refer to section 2.4 and the subsections of that section in the NVMe over Fabrics specification.

The submitter of entries to a queue uses the current Tail entry pointer to identify the next open queue slot. The submitter increments the Tail entry pointer after placing the new entry to the open queue slot. If the Tail entry pointer increment exceeds the queue size, the Tail entry shall roll to zero. The submitter may continue to place entries in free queue slots as long as the Full queue condition is not met (refer to section 4.1.2).

Note: The submitter shall take queue wrap conditions into account.

The consumer of entries on a queue uses the current Head entry pointer to identify the slot containing the next entry to be consumed. The consumer increments the Head entry pointer after consuming the next entry from the queue. If the Head entry pointer increment exceeds the queue size, the Head entry pointer shall roll to zero. The consumer may continue to consume entries from the queue as long as the Empty queue condition is not met (refer to section 4.1.1).

Note: The consumer shall take queue wrap conditions into account.

Creation and deletion of Submission Queue and associated Completion Queues are required to be ordered correctly by host software. Host software shall create the Completion Queue before creating any associated Submission Queue. Submission Queues may be created at any time after the associated Completion Queue is created. Host software shall delete all associated Submission Queues prior to deleting a Completion Queue. To abort all commands submitted to the Submission Queue host software should issue a Delete I/O Submission Queue command for that queue (refer to section 7.4.3).

Host software writes the Submission Queue Tail Doorbell (refer to section 3.1.25) and the Completion Queue Head Doorbell (refer to section 3.1.26) to communicate new values of the corresponding entry pointers to the controller. If host software writes an invalid value to the Submission Queue Tail Doorbell or Completion Queue Head Doorbell register and an Asynchronous Event Request command is outstanding, then an asynchronous event is posted to the Admin Completion Queue with a status code of Invalid Doorbell Write Value. The associated queue should be deleted and recreated by host software. For a Submission Queue that experiences this error, the controller may complete previously consumed commands; no additional commands are consumed. This condition may be caused by host software attempting to add an entry to a full Submission Queue or remove an entry from an empty Completion Queue.

Host software checks Completion Queue entry Phase Tag (P) bits in memory to determine whether new Completion Queue entries have been posted. The Completion Queue Tail pointer is only used internally by the controller and is not visible to the host. The controller uses the SQ Head Pointer (SQHD) field in Completion Queue entries to communicate new values of the Submission Queue Head Pointer to the host. A new SQHD value indicates that Submission Queue entries have been consumed, but does not indicate either execution or completion of any command. Refer to section 4.6.

A Submission Queue entry is submitted to the controller when the host writes the associated Submission Queue Tail Doorbell with a new value that indicates that the Submission Queue Tail Pointer has moved to or past the slot in which that Submission Queue entry was placed. A Submission Queue Tail Doorbell write may indicate that one or more Submission Queue entries have been submitted.

A Submission Queue entry has been consumed by the controller when a Completion Queue entry is posted that indicates that the Submission Queue Head Pointer has moved past the slot in which that Submission Queue entry was placed. A Completion Queue entry may indicate that one or more Submission Queue entries have been consumed.

A Completion Queue entry is posted to the Completion Queue when the controller write of that Completion Queue entry to the next free Completion Queue slot inverts the Phase Tag (P) bit from its previous value in memory. The controller may generate an interrupt to the host to indicate that one or more Completion Queue entries have been posted.

A Completion Queue entry has been consumed by the host when the host writes the associated Completion Queue Head Doorbell with a new value that indicates that the Completion Queue Head Pointer has moved past the slot in which that Completion Queue entry was placed. A Completion Queue Head Doorbell write may indicate that one or more Completion Queue entries have been consumed.

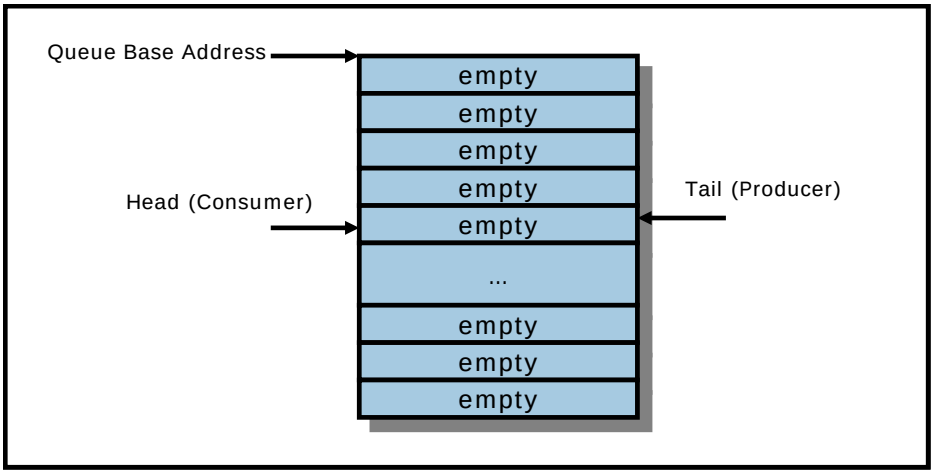
Once a Submission Queue or Completion Queue entry has been consumed, the slot in which it was placed is free and available for reuse. Altering a Submission Queue entry after that entry has been submitted but before that entry has been consumed results in undefined behavior. Altering a Completion Queue entry after that entry has been posted but before that entry has been consumed results in undefined behavior.

If there are no free slots in a Completion Queue, then the controller shall not post status to that Completion Queue until slots become available. In this case, the controller may stop processing additional Submission Queue entries associated with the affected Completion Queue until slots become available. The controller shall continue processing for other queues.

4.1.1 Empty Queue

The queue is Empty when the Head entry pointer equals the Tail entry pointer. Figure 103 defines the Empty Queue condition.

Figure 103: Empty Queue Definition

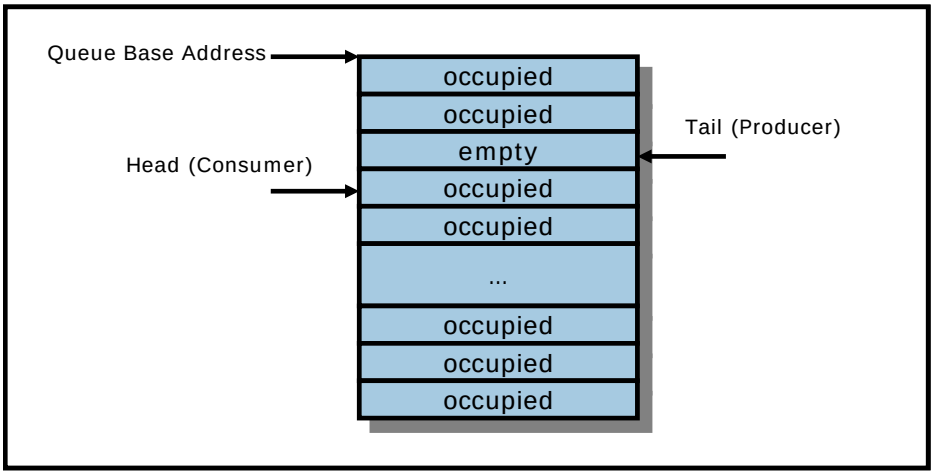


4.1.2 Full Queue

The queue is Full when the Head equals one more than the Tail. The number of entries in a queue when full is one less than the queue size. Figure 104 defines the Full Queue condition.

Note: Queue wrap conditions shall be taken into account when determining whether a queue is Full.

Figure 104: Full Queue Definition



4.1.3 Queue Size

The Queue Size is indicated in a 16-bit 0's based field that indicates the number of slots in the queue. The minimum size for a queue is two slots. The maximum size for either an I/O Submission Queue or an I/O Completion Queue is defined as 64 Ki slots, limited by the maximum queue size supported by the controller that is reported in the CAP.MQES field. The maximum size for the Admin Submission and Admin Completion Queue is defined as 4 Ki slots. One slot in each queue is not available for use due to Head and Tail entry pointer definition.

4.1.4 Queue Identifier

Each queue is identified through a 16-bit ID value that is assigned to the queue when it is created.

4.1.5 Queue Priority

If the weighted round robin with urgent priority class arbitration mechanism is supported, then host software may assign a queue priority service class of Urgent, High, Medium, or Low. If the weighted round robin with urgent priority class arbitration mechanism is not supported, then the priority setting is not used and is ignored by the controller.

4.2 Submission Queue Entry – Command Format

Each command is 64 bytes in size.

Command Dword 0, Namespace Identifier, Metadata Pointer, PRP Entry 1, PRP Entry 2, SGL Entry 1, and Metadata SGL Segment Pointer have common definitions for all Admin commands and NVM commands. Metadata Pointer, PRP Entry 1, PRP Entry 2, and Metadata SGL Segment Pointer are not used by all commands. Command Dword 0 is defined in Figure 105.

Figure 105: Command Dword 0

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:16</td><td>Command Identifier (CID): This field specifies a unique identifier for the command when combined with the Submission Queue identifier.

The value of FFFFh should not be used as the Error Information log page (refer to section 5.14.1.1) uses this value to indicate an error is not associated with a particular command.</td></tr>
<tr><td>15:14</td><td>PRP or SGL for Data Transfer (PSDT): This field specifies whether PRPs or SGLs are used for any data transfer associated with the command. PRPs shall be used for all Admin commands for NVMe over PCIe implementations. SGLs shall be used for all Admin and I/O commands for NVMe over Fabrics implementations (i.e., this field set to 01b). The definition is described in the table below.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>PRPs are used for this transfer.</td></tr>
<tr><td>01b</td><td>SGLs are used for this transfer. If used, Metadata Pointer (MPTR) contains an address of a single contiguous physical buffer that is byte aligned.</td></tr>
<tr><td>10b</td><td>SGLs are used for this transfer. If used, Metadata Pointer (MPTR) contains an address of an SGL segment containing exactly one SGL Descriptor that is qword aligned.</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table>

If there is metadata that is not interleaved with the logical block data, as specified in the Format NVM command, then the Metadata Pointer (MPTR) field is used to point to the metadata. The definition of the Metadata Pointer field is dependent on the setting in this field. Refer to Figure 106.</td></tr>
<tr><td>13:10</td><td>Reserved</td></tr>
<tr><td>09:08</td><td>Fused Operation (FUSE): In a fused operation, a complex command is created by “fusing” together two simpler commands. Refer to section 4.12. This field specifies whether this command is part of a fused operation and if so, which command it is in the sequence.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>Normal operation</td></tr>
<tr><td>01b</td><td>Fused operation, first command</td></tr>
<tr><td>10b</td><td>Fused operation, second command</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>07:00</td><td>Opcode (OPC): This field specifies the opcode of the command to be executed.</td></tr>
</table>

The 64 byte command format for the Admin Command Set and NVM Command Set is defined in Figure 106. Any additional I/O Command Set defined in the future may use an alternate command size or format.

SGLs shall not be used for Admin commands in NVMe over PCIe implementations.

Figure 106: Command Format – Admin and NVM Command Set

Bytes	Description
03:00	**Command Dword 0 (CDW0):** This field is common to all commands and is defined in Figure 105.

Figure 106: Command Format – Admin and NVM Command Set

Bytes	Description
07:04	**Namespace Identifier (NSID):** This field specifies the namespace that this command applies to. If the namespace identifier is not used for the command, then this field shall be cleared to 0h. The value FFFFFFFFh in this field is a broadcast value (refer to section 6.1), where the scope (e.g., the NVM subsystem, all attached namespaces, or all namespaces in the NVM subsystem) is dependent on the command. Refer to Figure 141, Figure 142, and Figure 350 for commands that support the use of the value FFFFFFFFh in this field. Specifying an inactive namespace identifier (refer to section 6.1.4) in a command that uses the namespace identifier shall cause the controller to abort the command with status Invalid Field in Command, unless otherwise specified. Specifying an invalid namespace identifier (refer to section 6.1.2) in a command that uses the namespace identifier shall cause the controller to abort the command with status Invalid Namespace or Format, unless otherwise specified. If the namespace identifier is used for the command (refer to Figure 141 and Figure 142), the value FFFFFFFFh is not supported for that command, and the host specifies a value of FFFFFFFFh, then the controller should abort the command with status Invalid Field in Command, unless otherwise specified. If the namespace identifier is not used for the command and the host specifies a value from 1h to FFFFFFFFh, then the controller should abort the command with status Invalid Field in Command, unless otherwise specified.
15:08	Reserved
23:16	**Metadata Pointer (MPTR):** This field is valid only if the command has metadata that is not interleaved with the logical block data, as specified in the Format NVM command. This is a reserved field in NVMe over Fabrics implementations. If CDW0.PSDT (refer to Figure 105) is cleared to 00b, then this field shall contain the address of a contiguous physical buffer of metadata and that address shall be dword aligned (i.e., bits 1:0 cleared to 00b). The controller is not required to check that bits 1:0 are cleared to 00b. The controller may report an error of Invalid Field in Command if bits 1:0 are not cleared to 00b. If the controller does not report an error of Invalid Field in Command, then the controller shall operate as if bits 1:0 are cleared to 00b. If CDW0.PSDT is set to 01b, then this field shall contain the address of a contiguous physical buffer of metadata. Refer to bit 17 of the SGLS field in the Identify Controller data structure for alignment requirements. If CDW0.PSDT is set to 10b, then this field shall contain the address of an SGL segment that contains exactly one SGL Descriptor. The address of that SGL segment shall be qword aligned (i.e., bits 2:0 cleared to 000b). The SGL Descriptor contained in that SGL segment is the first SGL Descriptor of the metadata for the command. If the SGL Descriptor contained in that SGL segment is an SGL Data Block descriptor, then that SGL Data Block Descriptor is the only SGL Descriptor and therefore describes the entire metadata data transfer. Refer to section 4.4. The controller is not required to check that bits 2:0 are cleared to 000b. The controller may report an error of Invalid Field in Command if bits 2:0 are not cleared to 000b. If the controller does not report an error of Invalid Field in Command, then the controller shall operate as if bits 2:0 are cleared to 000b.

Figure 106: Command Format – Admin and NVM Command Set

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>39:24</td><td>
Data Pointer (DPTR): This field specifies the data used in the command.

If CDW0.PSDT is cleared to 00b, then the definition of this field is:

<table>
<tr><td>39:32</td><td>PRP Entry 2 (PRP2): This field:
a) is reserved if the data transfer does not cross a memory page boundary;
b) specifies the Page Base Address of the second memory page if the data transfer crosses exactly one memory page boundary. E.g.,:
i. the command data transfer length is equal in size to one memory page and the offset portion of the PBAO field of PRP1 is non-zero; or
ii. the Offset portion of the PBAO field of PRP1 is equal to 0h and the command data transfer length is greater than one memory page and less than or equal to two memory pages in size;
and
c) is a PRP List pointer if the data transfer crosses more than one memory page boundary. E.g.,:
i. the command data transfer length is greater than or equal to two memory pages in size but the offset portion of the PBAO field of PRP1 is non-zero; or
ii. the command data transfer length is equal in size to more than two memory pages and the Offset portion of the PBAO field of PRP1 is equal to 0h.</td></tr>
<tr><td>31:24</td><td>PRP Entry 1 (PRP1): This field contains the first PRP entry for the command or a PRP List pointer depending on the command.</td></tr>
</table>

If CDW0.PSDT is set to 01b or 10b, then the definition of this field is:

<table>
<tr><td>39:24</td><td>SGL Entry 1 (SGL1): This field contains the first SGL segment for the command. If the SGL segment is an SGL Data Block or Keyed SGL Data Block or Transport SGL Data Block descriptor, then it describes the entire data transfer. If more than one SGL segment is needed to describe the data transfer, then the first SGL segment is a Segment, or Last Segment descriptor. Refer to section 4.4 for the definition of SGL segments and descriptor types.

The NVMe Transport may support a subset of SGL Descriptor types and features as defined in the NVMe Transport binding specification.</td></tr>
</table>
</td></tr>
<tr><td>43:40</td><td>Command Dword 10 (CDW10): This field is command specific Dword 10.</td></tr>
<tr><td>47:44</td><td>Command Dword 11 (CDW11): This field is command specific Dword 11.</td></tr>
<tr><td>51:48</td><td>Command Dword 12 (CDW12): This field is command specific Dword 12.</td></tr>
<tr><td>55:52</td><td>Command Dword 13 (CDW13): This field is command specific Dword 13.</td></tr>
<tr><td>59:56</td><td>Command Dword 14 (CDW14): This field is command specific Dword 14.</td></tr>
<tr><td>63:60</td><td>Command Dword 15 (CDW15): This field is command specific Dword 15.</td></tr>
</table>

In addition to the fields commonly defined for all Admin and NVM commands, Admin and NVM Vendor Specific commands may support the Number of Dwords in Data Transfer and Number of Dwords in Metadata Transfer fields. If supported, the command format for the Admin Vendor Specific Command and NVM Vendor Specific Commands are defined in Figure 107. For more details, refer to section 8.7.

Figure 107: Command Format – Admin and NVM Vendor Specific Commands (Optional)

Bytes	Description
03:00	**Command Dword 0 (CDW0):** This field is common to all commands and is defined in Figure 105.

Figure 107: Command Format – Admin and NVM Vendor Specific Commands (Optional)

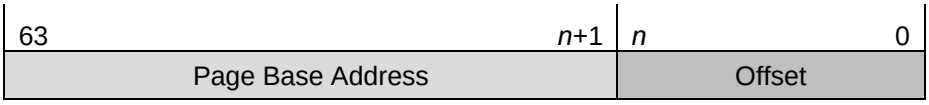
Bytes	Description
07:04	**Namespace Identifier (NSID):** This field indicates the namespace ID that this command applies to. If the namespace ID is not used for the command, then this field shall be cleared to 0h. Setting this value to FFFFFFFFh causes the command to be applied to all namespaces attached to the controller processing the command, unless otherwise specified. The behavior of a controller in response to an inactive namespace ID for a vendor specific command is vendor specific. Specifying an invalid namespace ID in a command that uses the namespace ID shall cause the controller to abort the command with status Invalid Namespace or Format, unless otherwise specified.
15:08	Reserved
39:16	Refer to Figure 106 for the definition of these fields.
43:40	**Number of Dwords in Data Transfer (NDT):** This field indicates the number of dwords in the data transfer.
47:44	**Number of Dwords in Metadata Transfer (NDM):** This field indicates the number of dwords in the metadata transfer.
51:48	**Command Dword 12 (CDW12):** This field is command specific Dword 12.
55:52	**Command Dword 13 (CDW13):** This field is command specific Dword 13.
59:56	**Command Dword 14 (CDW14):** This field is command specific Dword 14.
63:60	**Command Dword 15 (CDW15):** This field is command specific Dword 15.

4.3 Physical Region Page Entry and List

A physical region page (PRP) entry is a pointer to a physical memory page. PRPs are used as a scatter/gather mechanism for data transfers between the controller and memory. To enable efficient out of order data transfers between the controller and the host, PRP entries are a fixed size.

The size of the physical memory page is configured by host software in CC.MPS. Figure 108 shows the layout of a PRP entry that consists of a Page Base Address and an Offset. The size of the Offset field is determined by the physical memory page size configured in CC.MPS.

Figure 108: PRP Entry Layout



The definition of a PRP entry is described in Figure 109.

Figure 109: PRP Entry – Page Base Address and Offset

Bits	Description
63:00	**Page Base Address and Offset (PBAO):** This field indicates the 64-bit physical memory page address. The lower bits (*n*:0) of this field indicate the offset within the memory page (e.g., if the memory page size is 4 KiB, then bits 11:00 form the Offset; if the memory page size is 8 KiB, then bits 12:00 form the Offset). If this entry is not the first PRP entry in the command or a PRP List pointer in a command, then the Offset portion of this field shall be cleared to 0h. The Offset shall be dword aligned, indicated by bits 1:0 being cleared to 00b. Note: The controller is not required to check that bits 1:0 are cleared to 00b. The controller may report an error of PRP Offset Invalid if bits 1:0 are not cleared to 00b. If the controller does not report an error of PRP Offset Invalid, then the controller shall operate as if bits 1:0 are cleared to 00b.

A physical region page list (PRP List) is a set of PRP entries in a single page of contiguous memory. A PRP List describes additional PRP entries that could not be described within the command itself. Any PRP entries described within the command are not duplicated in a PRP List. If the amount of data to transfer requires multiple PRP List memory pages, then the last PRP entry before the end of the memory page shall be a pointer to the next PRP List, indicating the next segment of the PRP List. Figure 110 shows the layout of a PRP List where each PRP entry identifies memory pages that are physically contiguous. Figure 111 shows the layout of a PRP List where each PRP entry identifies a different memory page (i.e., the memory pages are not physically contiguous).

Figure 110: PRP List Layout for Physically Contiguous Memory Pages

63 ***n*+1**	***n*** **0**
Page Base Address *p*	0h
Page Base Address *p*+1	0h
…	
Page Base Address *p*+*q*	0h
Page Base Address *p*+*q*+1	0h

Figure 111: PRP List Layout for Physically Non-Contiguous Memory Pages

63 ***n*+1**	***n*** **0**
Page Base Address *p*	0h
Page Base Address *q*	0h
…	
Page Base Address *r*	0h
Page Base Address *s*	0h

Dependent on the command definition, the first PRP entry contained within the command may have a non-zero offset within the memory page. The first PRP List entry (i.e., the first pointer to a memory page containing additional PRP entries) that if present is typically contained in the PRP Entry 2 location within the command, shall be qword aligned and may also have a non-zero offset within the memory page.

PRP entries contained within a PRP List shall have a memory page offset of 0h. If a second PRP entry is present within a command, it shall have a memory page offset of 0h. In both cases, the entries are memory page aligned based on the value in CC.MPS. If the controller receives a non-zero offset for these PRP entries the controller should return an error of PRP Offset Invalid.

PRP Lists shall be minimally sized with packed entries starting with entry 0. If more PRP List pages are required, then the last entry of the PRP List contains the Page Base Address of the next PRP List page. The next PRP List page shall be memory page aligned. The total number of PRP entries required by a command is implied by the command parameters and memory page size.

4.4 Scatter Gather List (SGL)

A Scatter Gather List (SGL) is a data structure in memory address space used to describe a data buffer. The controller indicates the SGL types that the controller supports in the Identify Controller data structure. A data buffer is either a source buffer or a destination buffer. An SGL contains one or more SGL segments. The total length of the Data Block and Bit Bucket descriptors in an SGL shall be equal to or exceed the amount of data requested to be transferred.

An SGL segment is a qword aligned data structure in a contiguous region of physical memory describing all, part of, or none of a data buffer and the next SGL segment, if any. An SGL segment consists of an array

of one or more SGL descriptors. Only the last descriptor in an SGL segment may be an SGL Segment descriptor or an SGL Last Segment descriptor.

A last SGL segment is an SGL segment that does not contain an SGL Segment descriptor, or an SGL Last Segment descriptor.

A controller may support byte or dword alignment and granularity of Data Blocks. If a controller supports only dword alignment and granularity as indicated in the SGL Support field of the Identify Controller data structure (refer to Figure 251), then the values in the Address and Length fields of all Data Block descriptors shall have their lower two bits cleared to 00b. This requirement applies to Data Block descriptors that indicate data and/or metadata memory regions.

A Keyed SGL Data Block descriptor is a Data Block descriptor that includes a key that is used as part of the host memory access. The maximum length that may be specified in a Keyed SGL Data Block descriptor is (16 MiB – 1).

A Transport SGL Data Block descriptor is a Data Block descriptor that specifies a data block that is transferred by the NVMe Transport using a transfer mechanism and data buffers that are specific to the NVMe Transport.

The SGL Identifier Descriptor Sub Type field may indicate additional information about a descriptor. As an example, the Sub Type may indicate that the Address field is an offset rather than an absolute address. The Sub Type may also indicate NVMe Transport specific information.

The controller shall abort a command if:

- an SGL segment contains an SGL Segment descriptor or an SGL Last Segment descriptor in other than the last descriptor in the segment;
- a last SGL segment contains an SGL Segment descriptor, or an SGL Last Segment descriptor;
- an SGL descriptor has an unsupported format; or
- an SGL Data Block descriptor contains Address or Length fields with either of the two lower bits set to 1b and the controller supports only dword alignment and granularity as indicated in the SGL Support field of the Identify Controller data structure. Refer to Figure 251.

Figure 112 defines the SGL segment.

Figure 112: SGL Segment

Bytes	Description
15:00	SGL Descriptor 0
31:16	SGL Descriptor 1
…	…
((n*16)+15):(n*16)	SGL Descriptor n

An SGL segment contains one or more SGL descriptors. Figure 113 defines the generic SGL descriptor format.

Figure 113: Generic SGL Descriptor Format

Bytes	Description
14:00	**Descriptor Type Specific**
15	**SGL Identifier: The definition of this field is described in the table below.** **Bits** / **Description** 03:00 – SGL Descriptor Sub Type (refer to Figure 115) 07:04 – SGL Descriptor Type (refer to Figure 114)

The SGL Descriptor Type field defined in Figure 114 specifies the SGL descriptor type. If the SGL Descriptor Type field is set to a reserved value or an unsupported value, then the SGL descriptor shall be processed as having an SGL Descriptor Type error. If the SGL Descriptor Sub Type field is set to a reserved value or an unsupported value, then the descriptor shall be processed as having an SGL Descriptor Type error.

An SGL descriptor set to all zeroes is an SGL Data Block descriptor with the Address field cleared to 0h and the Length field cleared to 0h may be used as a NULL descriptor.

Figure 114: SGL Descriptor Type

Code	Descriptor
0h	SGL Data Block descriptor
1h	SGL Bit Bucket descriptor
2h	SGL Segment descriptor
3h	SGL Last Segment descriptor
4h	Keyed SGL Data Block descriptor
5h	Transport SGL Data Block descriptor
6h to Eh	Reserved
Fh	Vendor specific

Figure 115 defines the SGL Descriptor Sub Type values and indicates the SGL Descriptor Types to which each SGL Descriptor Sub Type applies.

Figure 115: SGL Descriptor Sub Type Values

SGL Descriptor Sub Type	SGL Descriptor Types	Sub Type Description
0h	0h, 2h, 3h, 4h	**Address:** The Address field specifies the starting 64-bit memory byte address of the Data Block, Segment, or Last Segment descriptor.
	1h	For Type 1h, the Sub Type field shall be cleared to 0h.
	All others	Reserved
1h	0h, 2h, 3h	**Offset**: The Address field contains an offset from the beginning of the location where data may be transferred. For NVMe over PCIe implementations, this Sub Type is reserved. For NVMe over Fabrics implementations, refer to the NVMe over Fabrics specification for details on the location from which the offset is specified.
	1h	The controller shall abort the command with the status of SGL Descriptor Type Invalid.
	4h	The controller shall abort the command with the status of SGL Descriptor Type Invalid.
	All others	Reserved
Ah to Fh	All	**NVMe Transport Specific:** The definitions for this range of Sub Types are defined by the binding section for the associated NVMe Transport.
All others	All	Reserved

The SGL Data Block descriptor, defined in Figure 116, describes a data block.

Figure 116: SGL Data Block descriptor

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>07:00</td><td>Address: If the SGL Identifier Descriptor Sub Type field is cleared to 0h, then the Address field specifies the starting 64-bit memory byte address of the data block. If the SGL Identifier Descriptor Sub Type field is set to 1h, then the Address field contains an offset from the beginning of the location where data may be transferred. If the controller requires dword alignment and granularity as indicated in the SGL Support (SGLS) field of the Identify Controller data structure (refer to Figure 251), then the lower two bits shall be cleared to 00b.

If dword alignment and granularity is required, the controller may report an error of Invalid Field in Command if bits 1:0 are not cleared to 00b. If the controller does not report an error of Invalid Field in Command, then the controller shall operate as if bits 1:0 are cleared to 00b.</td></tr>
<tr><td>11:08</td><td>Length: The Length field specifies the length in bytes of the data block. A Length field cleared to 0h specifies that no data is transferred. An SGL Data Block descriptor specifying that no data is transferred is a valid SGL Data Block descriptor. If the controller requires dword alignment and granularity as specified in the SGL Support (SGLS) field the of Identify Controller data structure, then the lower two bits shall be cleared to 00b.

If dword alignment and granularity is required, the controller may report an error of Invalid Field in Command if bits 1:0 are not cleared to 00b. If the controller does not report an error of Invalid Field in Command, then the controller shall operate as if bits 1:0 are cleared to 00b.

If the value in the Address field plus the value in the Length field is greater than 1_00000000_00000000h, then the SGL Data Block descriptor shall be processed as having a Data SGL Length Invalid or Metadata SGL Length Invalid error.</td></tr>
<tr><td>14:12</td><td>Reserved</td></tr>
<tr><td>15</td><td>SGL Identifier: The definition of this field is described in the table below.

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>03:00</td><td>SGL Descriptor Sub Type: Valid values are specified in Figure 115.</td></tr>
<tr><td>07:04</td><td>SGL Descriptor Type: 0h as specified in Figure 114.</td></tr>
</table>
</td></tr>
</table>

The SGL Bit Bucket descriptor, defined in Figure 117, is used to ignore parts of source data.

Figure 117: SGL Bit Bucket descriptor

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>07:00</td><td>Reserved</td></tr>
<tr><td>11:08</td><td>Length: The Length field specifies the amount of source data that is discarded. An SGL Bit Bucket descriptor specifying that no source data be discarded (i.e., the length field cleared to 0h) is a valid SGL Bit Bucket descriptor.

If the SGL Bit Bucket descriptor describes a destination data buffer (e.g., a read from the controller to host memory), then the Length field specifies the number of bytes of the source data which the controller shall discard (i.e., not transfer to the destination data buffer).

If the SGL Bit Bucket descriptor describes a source data buffer (e.g., a write from host memory to the controller), then the Bit Bucket Descriptor shall be treated as if the Length field were cleared to 0h (i.e., the Bit Bucket Descriptor has no effect).

If SGL Bit Bucket descriptors are supported, their length in a destination data buffer shall be included in the specified length of data to be transferred (e.g., their length in a source data buffer is not included in the NLB parameter).</td></tr>
<tr><td>14:12</td><td>Reserved</td></tr>
<tr><td>15</td><td>SGL Identifier: The definition of this field is described in the table below.

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>03:00</td><td>SGL Descriptor Sub Type: Valid values are specified in Figure 115.</td></tr>
<tr><td>07:04</td><td>SGL Descriptor Type: 1h as specified in Figure 114.</td></tr>
</table>
</td></tr>
</table>

The SGL Segment descriptor, defined in Figure 118, describes the next SGL segment, which is not the last SGL segment.

Figure 118: SGL Segment descriptor

Bytes	Description
07:00	**Address:** If the SGL Identifier Descriptor Sub Type field is cleared to 0h, then the Address field specifies the starting 64-bit memory byte address of the next SGL segment, which is a SGL segment. If the SGL Identifier Descriptor Sub Type field is set to 1h, then the Address field contains an offset from the beginning of the location where data may be transferred.
11:08	**Length:** The Length field specifies the length in bytes of the next SGL segment. The Length field shall be a non-zero value and a multiple of 16. If the value in the Address field plus the value in the Length field is greater than 1_00000000_00000000h, then the SGL Segment descriptor shall be processed as having a Data SGL Length Invalid or Metadata SGL Length Invalid error.
14:12	Reserved
15	**SGL Identifier:** The definition of this field is described in the table below. **Bits** / **Description** 03:00 — **SGL Descriptor Sub Type:** Valid values are specified in Figure 115. 07:04 — **SGL Descriptor Type:** 2h as specified in Figure 114.

The SGL Last Segment descriptor, defined in Figure 119, describes the next and last SGL segment. A last SGL segment that contains an SGL Segment descriptor or an SGL Last Segment descriptor is processed as an error.

Figure 119: SGL Last Segment descriptor

Bytes	Description
07:00	**Address:** If the SGL Identifier Descriptor Sub Type field is cleared to 0h, then the Address field specifies the starting 64-bit memory byte address of the next and last SGL segment, which is a SGL segment. If the SGL Identifier Descriptor Sub Type field is set to 1h, then the Address field contains an offset from the beginning of the location where data may be transferred.
11:08	**Length:** The Length field specifies the length in bytes of the next and last SGL segment. The Length field shall be a non-zero value and a multiple of 16. If the value in the Address field plus the value in the Length field is greater than 1_00000000_00000000h, then the SGL Last Segment descriptor shall be processed as having a Data SGL Length Invalid or Metadata SGL Length Invalid error.
14:12	Reserved
15	**SGL Identifier:** The definition of this field is described in the table below. **Bits** / **Description** 03:00 — **SGL Descriptor Sub Type:** Valid values are specified in Figure 115. 07:04 — **SGL Descriptor Type:** 3h as specified in Figure 114.

The Keyed SGL Data Block descriptor, defined in Figure 120, describes a keyed data block.

Figure 120: Keyed SGL Data Block descriptor

Bytes	Description
07:00	**Address:** The Address field specifies the starting 64-bit memory byte address of the data block.

Figure 120: Keyed SGL Data Block descriptor

Bytes	Description
10:08	**Length:** The Length field specifies the length in bytes of the data block. A Length field cleared to 0h specifies that no data is transferred. An SGL Data Block descriptor specifying that no data is transferred is a valid SGL Data Block descriptor. If the value in the Address field plus the value in the Length field is greater than 1_00000000_00000000h, then the SGL Data Block descriptor shall be processed as having a Data SGL Length Invalid or Metadata SGL Length Invalid error.
14:11	**Key:** Specifies a 32-bit key that is associated with the data block.
15	**SGL Identifier:** The definition of this field is described in the table below. **Bits** / **Description** 03:00 — **SGL Descriptor Sub Type:** Valid values are specified in Figure 115. 07:04 — **SGL Descriptor Type:** 4h as specified in Figure 114.

Figure 121: Transport SGL Data Block descriptor

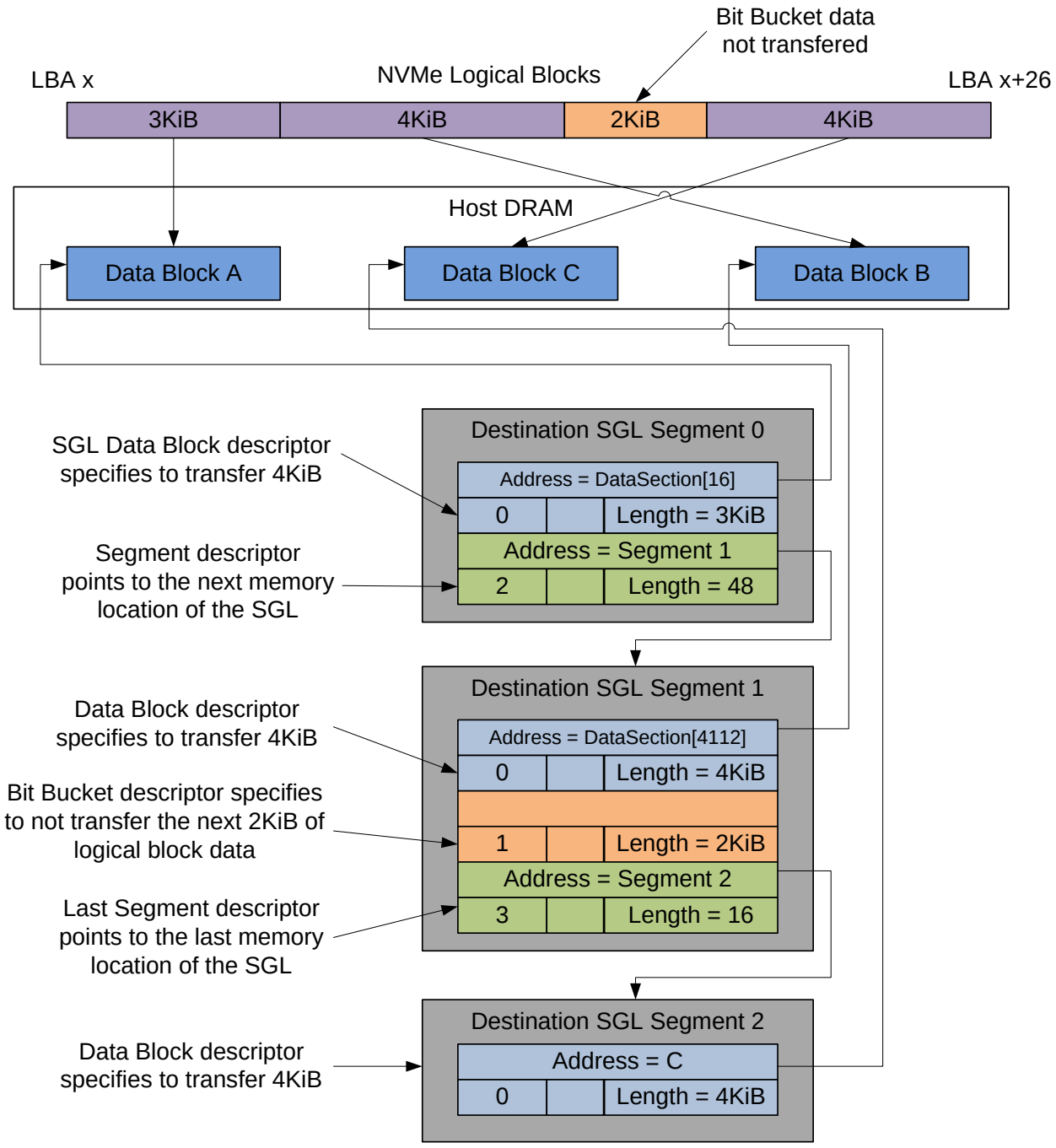
Bytes	Description
07:00	Reserved
11:08	**Length:** The Length field specifies the length in bytes of the data block. A Length field cleared to 0h specifies that no data is transferred. A Transport SGL Data Block descriptor specifying that no data is transferred is a valid Transport SGL Data Block descriptor. If the controller requires dword alignment and granularity as specified in the SGL Support field of Identify Controller (refer to Figure 251), then the lower two bits shall be cleared to 00b. The data transfer mechanism and data buffers for data specified by a Transport SGL Data Block descriptor are defined by the binding section for the associated NVMe Transport.
14:12	Reserved
15	**SGL Identifier:** The definition of this field is described in the table below. **Bits** / **Description** 03:00 — **SGL Descriptor Sub Type:** Valid values are specified in Figure 115. 07:04 — **SGL Descriptor Type:** 5h as specified in Figure 114.

4.4.1 SGL Example

Figure 122 shows an example of a data read request using SGLs. In the example, the logical block size is 512B. The total length of the logical blocks accessed is 13 KiB, of which only 11 KiB is transferred to the host. The Number of Logical Blocks (NLB) field in the command shall specify 26, indicating the total length of the logical blocks accessed on the controller is 13 KiB. There are three SGL segments describing the locations in memory where the logical block data is transferred.

The three SGL segments contain a total of three Data Block descriptors with lengths of 3 KiB, 4 KiB, and 4 KiB respectively. Segment 1 of the Destination SGL contains a Bit Bucket descriptor with a length of 2 KiB that specifies to not transfer (i.e., ignore) 2 KiB of logical block data from the NVM. Segment 1 of the destination SGL also contains a Last Segment descriptor specifying that the segment pointed to by the descriptor is the last SGL segment.

Figure 122: SGL Read Example



4.5 Metadata Region (MR)

Metadata may be supported for a namespace as part of the logical block (creating an extended logical block which is a larger logical block that is exposed to the application). Metadata may be transferred as interleaved with the logical block data (i.e., using the DPTR field) or as a separate buffer of data (i.e., using the MPTR field). The metadata shall not be split between the logical block data and a separate metadata buffer. For writes, the metadata shall be written atomically with its associated logical block. Refer to section 8.2.

In the case where the namespace is formatted to transfer the metadata as a separate buffer of data, then the Metadata Region is used. In this case, the location of the Metadata Region is indicated by the Metadata Pointer within the command.

The controller may support several physical formats of logical block size and associated metadata size. There may be performance differences between different physical formats. This is indicated as part of the Identify Namespace data structure.

If the namespace is formatted to use end-to-end data protection (refer to section 8.3), then the first eight bytes or last eight bytes of the metadata is used for protection information (specified as part of the Format NVM command).

4.6 Completion Queue Entry

An entry in the Completion Queue is at least 16 bytes in size. Figure 123 describes the layout of the first 16 bytes of the Completion Queue Entry data structure. The contents of Dword 0 are command specific. If a command uses Dword 0, then the definition of this dword is contained within the associated command definition. If a command does not use Dword 0, then the field is reserved. Dword 1 is reserved. Dword 2 is defined in Figure 124 and Dword 3 is defined in Figure 125. Any additional I/O Command Set defined in the future may use an alternate Completion Queue entry size or format.

If a Completion Queue Entry is constructed via multiple writes, the Phase Tag bit shall be updated in the last write of that Completion Queue Entry.

Figure 123: Completion Queue Entry Layout – Admin and NVM Command Set

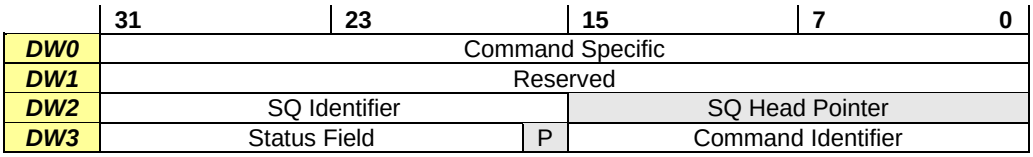


Figure 124: Completion Queue Entry: DW 2

Bits	Description
31:16	**SQ Identifier (SQID):** Indicates the Submission Queue to which the associated command was issued. This field is used by host software when more than one Submission Queue shares a single Completion Queue to uniquely determine the command completed in combination with the Command Identifier (CID). This is a reserved field in NVMe over Fabrics implementations.
15:00	**SQ Head Pointer (SQHD):** Indicates the current Submission Queue Head pointer for the Submission Queue indicated in the SQ Identifier field. This is used to indicate to the host the Submission Queue entries that have been consumed and may be re-used for new entries. Note: The value returned is the value of the SQ Head pointer when the completion queue entry was created. By the time host software consumes the completion queue entry, the controller may have an SQ Head pointer that has advanced beyond the value indicated.

Figure 125: Completion Queue Entry: DW 3

Bits	Description
31:17	**Status Field (SF):** Indicates status for the command that is being completed. Refer to section 4.6.1.

Figure 125: Completion Queue Entry: DW 3

Bits	Description
16	**Phase Tag (P):** Identifies whether a Completion Queue entry is new. The Phase Tag values for all Completion Queue entries shall be initialized to '0' by host software prior to setting CC.EN to '1'. When the controller places an entry in the Completion Queue, the controller shall invert the Phase Tag to enable host software to discriminate a new entry. Specifically, for the first set of completion queue entries after CC.EN is set to '1' all Phase Tags are set to '1' when they are posted. For the second set of completion queue entries, when the controller has wrapped around to the top of the Completion Queue, all Phase Tags are cleared to '0' when they are posted. The value of the Phase Tag is inverted each pass through the Completion Queue. This is a reserved bit in NVMe over Fabrics implementations.
15:00	**Command Identifier (CID):** Indicates the identifier of the command that is being completed. This identifier is assigned by host software when the command is submitted to the Submission Queue. The combination of the SQ Identifier and Command Identifier uniquely identifies the command that is being completed. The maximum number of requests outstanding for a Submission Queue at one time is 64 Ki.

4.6.1 Status Field Definition

The Status Field defines the status for the command indicated in the completion queue entry, defined in Figure 126.

A value of 0h for the Status Field indicates a successful command completion, with no fatal or non-fatal error conditions. Unless otherwise noted, if a command fails to complete successfully for multiple reasons, then the particular status code returned is chosen by the vendor.

Figure 126: Completion Queue Entry: Status Field

Bits	Description
31	**Do Not Retry (DNR):** If set to '1', indicates that if the same command is re-submitted to any controller in the NVM subsystem, then that re-submitted command is expected to fail. If cleared to '0', indicates that the same command may succeed if retried. If a command is aborted due to time limited error recovery (refer to section 5.21.1.5), this bit should be cleared to '0'. If the SCT and SC fields are cleared to 0h, then this bit should be cleared to '0'.
30	**More (M):** If set to '1', there is more status information for this command as part of the Error Information log that may be retrieved with the Get Log Page command. If cleared to '0', there is no additional status information for this command. Refer to section 5.14.1.1.
29:28	**Command Retry Delay (CRD):** If the DNR bit is cleared to '0' and the host has set the Advanced Command Retry Enable (ACRE) field to 1h in the Host Behavior Support feature (refer to section 5.21.1.22), then: a) a 00b CRD value indicates a command retry delay time of zero (i.e., the host may retry the command immediately); and b) a non-zero CRD value selects a field in the Identify Controller data structure (refer to Figure 251) that indicates the command retry delay time: • a 01b CRD value selects the Command Retry Delay Time 1 (CRDT1) field; • a 10b CRD value selects the Command Retry Delay Time 2 (CRDT2) field; and • a 11b CRD value selects the Command Retry Delay Time 3 (CRDT3) field. The host should not retry the command until at least the amount of time indicated by the selected field has elapsed. It is not an error for the host to retry the command prior to that time. If the DNR bit is set to'1' in the Status field or the ACRE field is cleared to 0h in the Host Behavior Support feature, then this field is reserved. If the SCT and SC fields are cleared to 0h, then this field should be cleared to 00b.
27:25	**Status Code Type (SCT):** Indicates the status code type of the completion queue entry. This indicates the type of status the controller is returning.

Figure 126: Completion Queue Entry: Status Field

Bits	Description
24:17	**Status Code (SC):** Indicates a status code identifying any error or status information for the command indicated.

4.6.1.1 Status Code Type (SCT)

Completion queue entries indicate a status code type for the type of completion being reported. Figure 127 specifies the status code type values and descriptions.

Figure 127: Status Code – Status Code Type Values

Value	Description	Reference
0h	**Generic Command Status:** Indicates that the command specified by the Command and Submission Queue identifiers in the completion queue entry has completed. These status values are generic across all command types, and include such conditions as success, opcode not supported, and invalid field.	4.6.1.2.1
1h	**Command Specific Status:** Indicates a status value that is specific to a particular command opcode. These values may indicate additional processing is required. Status values such as invalid firmware image or exceeded maximum number of queues is reported with this type.	4.6.1.2.2
2h	**Media and Data Integrity Errors:** Any media specific errors that occur in the NVM or data integrity type errors shall be of this type.	4.6.1.2.3
3h	**Path Related Status:** Indicates that the command specified by the Command and Submission Queue identifier in the completion queue entry has completed. These status values are generic across all command types. These values may indicate that additional process is required and indicate a status value that is specific to: a) the connection between the host and the controller processing the command; or b) the characteristics that support Asymmetric Namespace Access Reporting (refer to section 8.20), the characteristics of the relationship between the controller processing the command and the specified namespace.	4.6.1.2.4
4h to 6h	Reserved	
7h	Vendor Specific	

4.6.1.2 Status Code (SC)

The Status Code (SC) field in the completion queue entry indicates more detailed status information about the completion being reported.

Each Status Code set of values is split into three ranges:

- 00h to 7Fh: Applicable to Admin Command Set, or across multiple command sets;
- 80h to BFh: I/O Command Set Specific status codes; and
- C0h to FFh: Vendor Specific status codes.

Unless otherwise specified, if multiple status codes apply, then the controller selects the status code that is returned.

4.6.1.2.1 Generic Command Status Definition

Completion queue entries with a Status Code type of Generic Command Status indicate a status value associated with the command that is generic across many different types of commands.

Figure 128: Status Code – Generic Command Status Values

Value	Description
00h	**Successful Completion:** The command completed without error.
01h	**Invalid Command Opcode:** A reserved coded value or an unsupported value in the command opcode field.
02h	**Invalid Field in Command:** A reserved coded value or an unsupported value in a defined field (other than the opcode field). This status code should be used unless another status code is explicitly specified for a particular condition. The field may be in the command parameters as part of the Submission Queue Entry or in data structures pointed to by the command parameters.
03h	**Command ID Conflict:** The command identifier is already in use. Note: It is implementation specific how many commands are searched for a conflict.
04h	**Data Transfer Error:** Transferring the data or metadata associated with a command had an error.
05h	**Commands Aborted due to Power Loss Notification:** Indicates that the command was aborted due to a power loss notification.
06h	**Internal Error:** The command was not completed successfully due to an internal error. Details on the internal device error should be reported as an asynchronous event. Refer to Figure 147 for Internal Error Asynchronous Event Information.
07h	**Command Abort Requested:** The command was aborted due to an Abort command being received that specified the Submission Queue Identifier and Command Identifier of this command (refer to section 5.1).
08h	**Command Aborted due to SQ Deletion:** The command was aborted due to a Delete I/O Submission Queue request received for the Submission Queue to which the command was submitted.
09h	**Command Aborted due to Failed Fused Command:** The command was aborted due to the other command in a fused operation failing.
0Ah	**Command Aborted due to Missing Fused Command:** The fused command was aborted due to the adjacent submission queue entry not containing a fused command that is the other command in a supported fused operation (refer to section 6.2).
0Bh	**Invalid Namespace or Format:** The namespace or the format of that namespace is invalid.
0Ch	**Command Sequence Error:** The command was aborted due to a protocol violation in a multi-command sequence (e.g., a violation of the Security Send and Security Receive sequencing rules in the TCG Storage Synchronous Interface Communications protocol (refer to TCG Storage Architecture Core Specification)).
0Dh	**Invalid SGL Segment Descriptor:** The command includes an invalid SGL Last Segment or SGL Segment descriptor. This may occur under various conditions, including: • the SGL segment pointed to by an SGL Last Segment descriptor contains an SGL Segment descriptor or an SGL Last Segment descriptor; • an SGL Last Segment descriptor contains an invalid length (i.e., a length of 0h or 1h that is not a multiple of 16); or • an SGL Segment descriptor or an SGL Last Segment descriptor contains an invalid address (e.g., an address that is not qword aligned).
0Eh	**Invalid Number of SGL Descriptors:** There is an SGL Last Segment descriptor or an SGL Segment descriptor in a location other than the last descriptor of a segment based on the length indicated. This is also used for invalid SGLs in a command capsule (refer to NVMe over Fabrics specification).
0Fh	**Data SGL Length Invalid:** This may occur if the length of a Data SGL is too short. This may occur if the length of a Data SGL is too long and the controller does not support SGL transfers longer than the amount of data to be transferred as indicated in the SGL Support field of the Identify Controller data structure.
10h	**Metadata SGL Length Invalid:** This may occur if the length of a Metadata SGL is too short. This may occur if the length of a Metadata SGL is too long and the controller does not support SGL transfers longer than the amount of data to be transferred as indicated in the SGL Support field of the Identify Controller data structure.
11h	**SGL Descriptor Type Invalid:** The type of an SGL Descriptor is a type that is not supported by the controller, or the combination of type and subtype is not supported by the controller.
12h	**Invalid Use of Controller Memory Buffer:** The attempted use of the Controller Memory Buffer is not supported by the controller. Refer to section 4.7.

Figure 128: Status Code – Generic Command Status Values

Value	Description
13h	**PRP Offset Invalid:** The Offset field for a PRP entry is invalid. This may occur when there is a PRP entry with a non-zero offset after the first entry or when the Offset field in any PRP entry is not dword aligned (i.e., bits 1:0 are not cleared to 00b).
14h	**Atomic Write Unit Exceeded:** The length specified exceeds the atomic write unit size.
15h	**Operation Denied:** The command was denied due to lack of access rights. Refer to the appropriate security specification (e.g., TCG Storage Interface Interactions Specification). For media access commands, the Access Denied status code should be used instead.
16h	**SGL Offset Invalid:** The offset specified in a descriptor is invalid. This may occur when using capsules for data transfers in NVMe over Fabrics implementations and an invalid offset in the capsule is specified.
17h	Reserved
18h	**Host Identifier Inconsistent Format:** The NVM subsystem detected the simultaneous use of 64-bit and 128-bit Host Identifier values on different controllers.
19h	**Keep Alive Timer Expired:** The Keep Alive Timer expired.
1Ah	**Keep Alive Timeout Invalid:** The Keep Alive Timeout value specified is invalid. This may be due to an attempt to specify a value of 0h on a transport that requires the Keep Alive feature to be enabled. This may be due to the value specified being too large for the associated NVMe Transport as defined in the NVMe Transport binding specification.
1Bh	**Command Aborted due to Preempt and Abort:** The command was aborted due to a Reservation Acquire command with the Reservation Acquire Action (RACQA) set to 010b (Preempt and Abort).
1Ch	**Sanitize Failed:** The most recent sanitize operation failed and no recovery action has been successfully completed.
1Dh	**Sanitize In Progress:** The requested function (e.g., command) is prohibited while a sanitize operation is in progress. Refer to section 8.15.1.
1Eh	**SGL Data Block Granularity Invalid:** The Address alignment or Length granularity for an SGL Data Block descriptor is invalid. This may occur when a controller supports dword granularity only and the lower two bits of the Address or Length are not cleared to 00b. Note: An implementation compliant to revision 1.2.1 or earlier may use the status code value of 15h to indicate SGL Data Block Granularity Invalid.
1Fh	**Command Not Supported for Queue in CMB:** The implementation does not support submission of the command to a Submission Queue in the Controller Memory Buffer or command completion to a Completion Queue in the Controller Memory Buffer. Note: Revision 1.3 and later of this specification use this status code only for Sanitize commands.
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected as a result of a change in the namespace write protection state as defined by the Namespace Write Protection State Machine (refer to Figure 493).
21h	**Command Interrupted:** Command processing was interrupted and the controller is unable to successfully complete the command. The host should retry the command. If this status code is returned, then the controller shall clear the Do Not Retry bit to '0' in the Status field of the CQE (refer to Figure 126). The controller shall not return this status code unless the host has set the Advanced Command Retry Enable (ACRE) field to 1h in the Host Behavior Support feature (refer to section 5.21.1.22).
22h	**Transient Transport Error:** A transient transport error was detected. If the command is retried on the same controller, the command is likely to succeed. A command that fails with a transient transport error four or more times should be treated as a persistent transport error that is not likely to succeed if retried on the same controller.
23h to 7Fh	Reserved
80h to BFh	I/O Command Set Specific
C0h to FFh	Vendor Specific

Figure 129: Status Code – Generic Command Status Values, NVM Command Set

Value	Description
80h	**LBA Out of Range:** The command references an LBA that exceeds the size of the namespace.
81h	**Capacity Exceeded:** Execution of the command has caused the capacity of the namespace to be exceeded. This error occurs when the Namespace Utilization exceeds the Namespace Capacity, as reported in Figure 249.
82h	**Namespace Not Ready:** The namespace is not ready to be accessed as a result of a condition other than a condition that is reported as an Asymmetric Namespace Access condition. The Do Not Retry bit indicates whether re-issuing the command at a later time may succeed.
83h	**Reservation Conflict:** The command was aborted due to a conflict with a reservation held on the accessed namespace. Refer to section 8.8.
84h	**Format In Progress:** A Format NVM command is in progress on the namespace. The Do Not Retry bit shall be cleared to '0' to indicate that the command may succeed if resubmitted.
85h to BFh	Reserved

4.6.1.2.2 Command Specific Status Definition

Completion queue entries with a Status Code Type of Command Specific Errors indicate an error that is specific to a particular command opcode. Status codes of 00h to 7Fh are for Admin command errors. Status codes of 80h to BFh are specific to the selected I/O command set.

Figure 130: Status Code – Command Specific Status Values

Value	Description	Commands Affected
00h	Completion Queue Invalid	Create I/O Submission Queue
01h	Invalid Queue Identifier	Create I/O Submission Queue, Create I/O Completion Queue, Delete I/O Completion Queue, Delete I/O Submission Queue
02h	Invalid Queue Size	Create I/O Submission Queue, Create I/O Completion Queue
03h	Abort Command Limit Exceeded	Abort
04h	Reserved	
05h	Asynchronous Event Request Limit Exceeded	Asynchronous Event Request
06h	Invalid Firmware Slot	Firmware Commit
07h	Invalid Firmware Image	Firmware Commit
08h	Invalid Interrupt Vector	Create I/O Completion Queue
09h	Invalid Log Page	Get Log Page
0Ah	Invalid Format	Format NVM, Namespace Management
0Bh	Firmware Activation Requires Conventional Reset	Firmware Commit, Sanitize
0Ch	Invalid Queue Deletion	Delete I/O Completion Queue
0Dh	Feature Identifier Not Saveable	Set Features
0Eh	Feature Not Changeable	Set Features
0Fh	Feature Not Namespace Specific	Set Features
10h	Firmware Activation Requires NVM Subsystem Reset	Firmware Commit, Sanitize
11h	Firmware Activation Requires Controller Level Reset	Firmware Commit, Sanitize
12h	Firmware Activation Requires Maximum Time Violation	Firmware Commit
13h	Firmware Activation Prohibited	Firmware Commit
14h	Overlapping Range	Firmware Commit, Firmware Image Download, Set Features
15h	Namespace Insufficient Capacity	Namespace Management
16h	Namespace Identifier Unavailable	Namespace Management
17h	Reserved	
18h	Namespace Already Attached	Namespace Attachment
19h	Namespace Is Private	Namespace Attachment
1Ah	Namespace Not Attached	Namespace Attachment

Figure 130: Status Code – Command Specific Status Values

Value	Description	Commands Affected
1Bh	Thin Provisioning Not Supported	Namespace Management
1Ch	Controller List Invalid	Namespace Attachment
1Dh	Device Self-test In Progress	Device Self-test
1Eh	Boot Partition Write Prohibited	Firmware Commit
1Fh	Invalid Controller Identifier	Virtualization Management
20h	Invalid Secondary Controller State	Virtualization Management
21h	Invalid Number of Controller Resources	Virtualization Management
22h	Invalid Resource Identifier	Virtualization Management
23h	Sanitize Prohibited While Persistent Memory Region is Enabled	Sanitize
24h	ANA Group Identifier Invalid	Namespace Management
25h	ANA Attach Failed	Namespace Attachment
26h to 6Fh	Reserved	
70h to 7Fh	Directive Specific	NOTE 1
80h to BFh	I/O Command Set Specific	NOTE 2
C0h to FFh	Vendor Specific	

NOTES:
1. The Directives Specific range defines Directives specific status values. Refer to section 9.
2. The I/O Command Set Specific range in the NVMe over Fabrics specification defines Fabrics command specific status values.

Figure 131: Status Code – Command Specific Status Values, NVM Command Set

Value	Description	Commands Affected
80h	Conflicting Attributes	Dataset Management, Read, Write
81h	Invalid Protection Information	Compare, Read, Verify, Write, Write Zeroes
82h	Attempted Write to Read Only Range	Dataset Management, Write, Write Uncorrectable, Write Zeroes, Flush, Format NVM
83h to BFh	Reserved	

4.6.1.2.3 Media and Data Integrity Errors Definition

Completion queue entries with a Status Code Type of Media and Data Integrity Errors indicate an error associated with the command that is due to an error associated with the NVM media or a data integrity type error.

Figure 132: Status Code – Media and Data Integrity Error Values

Value	Description
00h to 7Fh	Reserved
80h to BFh	I/O Command Set Specific
C0h to FFh	Vendor Specific

Figure 133: Status Code – Media and Data Integrity Error Values, NVM Command Set

Value	Description
80h	**Write Fault:** The write data could not be committed to the media.
81h	**Unrecovered Read Error:** The read data could not be recovered from the media.

Figure 133: Status Code – Media and Data Integrity Error Values, NVM Command Set

Value	Description
82h	**End-to-end Guard Check Error:** The command was aborted due to an end-to-end guard check failure.
83h	**End-to-end Application Tag Check Error:** The command was aborted due to an end-to-end application tag check failure.
84h	**End-to-end Reference Tag Check Error:** The command was aborted due to an end-to-end reference tag check failure.
85h	**Compare Failure:** The command failed due to a miscompare during a Compare command.
86h	**Access Denied:** Access to the namespace and/or LBA range is denied due to lack of access rights. Refer to the appropriate security specification (e.g., TCG Storage Interface Interactions Specification).
87h	**Deallocated or Unwritten Logical Block:** The command failed due to an attempt to read from or verify an LBA range containing a deallocated or unwritten logical block.
88h to BFh	Reserved

4.6.1.2.4 Path Related Status Definition

Completion queue entries with a Status Code type of Path Related Status (refer to Figure 134) indicate a status value associated with the command that is generic across many different types of commands and applies to a specific connection between the host and controller processing the command or between the controller and the namespace. The command for which this status is returned may be retried on a different controller in the same NVM subsystem if more than one controller is available to the host.

In a multipath environment, unless otherwise specified, errors of this type should be retried using a different path, if one is available.

Figure 134: Status Code – Path Related Status Values

Value	Description
00h	**Internal Path Error:** The command was not completed as the result of a controller internal error that is specific to the controller processing the command. Retries for the request function should be based on the setting of the DNR bit (refer to Figure 126).
01h	**Asymmetric Access Persistent Loss:** The requested function (e.g., command) is not able to be performed as a result of the relationship between the controller and the namespace being in the ANA Persistent Loss state (refer to section 8.20.3.4). The command should not be re-submitted to the same controller.
02h	**Asymmetric Access Inaccessible:** The requested function (e.g., command) is not able to be performed as a result of the relationship between the controller and the namespace being in the ANA Inaccessible state (refer to section 8.20.3.3). The command should not be re-submitted to the same controller.
03h	**Asymmetric Access Transition:** The requested function (e.g., command) is not able to be performed as a result of the relationship between the controller and the namespace transitioning between Asymmetric Namespace Access states (refer to section 8.20.3.5). The requested function should be retried after the transition is complete.
04h to 5Fh	Reserved
Controller detected Pathing errors	
60h	**Controller Pathing Error:** A pathing error was detected by the controller.
61h to 6Fh	Reserved
Host detected Pathing errors	
70h	**Host Pathing Error:** A pathing error was detected by the host.
71h	**Command Aborted By Host:** The command was aborted as a result of host action (e.g., the host disconnected the Fabric connection).
72h to 7Fh	Reserved
Other Pathing errors	

Figure 134: Status Code – Path Related Status Values

Value	Description
80h to BFh	I/O Command Set Specific
C0h to FFh	Vendor Specific

4.7 Controller Memory Buffer

The Controller Memory Buffer (CMB) is a region of general purpose read/write memory on the controller. The controller indicates support for the CMB by setting CAP.CMBS to ‘1’. The host indicates intent to use the CMB by setting CMBMSC.CRE to ‘1’. Once this bit is set to ‘1’, the controller indicates the properties of the CMB via the CMBLOC and CMBSZ registers.

The CMB may be used for a variety of purposes. The controller indicates which purposes the memory may be used for by setting support flags in the CMBSZ register.

The CMB’s PCI Express address range is used for external memory read and write requests to the CMB. The PCI Express base address of the CMB is defined by the PCI Base Address Register (BAR) indicated by CMBLOC.BIR, and the offset indicated by CMBLOC.OFST. The size of the CMB is indicated by CMBSZ.SZ.

The controller uses the CMB’s controller address range to reference CMB with addresses supplied by the host. The PCI Express address range and the controller address range of the CMB may differ, but both ranges have the same size, and equivalent offsets within each range have a one-to-one correspondence. The host configures the controller address range via the CMBMSC register.

The host enables the CMB’s controller memory space via the CMBMSC.CMSE bit. When controller memory space is enabled, if host supplies an address referencing the CMB’s controller address range, then the controller directs memory read or write requests for this address to the CMB.

When the CMB’s controller memory space is disabled, the controller does not consider any host-supplied address to reference the CMB’s controller address range, and memory read and write requests are directed elsewhere (e.g., to memory other than the CMB).

To prevent possible misdirection of the controller’s memory requests, before host software enables the CMB’s controller memory space, the host should configure the CMB’s controller address range to so that the addresses do not overlap any address that host software intends to use for DMA.

In earlier versions of this specification, for a controller that supports the CMB, the CMB’s controller address range is fixed to be equal to its PCI Express address range, and the CMB’s controller memory space is always enabled whenever the controller is enabled. To prevent misdirection of controller memory requests when such a controller is assigned to a virtual machine, host software (on the hypervisor or host OS) should not enable translation of the CMB’s PCI Express address range and should ensure that this address range does not overlap any range of pre-translated addresses that the virtual machine may use for DMA.

Host software may configure CMBMSC so that CMB operates when the controller is assigned to a virtual machine that only supports versions 1.3 and earlier of this specification. To prevent that virtual machine from unintentionally clearing CMBMSC to 0h, the contents of CMBSMC are preserved across Controller Reset and Function Level Reset.

Submission Queues in host memory require the controller to perform a PCI Express read from host memory in order to fetch the queue entries. Submission Queues in controller memory enable host software to directly write the entire Submission Queue Entry to the controller's internal memory space, avoiding one read from the controller to the host. This approach reduces latency in command execution and improves efficiency in a PCI Express fabric topology that may include multiple switches. Similarly, PRP Lists or SGLs require separate fetches across the PCI Express fabric, which may be avoided by writing the PRP or SGL to the Controller Memory Buffer. Completion Queues in the Controller Memory Buffer may be used for peer to peer or other applications. For writes of small amounts of data, it may be advantageous to have the host

write the data and/or metadata to the Controller Memory Buffer rather than have the controller fetch it from host memory.

The contents of the Controller Memory Buffer are undefined as the result of:

- the CMBMSC.CMSE bit transitioning from ‘0’ to ‘1’;
- a Controller Reset; or
- a Function Level Reset.

Host software should initialize any memory in the Controller Memory Buffer before being referenced (e.g., a Completion Queue shall be initialized by host software in order for the Phase Tag to be used correctly).

A controller memory based queue is used in the same manner as a host memory based queue – the difference is the memory address used is located within the controller’s own memory rather than in the host memory. The Admin or I/O Queues may be placed in the Controller Memory Buffer. If the CMBLOC.CQMMS bit (refer to Figure 84) is cleared to ‘0’, then for a particular queue, all memory associated with it shall reside in either the Controller Memory Buffer or outside the Controller Memory Buffer.

If the CMBLOC.CQPDS bit (refer to Figure 84) is cleared to ‘0’, then for all queues in the Controller Memory Buffer, the queue shall be physically contiguous.

The controller may support PRP Lists and SGLs in the Controller Memory Buffer. If the CMBLOC.CDPMLS bit (refer to Figure 84) is cleared to ‘0’, then for a particular PRP List or SGL associated with a single command, all memory associated with the PRP List or SGL shall be either entirely located in the Controller Memory Buffer or entirely located outside the Controller Memory Buffer.

PRP Lists and SGLs associated with a command may be placed in the Controller Memory Buffer if that command is present in a Submission Queue in the Controller Memory Buffer. If:

a) CMBLOC.CDPCILS bit (refer to Figure 84) is cleared to ‘0’; and
b) a command is not present in a Submission Queue in the Controller Memory Buffer,

then the PRP Lists and SGLs associated with that command shall not be placed in the Controller Memory Buffer.

The controller may support data and metadata in the Controller Memory Buffer. If the CMBLOC.CDMMMS bit (refer to Figure 84) is cleared to ‘0’, then all data and metadata, if any, associated with a particular command shall be either entirely located in the Controller Memory Buffer or entirely located outside the Controller Memory Buffer.

If the requirements for the Controller Memory Buffer use are violated by the host, the controller shall fail the associated command with Invalid Use of Controller Memory Buffer status.

The address region allocated for the CMB shall be 4 KiB aligned. It is recommended that a controller allocate the CMB on an 8 KiB boundary. The controller shall support burst transactions up to the maximum payload size, support byte enables, and arbitrary byte alignment. The host shall ensure that all writes to the CMB that are needed for a command have been sent before updating the SQ Tail doorbell register. The Memory Write Request to the SQ Tail doorbell register shall not have the Relaxed Ordering bit set to ‘1’, to ensure that prior writes to the CMB have completed.

4.8 Persistent Memory Region

The Persistent Memory Region (PMR) is an optional region of general purpose PCI Express read/write persistent memory that may be used for a variety of purposes. The controller indicates support for the PMR by setting CAP.PMRS to ‘1’ and indicates whether the controller supports command data and metadata transfers to or from the PMR by setting support flags in the PMRCAP register. When command data and metadata transfers to or from PMR are supported, all data and metadata associated with a particular command shall be either entirely located in the Persistent Memory Region or outside the Persistent Memory Region.

The PMR’s PCI Express address range is used for external memory read and write requests to the PMR. The PCI Express address range and size of the PMR is defined by the PCI Base Address Register (BAR)

indicated by PMRCAP.BIR. The PMR consumes the entire address region exposed by the BAR and supports all the required features of the PCI Express programming model (i.e., it in no way restricts what is otherwise permitted by PCI Express).

The controller uses the PMR's controller address range to reference PMR with addresses supplied by the host. The PCI Express address range and the controller address range of the PMR may differ, but both ranges have the same size, and equivalent offsets within each range have a one-to-one correspondence. The host configures the controller address range via the PMRMSCU and PMRMSCL registers.

The host enables the PMR's controller memory space via the PMRMSCL.CMSE bit. When controller memory space is enabled, if host supplies an address referencing the PMR's controller address range, then the controller directs memory read or write requests for this address to the PMR.

When the PMR's controller memory space is disabled, the controller does not consider any host-supplied address to reference the PMR's controller address range, and memory read and write requests are directed elsewhere (e.g., to memory other than the PMR).

The contents of data written to the PMR while the PMR is ready persists across power cycles, Controller Level Resets, and disabling of the PMR. The mechanism used to make a write to the PMR persistent is implementation specific. For example, in one implementation this may mean that a write to non-volatile memory has completed while in another implementation this may mean that the write has been stored in a non-volatile write buffer and is written to non-volatile memory at some later point.

A PMR implementation has a maximum sustained write throughput. The PMR implementation may also have an optional write elasticity buffer used to buffer writes from PMR PCIe write requests. When the PMR sustained write throughput is less than the PCI Express link throughput, then such a write elasticity buffer allows PCIe write request burst throughput to exceed the PMR sustained write throughput without back pressuring into the PCI Express fabric.

The time required to transfer data from the write elasticity buffer to nonvolatile media is the amount of data written to the elasticity buffer divided by the Persistent Memory Region Sustained Write Throughput (refer to section 3.1.22). The time to transfer the entire contents of the write elasticity buffer is the Persistent Memory Region Elasticity Buffer Size (refer to section 3.1.21) divided by the Persistent Memory Region Sustained Write Throughput.

The host enables the PMR by setting PMRCTL.EN to '1'. Once enabled, the controller indicates that the PMR is ready by clearing PMRSTS.NRDY to '0'. It is not necessary to enable the controller to enable the PMR. Restoring and saving the contents of the PMR may take time to complete. When the host modifies the value of PMRCTL.EN, the host should wait for at least the time interval specified in PMRCAP.PMRTO for PMRSTS.NRDY to reflect the change.

When the PMR is not ready, PMR reads complete successfully and return an undefined value while PMR writes complete normally, but do not update memory (i.e., the contents of the PMR address written remains unchanged). The undefined value returned by a PMR read following a sanitize operation is such that recovery of any previous user data from any cache or the non-volatile media is not possible.

When the PMR becomes read-only or unreliable, then a critical warning is reported in the SMART/Health Information Log which may be used to trigger an NVMe interface asynchronous event. Since reporting of an asynchronous event may occur an unspecified amount of time after the PMR health status has changed, the host should assume that all operations to the PMR have been affected since the last time normal operation was reported in PMRSTS.HSTS.

PMRCAP.PMRWBM enumerates supported PMR write barrier mechanisms. At least one mechanism shall be supported. An implementation may optionally support a mechanism where a PCI Express read of any size to the PMR, including a "zero-length read," ensures that all previous memory writes (i.e., Posted PCI Express requests) to the PMR have completed and are persistent. An implementation may optionally support a write barrier mechanism that utilizes a read of the PMRSTS register. When supported, a read of the PMRSTS register allows a host to:

- ensure that previously issued memory writes to the PMR have completed; and

- determine whether the PMR updates associated with those writes have completed without error and are persistent.

A PMR memory write error may be the result of a poisoned PCI Express TLP, an NVM subsystem internal error, or a PMR health status issue.

Regardless of the supported PMR write barrier mechanisms, a host may periodically read PMRSTS to ensure that reads to the PMR have returned valid data. For example, if a read to the PMRSTS register indicates that the PMR is operating normally is then followed by a series of reads, and finally a second read to the PMRSTS register that indicates the PMR is unreliable, then one or more of the reads between the two PMRSTS reads may have returned invalid data. Such polling of the PMRSTS register may be unnecessary if the host handles poisoned TLPs and/or poisoned TLP error reporting is enabled.

The PMR write elasticity buffer size along with the PMR sustained write throughput allows a host to determine the amount of time for a read associated with a persistent memory region write barrier mechanism to complete.

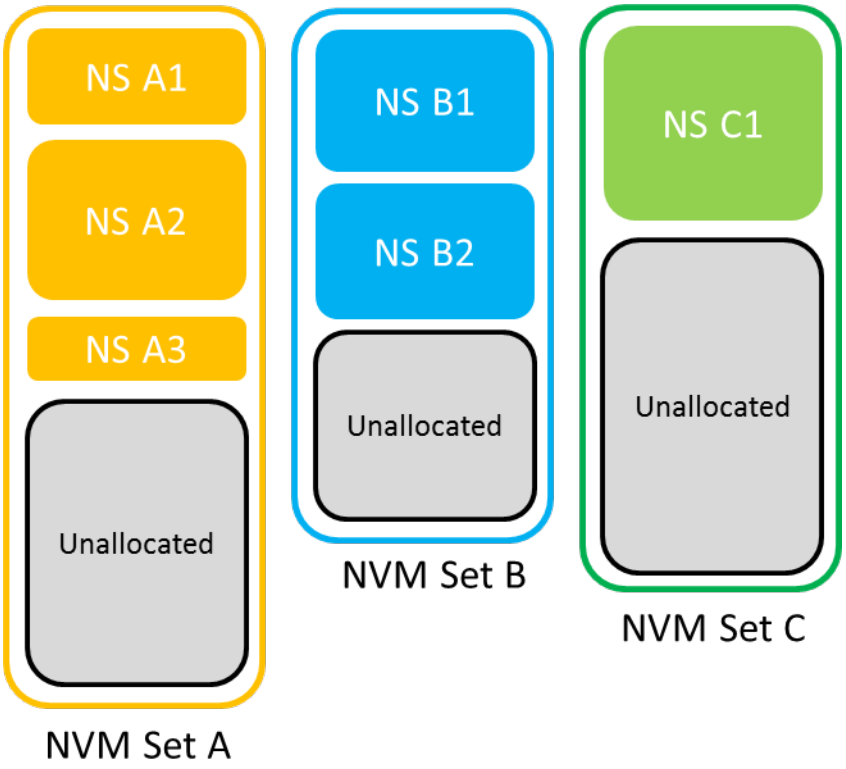
Support for PRPs, SGL Lists, Completion Queues, and Submission Queues in the Persistent Memory Region is outside the scope of this specification. If the host attempts to use the Persistent Memory Region for a PRP, SGL List, Completion Queue, or Submission Queue, the controller may abort the command with a status code of Invalid Field in Command.

4.9 NVM Sets

An NVM Set is a collection of NVM that is separate (logically and potentially physically) from NVM in other NVM Sets. One or more namespaces may be created within an NVM Set and those namespaces inherit the attributes of the NVM Set. A namespace is wholly contained within a single NVM Set and shall not span more than one NVM Set.

Figure 135 shows an example of three NVM Sets. NVM Set A contains three namespaces (NS A1, NS A2, and NS A3). NVM Set B contains two namespaces (NS B1 and NS B2). NVM Set C contains one namespace (NS C1). Each NVM Set shown also contains ‘Unallocated’ regions that consist of NVM that is not yet allocated to a namespace.

Figure 135: NVM Sets and Associated Namespaces



There is a subset of Admin commands that are NVM Set aware as described in Figure 136.

Figure 136: NVM Set Aware Admin Commands

Admin Command	Details
Identify	• The Identify Namespace data structure includes the associated NVM Set Identifier. • The NVM Set List data structure includes attributes for each NVM Set.
Namespace Management	• The create action includes the NVM Set Identifier as a host specified field.
Get Features and Set Features	• The Read Recovery Level Feature specifies the associated NVM Set Identifier. • The Predictable Latency Mode Config Feature specifies the associated NVM Set Identifier. • The Predictable Latency Mode Window Feature specifies the associated NVM Set Identifier.

The host determines the NVM Sets present and their attributes using the Identify command with CNS value of 04h to retrieve the NVM Set List (refer to Figure 254). For each NVM Set, the attributes include:

- an identifier associated with the NVM Set;
- the optimal size for writes to the NVM Set;
- the total capacity of the NVM Set; and
- the unallocated capacity for the NVM Set.

An NVM Set Identifier is a 16-bit value that specifies the NVM Set with which an action is associated. An NVM Set Identifier may be specified in NVM Set aware Admin commands (refer to Figure 136). An NVM Set Identifier value of 0h is reserved and is not a valid NVM Set Identifier. Unless otherwise specified, if the

host specifies an NVM Set Identifier cleared to 0h for a command that requires an NVM Set Identifier, then that command shall abort with a status code of Invalid Field in Command.

Each NVM Set is associated with exactly one Endurance Group (refer to section 8.17).

The NVM Set with which a namespace is associated is reported in the Identify Namespace data structure (refer to Figure 249). When a host creates a namespace using the Namespace Management command, the host specifies the NVM Set Identifier of the NVM Set that the namespace is to be created in. The namespace that is created inherits attributes from the NVM Set (e.g., the optimal write size to the NVM).

If NVM Sets are supported, then all controllers in the NVM subsystem shall:

- Indicate support for NVM Sets in the Controller Attributes field in the Identify Controller data structure;
- Support the NVM Set Identifier in all commands that use the NVM Set Identifier;
- Support the NVM Set List for the Identify command;
- Indicate the NVM Set Identifier with which the namespace is associated in the Identify Namespace data structure;
- Support Endurance Groups; and
- For each NVM Set, indicate the associated Endurance Group as an attribute.

4.10 Namespace List

A Namespace List, defined in Figure 137, is an ordered list of namespace IDs. Unused entries are zero filled.

Figure 137: Namespace List Format

Bytes	Description
03:00	**Identifier 0:** This field contains the lowest namespace ID in the list or 0h if the list is empty.
07:04	**Identifier 1:** This field contains the second lowest namespace ID in the list or 0h if the list contains less than two entries.
…	…
(N*4+3):(N*4)	**Identifier N:** This field contains the N+1 lowest namespace ID in the list or 0h if the list contains fewer than N entries.

4.11 Controller List

A Controller List, defined in Figure 138, is an ordered list of ascending controller IDs. The controller identifier is defined in bytes 79:78 of the Identify data structure in Figure 251. Unused entries are zero filled.

Figure 138: Controller List Format

Bytes	Description
01:00	**Number of Identifiers:** This field contains the number of controller entries in the list. There may be up to 2,047 identifiers in the list. A value of 0h indicates there are no controllers in the list.
03:02	**Identifier 0:** This field contains the NVM subsystem unique controller identifier for the first controller in the list, if present.
05:04	**Identifier 1:** This field contains the NVM subsystem unique controller identifier for the second controller in the list, if present.
…	…
(N*2+3):(N*2+2)	**Identifier N:** This field contains the NVM subsystem unique controller identifier for the N+1 controller in the list, if present.

4.12 Fused Operations

Fused operations enable a more complex command by “fusing” together two simpler commands. This feature is optional; support for this feature is indicated in FUSES field in the Identify Controller data structure in Figure 251. In a fused operation, the requirements are:

- The commands shall be executed in sequence as an atomic unit. The controller shall behave as if no other operations have been executed between these two commands;
- The operation ends at the point an error is encountered in either command. If the first command in the sequence failed, then the second command in the sequence shall be aborted. If the second command in the sequence failed, then the completion status of the first command is sequence specific;
- The LBA range, if used, shall be the same for the two commands. If the LBA ranges do not match, the commands should be aborted with status of Invalid Field in Command;
- The commands shall be inserted next to each other in the same Submission Queue. If the first command is in the last slot in the Submission Queue, then the second command shall be the first slot in the Submission Queue as part of wrapping around. The Submission Queue Tail doorbell pointer update shall indicate both commands as part of one doorbell update;
- To abort the fused operation, the host shall submit an Abort command separately for each of the commands; and
- A completion queue entry is posted by the controller for each of the commands.

Whether a command is part of a fused operation is indicated in the Fused Operation (FUSE) field of Command Dword 0 shown in Figure 105. The FUSE field also indicates whether each command is the first command in the fused operation or the second command in the fused operation. If the FUSE field is set to a non-zero value and the controller does not support the requested fused operation, then the controller should abort the command with a status of Invalid Field in Command.

4.13 Command Arbitration

For NVMe over PCIe implementations, a command is submitted to the controller when a Submission Queue Tail Doorbell write by the host moves the Submission Queue Tail Pointer past the slot containing the corresponding Submission Queue entry. For NVMe over Fabrics implementations, refer to section 1.4.14 in the NVMe over Fabrics specification for the definition of command submission. The controller transfers submitted commands into the controller for subsequent processing using a vendor specific algorithm.

A command is being processed when the controller and/or namespace state is being accessed or modified by the command (e.g., a Feature setting is being accessed or modified or a logical block is being accessed or modified).

A command is completed when a Completion Queue entry for the command has been posted to the corresponding Completion Queue. Upon completion, all controller state and/or namespace state modifications made by that command are globally visible to all subsequently submitted commands.

A candidate command is a submitted command which has been transferred into the controller that the controller deems ready for processing. The controller selects command(s) for processing from the pool of submitted commands for each Submission Queue. The commands that comprise a fused operation shall be processed together and in order by the controller. The controller may select candidate commands for processing in any order. The order in which commands are selected for processing does not imply the order in which commands are completed.

Arbitration is the method used to determine the Submission Queue from which the controller starts processing the next candidate command(s). Once a Submission Queue is selected using arbitration, the Arbitration Burst setting determines the maximum number of commands that the controller may start processing from that Submission Queue before arbitration shall again take place. A fused operation may be considered as one or two commands by the controller.

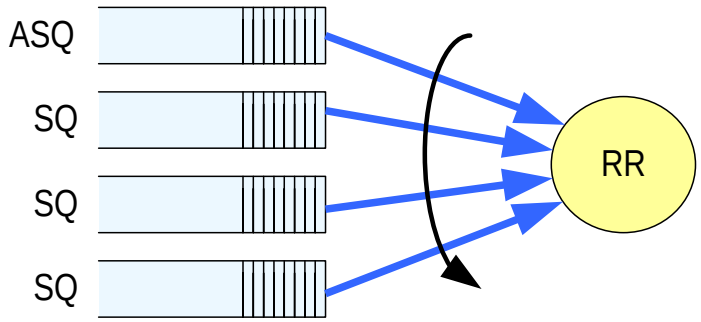
All controllers shall support the round robin command arbitration mechanism. A controller may optionally implement weighted round robin with urgent priority class and/or a vendor specific arbitration mechanism. The Arbitration Mechanism Supported field in the Controller Capabilities register (CC.AMS) indicates optional arbitration mechanisms supported by the controller.

In order to make efficient use of the non-volatile memory, it is often advantageous to execute multiple commands from a Submission Queue in parallel. For Submission Queues that are using weighted round robin with urgent priority class or round robin arbitration, host software may configure an Arbitration Burst setting. The Arbitration Burst setting indicates the maximum number of commands that the controller may launch at one time from a particular Submission Queue. It is recommended that host software configure the Arbitration Burst setting as close to the recommended value by the controller as possible (specified in the Recommended Arbitration Burst field of the Identify Controller data structure in Figure 251), taking into consideration any latency requirements. Refer to section 5.21.1.1.

4.13.1 Round Robin Arbitration

If the round robin arbitration mechanism is selected, the controller shall implement round robin command arbitration amongst all Submission Queues, including the Admin Submission Queue. In this case, all Submission Queues are treated with equal priority. The controller may select multiple candidate commands for processing from each Submission Queue per round based on the Arbitration Burst setting.

Figure 139: Round Robin Arbitration



4.13.2 Weighted Round Robin with Urgent Priority Class Arbitration

In this arbitration mechanism, there are three strict priority classes and three weighted round robin priority levels. If Submission Queue A is of higher strict priority than Submission Queue B, then all candidate commands in Submission Queue A shall start processing before candidate commands from Submission Queue B start processing.

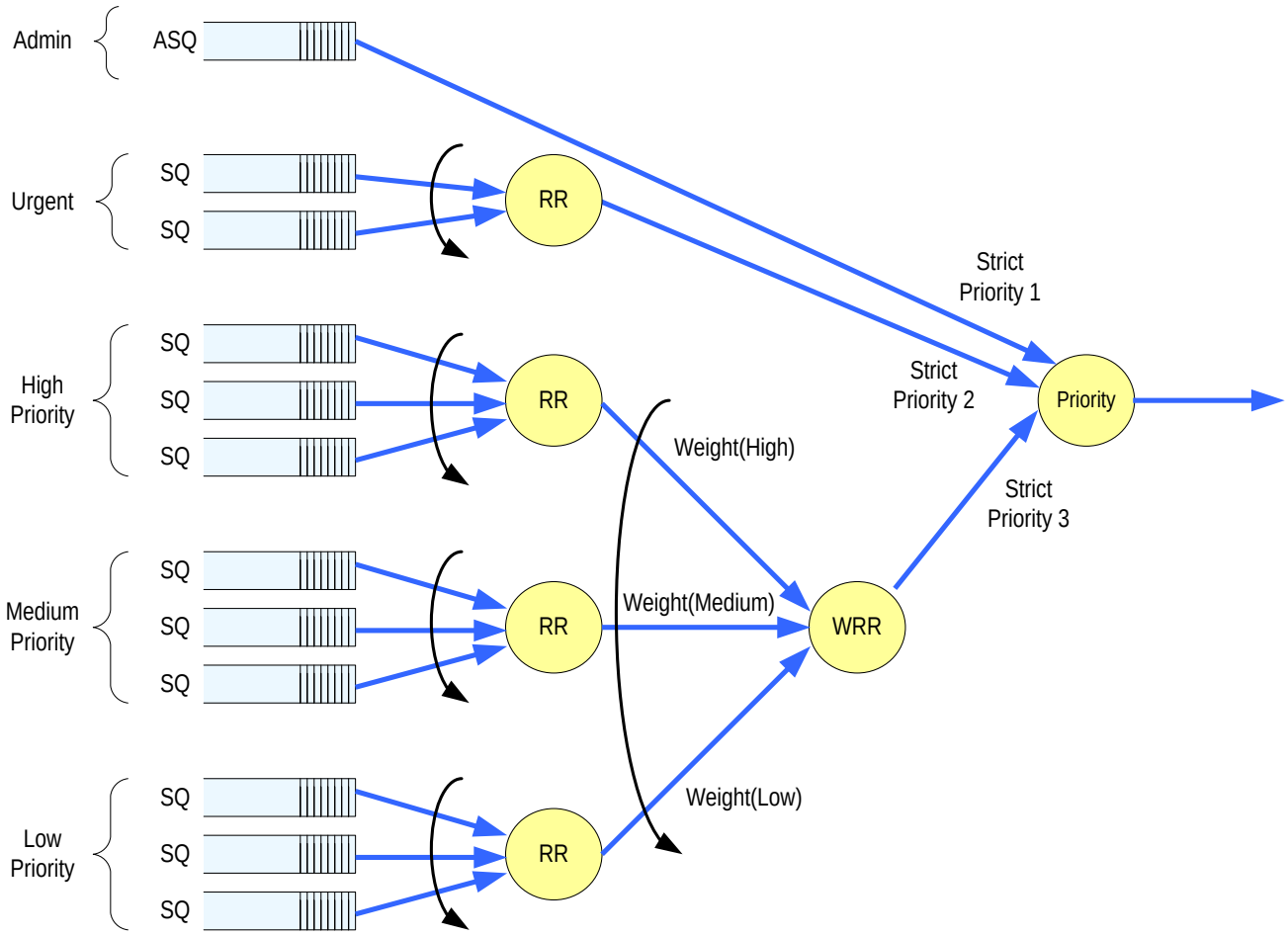
The highest strict priority class is the Admin class that includes any command submitted to the Admin Submission Queue. This class has the highest strict priority above commands submitted to any other Submission Queue.

The next highest strict priority class is the Urgent class. Any I/O Submission Queue assigned to the Urgent priority class is serviced next after commands submitted to the Admin Submission Queue, and before any commands submitted to a weighted round robin priority level. Host software should use care in assigning any Submission Queue to the Urgent priority class since there is the potential to starve I/O Submission Queues in the weighted round robin priority levels as there is no fairness protocol between Urgent and non Urgent I/O Submission Queues.

The lowest strict priority class is the Weighted Round Robin class. This class consists of the three weighted round robin priority levels (High, Medium, and Low) that share the remaining bandwidth using weighted round robin arbitration. Host software controls the weights for the High, Medium, and Low service classes

via the Set Features command. Round robin is used to arbitrate within multiple Submission Queues assigned to the same weighted round robin level. The number of candidate commands that may start processing from each Submission Queue per round is either the Arbitration Burst setting or the remaining weighted round robin credits, whichever is smaller.

Figure 140: Weighted Round Robin with Urgent Priority Class Arbitration



In Figure 140, the Priority decision point selects the highest priority candidate command selected next to start processing.

4.13.3 Vendor Specific Arbitration

A vendor may choose to implement a vendor specific arbitration mechanism. The mechanism(s) are outside the scope of this specification.

5 Admin Command Set

The Admin Command Set defines the commands that may be submitted to the Admin Submission Queue.

The Submission Queue Entry (SQE) structure and the fields that are common to all Admin commands are defined in section 4.2. The Completion Queue Entry (CQE) structure and the fields that are common to all Admin commands are defined in section 4.6. The command specific fields in the SQE and CQE structures (i.e., SQE Command Dwords 10 to 15 and CQE Dword 0) for the Admin Command Set are defined in this section.

Admin commands should not be impacted by the state of I/O queues (e.g., a full I/O Completion Queue should not delay or stall the Delete I/O Submission Queue command).

Figure 141 defines Admin commands while Figure 142 defines I/O Command Set Specific Admin commands that are specific to the NVM Command Set (i.e., NVM Command Set Specific Admin commands). Refer to section 7.1 for mandatory, optional, and prohibited commands for the various controller types.

Figure 141: Opcodes for Admin Commands

Opcode by Field			Combined Opcode [1]	Namespace Identifier Used [2]	Command
(07)	(06:02)	(01:00)			
Generic Command	Function	Data Transfer [3]			
0b	000 00b	00b	00h	No	Delete I/O Submission Queue
0b	000 00b	01b	01h	No	Create I/O Submission Queue
0b	000 00b	10b	02h	Yes	Get Log Page
0b	000 01b	00b	04h	No	Delete I/O Completion Queue
0b	000 01b	01b	05h	No	Create I/O Completion Queue
0b	000 01b	10b	06h	NOTE 6	Identify
0b	000 10b	00b	08h	No	Abort
0b	000 10b	01b	09h	Yes	Set Features
0b	000 10b	10b	0Ah	Yes	Get Features
0b	000 11b	00b	0Ch	No	Asynchronous Event Request
0b	000 11b	01b	0Dh	Yes	Namespace Management
0b	001 00b	00b	10h	No	Firmware Commit
0b	001 00b	01b	11h	No	Firmware Image Download
0b	001 01b	00b	14h	Yes	Device Self-test
0b	001 01b	01b	15h	Yes [4]	Namespace Attachment
0b	001 10b	00b	18h	No	Keep Alive
0b	001 10b	01b	19h	Yes [5]	Directive Send
0b	001 10b	10b	1Ah	Yes [5]	Directive Receive
0b	001 11b	00b	1Ch	No	Virtualization Management
0b	001 11b	01b	1Dh	No	NVMe-MI Send
0b	001 11b	10b	1Eh	No	NVMe-MI Receive
0b	111 11b	00b	7Ch	No	Doorbell Buffer Config
0b	111 11b	11b	7Fh	Refer to the NVMe over Fabrics specification.	
	I/O Command Set Specific				
1b	n/a	NOTE 3	80h to BFh		I/O Command Set specific

Figure 141: Opcodes for Admin Commands

Opcode by Field			Combined Opcode [1]	Namespace Identifier Used [2]	Command
(07)	(06:02)	(01:00)			
Generic Command	Function	Data Transfer [3]			
	Vendor Specific				
1b	n/a	NOTE 3	C0h to FFh		Vendor specific

NOTES:
1. Opcodes not listed are reserved.
2. A subset of commands use the Namespace Identifier (NSID) field. If the Namespace Identifier field is used, then the value FFFFFFFFh is supported in this field unless otherwise indicated in footnotes in this figure that a specific command does not support that value or supports that value only under specific conditions. When this field is not used, the field is cleared to 0h as described in Figure 106.
3. Indicates the data transfer direction of the command. All options to the command shall transfer data as specified or transfer no data. All commands, including vendor specific commands, shall follow this convention: 00b = no data transfer; 01b = host to controller; 10b = controller to host; 11b = bidirectional.
4. This command does not support the use of the Namespace Identifier (NSID) field set to FFFFFFFFh.
5. Support for the Namespace Identifier field set to FFFFFFFFh depends on the Directive Operation (refer to section 9).
6. Use of the Namespace Identifier field depends on the CNS value in the Identify Command as described in Figure 248.

Figure 142: Opcodes for Admin Commands – NVM Command Set Specific

Opcode (07)	Opcode (06:02)	Opcode (01:00)	Opcode [1]	Namespace Identifier Used [2]	Command
Generic Command	Function	Data Transfer [3]			
1b	000 00b	00b	80h	Yes	Format NVM
1b	000 00b	01b	81h	NOTE 4	Security Send
1b	000 00b	10b	82h	NOTE 4	Security Receive
1b	000 01b	00b	84h	No	Sanitize
1b	000 01b	10b	86h	NOTE 5	Get LBA Status

NOTES:
1. NVM Command Set Specific opcodes not listed are reserved.
2. A subset of commands use the Namespace Identifier (NSID) field. If the Namespace Identifier field is used, then unless otherwise specified, the value FFFFFFFFh is supported in this field. When this field is not used, the field is cleared to 0h as described in Figure 106.
3. Indicates the data transfer direction of the command. All options to the command shall transfer data as specified or transfer no data. All commands, including vendor specific commands, shall follow this convention: 00b = no data transfer; 01b = host to controller; 10b = controller to host; 11b = bidirectional.
4. The use of the Namespace Identifier is Security Protocol specific.
5. This command does not support the use of the Namespace Identifier (NSID) field set to FFFFFFFFh.

5.1 Abort command

The Abort command is used to abort a specific command previously submitted to the Admin Submission Queue or an I/O Submission Queue. An Abort command is a best effort command; the command to abort may have already completed, currently be in execution, or may be deeply queued.

To abort a large number of commands (e.g., a larger number of commands than the limit listed in the ACL field), the host should follow the procedures described in section 7.3.3 to delete the I/O Submission Queue and recreate the I/O Submission Queue.

The Abort command uses the Command Dword 10 field. All other command specific fields are reserved.

The Abort Command Limit field in the Identify Controller data structure (refer to Figure 251) indicates the controller limit on concurrent execution of Abort commands. A host should not allow the number of outstanding Abort commands to exceed this value. The controller may complete any excess Abort commands with Abort Command Limit Exceeded status.

Figure 143: Abort – Command Dword 10

Bits	Description
31:16	**Command Identifier (CID):** This field specifies the command identifier of the command to be aborted, that was specified in the CDW0.CID field within the command itself.
15:00	**Submission Queue Identifier (SQID):** This field specifies the identifier of the Submission Queue that the command to be aborted is associated with.

5.1.1 Command Completion

Upon completion of the Abort command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the Abort command and indicating whether the command to abort was aborted. Dword 0 of the completion queue entry indicates whether the command to abort was aborted.

If the command to abort was successfully aborted, then a completion queue entry for the aborted command shall be posted to the appropriate Admin or I/O Completion Queue with a status of Command Abort Requested before the completion queue entry for the Abort command is posted to the Admin Completion Queue, and bit 0 of Dword 0 shall be cleared to ‘0’ in the completion queue entry for the Abort command. If the command to abort was not aborted for any reason, then bit 0 of Dword 0 shall be set to ‘1’ in the completion queue entry for the Abort command.

Command specific status values associated with the Abort command are defined in Figure 144.

Figure 144: Abort – Command Specific Status Values

Value	Description
3h	**Abort Command Limit Exceeded:** The number of concurrently outstanding Abort commands has exceeded the limit indicated in the Identify Controller data structure.

5.2 Asynchronous Event Request command

Asynchronous events are used to notify host software of status, error, and health information as these events occur. To enable asynchronous events to be reported by the controller, host software needs to submit one or more Asynchronous Event Request commands to the controller. The controller specifies an event to the host by completing an Asynchronous Event Request command. Host software should expect that the controller may not execute the command immediately; the command should be completed when there is an event to be reported.

The Asynchronous Event Request command is submitted by host software to enable the reporting of asynchronous events from the controller. This command has no timeout. The controller posts a completion queue entry for this command when there is an asynchronous event to report to the host. If Asynchronous Event Request commands are outstanding when the controller is reset, then each of those commands is aborted and should not return a CQE.

All command specific fields are reserved.

Host software may submit multiple Asynchronous Event Request commands to reduce event reporting latency. The total number of simultaneously outstanding Asynchronous Event Request commands is limited by the Asynchronous Event Request Limit specified in the Identify Controller data structure in Figure 251.

Asynchronous events are grouped into event types. The event type is indicated in the Asynchronous Event Type field in Dword 0 of the completion queue entry for the Asynchronous Event Request command. When

the controller posts a completion queue entry for an outstanding Asynchronous Event Request command and thus reports an asynchronous event, subsequent events of that event type are automatically masked by the controller until the host clears that event. An event is cleared by reading the log page associated with that event using the Get Log Page command (refer to section 5.14).

The following event types are defined:

a) **Error event:** Indicates a general error that is not associated with a specific command (refer to Figure 147). To clear this event, host software reads the Error Information log (refer to section 5.14.1.1) using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0';
b) **SMART / Health Status event:** Indicates a SMART or health status event (refer to Figure 148). To clear this event, host software reads the SMART / Health Information log (refer to section 5.14.1.2) using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0'. The SMART / Health conditions that trigger asynchronous events may be configured in the Asynchronous Event Configuration feature using the Set Features command (refer to section 5.21);
c) **Notice event:** Indicates a general event (refer to Figure 149). To clear this event, host software reads the appropriate log page as described in Figure 149. The conditions that trigger asynchronous events may be configured in the Asynchronous Event Configuration feature using the Set Features command (refer to section 5.21.1.11). These notice events include:
   A. Namespace Attribute Changed;
   B. Firmware Activation Starting;
   C. Telemetry Log Changed;
   D. Asymmetric Namespace Access Change;
   E. Predictable Latency Event Aggregate Log Change;
   F. LBA Status Information Alert; and
   G. Endurance Group Event Aggregate Log Page Change;
d) **NVM Command Set Specific events:** Events that are defined by an I/O command set:
   A. **Reservation Log Page Available event:** Indicates that one or more Reservation Notification log pages (refer to section 5.14.1.16.1) are available. To clear this event, host software reads the Reservation Notification log page using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0';
   B. **Sanitize Operation Completed event:** Indicates that a sanitize operation has completed (including any associated additional media modification, refer to the No-Deallocate Modifies Media After Sanitize field in Figure 251) without unexpected deallocation of all logical blocks (refer to section 5.21.1.23) and status is available in the Sanitize Status log page (refer to section 5.14.1.16.2). To clear this event, host software reads the Sanitize Status log page using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0'; and
   C. **Sanitize Operation Completed With Unexpected Deallocation event:** Indicates that a sanitize operation has completed with unexpected deallocation of all LBAs (refer to section 5.21.1.23) and status is available in the Sanitize Status log page (refer to section 5.14.1.16.2). To clear this event, host software reads the Sanitize Status log page using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0';

   and
e) **Vendor Specific event:** Indicates a vendor specific event. To clear this event, host software reads the indicated vendor specific log page using the Get Log Page command with the Retain Asynchronous Event bit cleared to '0'.

The Sanitize Operation Completed With Unexpected Deallocation asynchronous event shall be supported if the controller supports the Sanitize Config feature (refer to section 5.21.1.23).

Asynchronous events are reported due to a new entry being added to a log page (e.g., Error Information log) or a status update (e.g., status in the SMART / Health log). A status change may be permanent (e.g., the media has become read only) or transient (e.g., the temperature reached or exceeded a threshold for a period of time). Host software should modify the event threshold or mask the event for transient and permanent status changes before issuing another Asynchronous Event Request command to avoid repeated reporting of asynchronous events.

If an event occurs for which reporting is enabled and there are no Asynchronous Event Request commands outstanding, the controller should retain the event information for that Asynchronous Event Type and use that information as a response to the next Asynchronous Event Request command that is received. If a Get Log Page command clears the event prior to receiving the Asynchronous Event Request command or if a power off condition occurs, then a notification is not sent. If multiple events of the same type occur that have identical responses to the Asynchronous Event Request command, then those events may be reported as a single response to an Asynchronous Event Request command. If multiple events occur that are of different types, then the controller should retain a queue of those events for reporting in responses to subsequent Asynchronous Event Request commands.

5.2.1 Command Completion

A completion queue entry is posted to the Admin Completion Queue if there is an asynchronous event to report to the host. Command specific status values associated with Asynchronous Event Request are defined in Figure 145.

Figure 145: Status Code – Command Specific Status Values

Value	Description
05h	**Asynchronous Event Request Limit Exceeded:** The number of concurrently outstanding Asynchronous Event Request commands has been exceeded.

Dword 0 of the completion queue entry contains information about the asynchronous event. The definition of Dword 0 of the completion queue entry is in Figure 146.

Figure 146: Asynchronous Event Request – Completion Queue Entry Dword 0

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:24</td><td>Reserved</td></tr>
<tr><td>23:16</td><td>Log Page Identifier: Indicates the log page associated with the asynchronous event. This log page needs to be read by the host to clear the event.</td></tr>
<tr><td>15:08</td><td>Asynchronous Event Information: Refer to Figure 147, Figure 148, Figure 149, and Figure 150 for detailed information regarding the asynchronous event.</td></tr>
<tr><td>07:03</td><td>Reserved</td></tr>
<tr><td>02:00</td><td>Asynchronous Event Type: Indicates the event type of the asynchronous event. More specific information on the event is provided in the Asynchronous Event Information field.
<table>
<tr><th>Value</th><th>Definition</th><th>Reference</th></tr>
<tr><td>000b</td><td>Error status</td><td>Figure 147</td></tr>
<tr><td>001b</td><td>SMART / Health status</td><td>Figure 148</td></tr>
<tr><td>010b</td><td>Notice</td><td>Figure 149</td></tr>
<tr><td>011b to 101b</td><td>Reserved</td><td>-</td></tr>
<tr><td>110b</td><td>I/O Command Set specific status</td><td>Figure 150</td></tr>
<tr><td>111b</td><td>Vendor specific</td><td>-</td></tr>
</table></td></tr>
</table>

The information in either Figure 147, Figure 148, Figure 149, or Figure 150 is returned in the Asynchronous Event Information field, depending on the Asynchronous Event Type.

Figure 147: Asynchronous Event Information – Error Status

Value	Description
00h	**Write to Invalid Doorbell Register:** Host software wrote the doorbell of a queue that was not created.

Figure 147: Asynchronous Event Information – Error Status

Value	Description
01h	**Invalid Doorbell Write Value:** Host software attempted to write an invalid doorbell value. Some possible causes of this error are: • the value written was out of range of the corresponding queue's base address and size; • the value written is the same as the previously written doorbell value; • the number of commands that would be added as part of a doorbell write would exceed the number of available entries; • host software attempts to add a command to a full Submission Queue; and • host software attempts to remove a completion queue entry from an empty Completion Queue.
02h	**Diagnostic Failure:** A diagnostic failure was detected. This may include a self test operation.
03h	**Persistent Internal Error:** A failure occurred that is persistent and the controller is unable to isolate to a specific set of commands. If this error is indicated, then the CSTS.CFS bit may be set to '1' and the host should perform a reset as described in section 7.3.
04h	**Transient Internal Error:** A transient error occurred that is specific to a particular set of commands; controller operation may continue without a reset.
05h	**Firmware Image Load Error:** The firmware image could not be loaded. The controller reverted to the previously active firmware image or a baseline read-only firmware image.
06h to FFh	Reserved

Figure 148: Asynchronous Event Information – SMART / Health Status

Value	Description
00h	**NVM subsystem Reliability:** NVM subsystem reliability has been compromised. This may be due to significant media errors, an internal error, the media being placed in read only mode, or a volatile memory backup device failing. This status value shall not be used if the read-only condition on the media is due to a change in the write protection state of a namespace (refer to section 8.19.1).
01h	**Temperature Threshold:** A temperature is greater than or equal to an over temperature threshold or less than or equal to an under temperature threshold (refer to section 5.21.1.4).
02h	**Spare Below Threshold:** Available spare capacity has fallen below the threshold.
03h to FFh	Reserved

Figure 149: Asynchronous Event Information – Notice

Value	Description
00h	**Namespace Attribute Changed:** Indicates a change to one or both of the following: • the Identify Namespace data structure (refer to Figure 249) for one or more namespaces; or • the Namespace List returned when the Identify command is issued with the CNS field set to 02h. To clear this event, host software issues a Get Log Page command for the Changed Namespace List log page (Log Identifier 04h - refer to section 5.14.1.4) with the Retain Asynchronous Event bit cleared to '0'. A controller shall not send this event if: a) Namespace Utilization (refer to Figure 249) has changed, as this is a frequent event that does not require action by the host; b) the ANAGRPID field (refer to Figure 249) has changed; or c) capacity information (i.e., the NUSE field and the NVMCAP field) returned in the Identify Namespace data structure (refer to Figure 249) changed as a result of an ANA state change. A controller shall only send this event for changes to the Format Progress Indicator field when bits 6:0 of that field transition from a non-zero value to 0h, or from 0h to a non-zero value.

Figure 149: Asynchronous Event Information – Notice

Value	Description
01h	**Firmware Activation Starting:** The controller is starting a firmware activation process during which command processing is paused. Host software may use CSTS.PP to determine when command processing has resumed. To clear this event, host software reads the Firmware Slot Information log page.
02h	**Telemetry Log Changed:** The controller has saved the controller internal state in the Telemetry Controller-Initiated log page and set the Telemetry Controller-Initiated Data Available field to 1h in that log page. To clear this event, the host issues a Get Log Page command with Retain Asynchronous Event bit cleared to '0' for the Telemetry Controller-Initiated log.
03h	**Asymmetric Namespace Access Change:** The Asymmetric Namespace Access information (refer to section 5.14.1.12) related to an ANA Group that contains namespaces attached to this controller has changed (e.g., an ANA state has changed, an ANAGRPID has changed). The current Asymmetric Namespace Access information for attached namespaces is indicated in the Asymmetric Namespace Access log page (refer to section 5.14.1.12). To clear this event, the host issues a Get Log Page with the Retain Asynchronous Event bit cleared to '0' for the Asymmetric Namespace Access log. A controller shall not send this event if a Namespace Attribute Changed notice is sent for the same event, such as a change due to: a) the attachment of a namespace (refer to to section 5.19); b) the deletion of a namespace (refer to section 5.20); or c) the detachment of a namespace (refer to section 5.19).
04h	**Predictable Latency Event Aggregate Log Change:** Indicates that event pending entries for one or more NVM Sets (refer to section 5.14.1.11) have been added to the Predictable Latency Event Aggregate log.
05h	**LBA Status Information Alert:** The criteria for generating an LBA Status Information Alert Notice event have been met (refer to section 8.22). Information about Potentially Unrecoverable LBAs is available in the LBA Status Information log page (refer to section 5.14.1.14). To clear this event, the host issues a Get Log Page command with Retain Asynchronous Event bit cleared to '0' for the LBA Status Information log.
06h	**Endurance Group Event Aggregate Log Page Change:** Indicates that event entries for one or more Endurance Groups (refer to section 5.14.1.9) have been added to the Endurance Group Event Aggregate log. To clear this event, the host issues a Get Log Page command with the Retain Asynchronous Event bit cleared to '0' for the Endurance Group Event Aggregate log.
07h to EFh	Reserved
F0h to FFh	Refer to the NVMe over Fabrics specification

Figure 150: Asynchronous Event Information – NVM Command Set Specific Status

Value	Description
00h	**Reservation Log Page Available:** Indicates that one or more Reservation Notification log pages (refer to section 5.14.1.16.1) have been added to the Reservation Notification log.
01h	**Sanitize Operation Completed:** Indicates that a sanitize operation has completed (including any associated additional media modification, refer to the No-Deallocate Modifies Media After Sanitize field in Figure 251) without unexpected deallocation of all logical blocks (refer to section 5.21.1.23) and status is available in the Sanitize Status log page (refer to section 5.14.1.16.2).
02h	**Sanitize Operation Completed With Unexpected Deallocation:** Indicates that a sanitize operation for which No-Deallocate After Sanitize (refer to Figure 334) was requested has completed with the unexpected deallocation of all logical blocks (refer to section 5.21.1.23) and status is available in the Sanitize Status log page (refer to section 5.14.1.16.2).
03h to FFh	Reserved

5.3 Create I/O Completion Queue command

The Create I/O Completion Queue command is used to create all I/O Completion Queues with the exception of the Admin Completion Queue. The Admin Completion Queue is created by specifying its base address in the ACQ register. If a PRP List is provided to describe the CQ, then the PRP List shall be maintained by host software at the same location in host physical memory and the values in the PRP List shall not be modified until the corresponding Delete I/O Completion Queue command for this CQ is completed successfully or the controller is reset. If the PRP List values are modified, the behavior is undefined.

The Create I/O Completion Queue command uses the PRP Entry 1, Command Dword 10, and Command Dword 11 fields. All other command specific fields are reserved.

Figure 151: Create I/O Completion Queue – PRP Entry 1

Bits	Description
63:00	**PRP Entry 1 (PRP1):** If CDW11.PC is set to '1', then this field specifies a 64-bit base memory address pointer of the Completion Queue that is physically contiguous. The address pointer is memory page aligned (based on the value in CC.MPS) unless otherwise specified. If CDW11.PC is cleared to '0', then this field specifies a PRP List pointer that describes the list of pages that constitute the Completion Queue. The list of pages is memory page aligned (based on the value in CC.MPS) unless otherwise specified. In both cases the PRP Entry shall have an offset of 0h. In a non-contiguous Completion Queue, each PRP Entry in the PRP List shall have an offset of 0h. If there is a PRP Entry with a non-zero offset, then the controller should return an error of PRP Offset Invalid.

Figure 152: Create I/O Completion Queue – Command Dword 10

Bits	Description
31:16	**Queue Size (QSIZE):** This field indicates the size of the Completion Queue to be created. If the size is 0h or larger than the controller supports, the controller should return an error of Invalid Queue Size. Refer to section 4.1.3. This is a 0's based value.
15:00	**Queue Identifier (QID):** This field indicates the identifier to assign to the Completion Queue to be created. This identifier corresponds to the Completion Queue Head Doorbell used for this command (i.e., the value *y* in section 3.1.26). This value shall not exceed the value reported in the Number of Queues feature (refer to section 5.21.1.7) for I/O Completion Queues. If the value specified is 0h, exceeds the Number of Queues reported, or corresponds to an identifier already in use, the controller should return an error of Invalid Queue Identifier.

Figure 153: Create I/O Completion Queue – Command Dword 11

Bits	Description
31:16	**Interrupt Vector (IV):** This field indicates interrupt vector to use for this Completion Queue. This corresponds to the MSI-X or multiple message MSI vector to use. If using single message MSI or pin-based interrupts, then this field shall be cleared to 0h. In MSI-X, a maximum of 2,048 vectors are used. This value shall not be set to a value greater than the number of messages the controller supports (refer to MSICAP.MC.MME or MSIXCAP.MXC.TS). If the value is greater than the number of messages the controller supports, the controller should return an error of Invalid Interrupt Vector.
15:02	Reserved
01	**Interrupts Enabled (IEN):** If set to '1', then interrupts are enabled for this Completion Queue. If cleared to '0', then interrupts are disabled for this Completion Queue.

Figure 153: Create I/O Completion Queue – Command Dword 11

Bits	Description
00	**Physically Contiguous (PC):** If set to '1', then the Completion Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Completion Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If this bit is cleared to '0' and CAP.CQR is set to '1', then the controller should return an error of Invalid Field in Command. If the: • queue is located in the Controller Memory Buffer; • PC is cleared to '0'; and • CMBLOC.CQPDS is cleared to '0', then the controller shall abort the command with Invalid Use of Controller Memory Buffer status.

5.3.1 Command Completion

If the command is completed, then the controller shall post a completion queue entry to the Admin Completion Queue indicating the status for the command.

Create I/O Completion Queue command specific status values are defined in Figure 154.

Figure 154: Create I/O Completion Queue – Command Specific Status Values

Value	Description
1h	**Invalid Queue Identifier:** The creation of the I/O Completion Queue failed due to an invalid queue identifier specified as part of the command. An invalid queue identifier is one that identifies the Admin Queue (i.e., 0h), is outside the range supported by the controller, or is a Completion Queue Identifier that is already in use.
2h	**Invalid Queue Size:** The host attempted to create an I/O Completion Queue: • with an invalid number of entries (e.g., a value of 0h or a value which exceeds the maximum supported by the controller, specified in CAP.MQES); or • before initializing the CC.IOCQES field.
8h	**Invalid Interrupt Vector:** The creation of the I/O Completion Queue failed due to an invalid interrupt vector specified as part of the command.

5.4 Create I/O Submission Queue command

The Create I/O Submission Queue command is used to create I/O Submission Queues. The Admin Submission Queue is created by specifying its base address in the ASQ register. If a PRP List is provided to describe the SQ to be created, then the PRP List shall be maintained by host software at the same location in host physical memory and the values in the PRP List shall not be modified until the corresponding Delete I/O Submission Queue command for that SQ is completed or the controller is reset. If the PRP List values are modified, the behavior is undefined.

The Create I/O Submission Queue command uses the PRP Entry 1, Command Dword 10, Command Dword 11, and Command Dword 12 fields. All other command specific fields are reserved.

Figure 155: Create I/O Submission Queue – PRP Entry 1

Bits	Description
63:00	**PRP Entry 1 (PRP1):** If CDW11.PC is set to '1', then this field specifies a 64-bit base memory address pointer of the Submission Queue that is physically contiguous. The address pointer is memory page aligned (based on the value in CC.MPS) unless otherwise specified. If CDW11.PC is cleared to '0', then this field specifies a PRP List pointer that describes the list of pages that constitute the Submission Queue. The list of pages is memory page aligned (based on the value in CC.MPS) unless otherwise specified. In both cases, the PRP Entry shall have an offset of 0h. In a non-contiguous Submission Queue, each PRP Entry in the PRP List shall have an offset of 0h. If there is a PRP Entry with a non-zero offset, then the controller should return an error of PRP Offset Invalid.

Figure 156: Create I/O Submission Queue – Command Dword 10

Bits	Description
31:16	**Queue Size (QSIZE):** This field indicates the size of the Submission Queue to be created. If the size is 0h or larger than the controller supports, the controller should return an error of Invalid Queue Size. Refer to section 4.1.3. This is a 0's based value.
15:00	**Queue Identifier (QID):** This field indicates the identifier to assign to the Submission Queue to be created. This identifier corresponds to the Submission Queue Tail Doorbell used for this command (i.e., the value *y* in section 3.1.25). This value shall not exceed the value reported in the Number of Queues feature (refer to section 5.21.1.7) for I/O Submission Queues. If the value specified is 0h, exceeds the Number of Queues reported, or corresponds to an identifier already in use, the controller should return an error of Invalid Queue Identifier.

Figure 157: Create I/O Submission Queue – Command Dword 11

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:16</td><td>Completion Queue Identifier (CQID): This field indicates the identifier of the I/O Completion Queue to utilize for any command completions entries associated with this Submission Queue.

If the value specified:
a) is 0h (i.e., the Admin Completion Queue), then the controller should return an error of Invalid Queue Identifier;
b) is outside the range supported by the controller, then the controller should return an error of Invalid Queue Identifier; or
c) is within the range supported by the controller and does not identify an I/O Completion Queue that has been created, then the controller should return an error of Completion Queue Invalid.</td></tr>
<tr><td>15:03</td><td>Reserved</td></tr>
<tr><td>02:01</td><td>Queue Priority (QPRIO): This field indicates the priority class to use for commands within this Submission Queue. This field is only used when the weighted round robin with urgent priority class is the arbitration mechanism selected, the field is ignored if weighted round robin with urgent priority class is not used. Refer to section 4.13.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>Urgent</td></tr>
<tr><td>01b</td><td>High</td></tr>
<tr><td>10b</td><td>Medium</td></tr>
<tr><td>11b</td><td>Low</td></tr>
</table>
</td></tr>
</table>

Figure 157: Create I/O Submission Queue – Command Dword 11

Bits	Description
00	**Physically Contiguous (PC):** If set to '1', then the Submission Queue is physically contiguous and PRP Entry 1 (PRP1) is the address of a contiguous physical buffer. If cleared to '0', then the Submission Queue is not physically contiguous and PRP Entry 1 (PRP1) is a PRP List pointer. If this bit is cleared to '0' and CAP.CQR is set to '1', then the controller should return an error of Invalid Field in Command. If the: • queue is located in the Controller Memory Buffer; • PC is cleared to '0'; and • CMBLOC.CQPDS is cleared to '0', then the controller shall abort the command with Invalid Use of Controller Memory Buffer status.

Figure 158: Create I/O Submission Queue – Command Dword 12

Bits	Description
31:16	Reserved
15:00	**NVM Set Identifier (NVMSETID):** This field indicates the identifier of the NVM Set to be associated with this Submission Queue. If this field is cleared to 0h or the SQ Associations capability is not supported (refer to section 8.23), then this Submission Queue is not associated with any specific NVM Set. If this field is set to a non-zero value that is not specified in the NVM Set List (refer to Figure 254) and the SQ Associations feature is supported (refer to section 8.23), then the controller shall abort the command with a status code of Invalid Field in Command. The host should not submit commands for namespaces associated with other NVM Sets in this Submission Queue (refer to section 8.23).

5.4.1 Command Completion

Upon completion of the Create I/O Submission Queue command, the controller posts a completion queue entry to the Admin Completion Queue.

Create I/O Submission Queue command specific status values are defined in Figure 159.

Figure 159: Create I/O Submission Queue – Command Specific Status Values

Value	Description
0h	**Completion Queue Invalid:** The Completion Queue identifier specified in the command has not been created.
1h	**Invalid Queue Identifier:** The creation of the I/O Submission Queue failed due an invalid queue identifier specified as part of the command. An invalid queue identifier is one that identifies the Admin Queue (i.e., 0h), is outside the range supported by the controller, or is a Submission Queue Identifier that is already in use.
2h	**Invalid Queue Size:** The host attempted to create an I/O Submission Queue: • with an invalid number of entries (e.g., a value of 0h or a value which exceeds the maximum supported by the controller, specified in CAP.MQES); or • before initializing the CC.IOSQES field.

5.5 Delete I/O Completion Queue command

The Delete I/O Completion Queue command is used to delete an I/O Completion Queue. The Delete I/O Completion Queue command uses the Command Dword 10 field. All other command specific fields are

reserved. After this command has completed, the PRP List that describes the Completion Queue may be deallocated by host software.

Host software shall ensure that any associated I/O Submission Queue is deleted prior to deleting a Completion Queue. If there are any associated I/O Submission Queues present, then the Delete I/O Completion Queue command shall abort with a status value of Invalid Queue Deletion.

Note: It is not possible to delete the Admin Completion Queue.

Figure 160: Delete I/O Completion Queue – Command Dword 10

Bits	Description
31:16	Reserved
15:00	**Queue Identifier (QID):** This field indicates the identifier of the Completion Queue to be deleted. The value of 0h (Admin Completion Queue) shall not be specified.

5.5.1 Command Completion

Upon completion of the Delete I/O command, the controller posts a completion queue entry to the Admin Completion Queue. Delete I/O Completion Queue command specific status values are defined in Figure 161.

Figure 161: Delete I/O Completion Queue – Command Specific Status Values

Value	Description
01h	**Invalid Queue Identifier:** The Queue Identifier specified in the command is invalid. This error is also indicated if the Admin Completion Queue identifier is specified.
0Ch	**Invalid Queue Deletion:** This error indicates that it is invalid to delete the I/O Completion Queue specified. The typical reason for this error condition is that there is an associated I/O Submission Queue that has not been deleted.

5.6 Delete I/O Submission Queue command

The Delete I/O Submission Queue command is used to delete an I/O Submission Queue. The Delete I/O Submission Queue command uses the Command Dword 10 field. All other command specific fields are reserved. After this command has completed, the PRP List that describes the Submission Queue may be deallocated by host software.

Upon successful completion of the Delete I/O Submission Queue command, all I/O commands previously submitted to the indicated Submission Queue shall be either explicitly completed or implicitly completed. Prior to returning a completion queue entry for the Delete I/O Submission Queue command, other commands previously submitted to the I/O Submission Queue to be deleted may be completed with appropriate status (e.g., Successful Completion, Command Aborted due to SQ Deletion). After successful completion of the Delete I/O Submission Queue command, the controller shall not post completion status for any I/O commands that were submitted to the deleted I/O Submission Queue. The successful completion of the Delete I/O Submission Queue command indicates an implicit completion status of Command Aborted due to SQ Deletion for any previously submitted I/O commands that did not have a completion queue entry posted by the controller.

Note: It is not possible to delete the Admin Submission Queue.

Figure 162: Delete I/O Submission Queue – Command Dword 10

Bits	Description
31:16	Reserved
15:00	**Queue Identifier (QID):** This field indicates the identifier of the Submission Queue to be deleted. The value of 0h (Admin Submission Queue) shall not be specified.

5.6.1 Command Completion

After all commands submitted to the indicated I/O Submission Queue are either completed or aborted, a completion queue entry is posted to the Admin Completion Queue when the queue has been deleted. Delete I/O Submission Queue command specific status values are defined in Figure 163.

Figure 163: Delete I/O Submission Queue – Command Specific Status Values

Value	Description
1h	**Invalid Queue Identifier:** The Queue Identifier specified in the command is invalid. This error is also indicated if the Admin Submission Queue identifier is specified.

5.7 Doorbell Buffer Config command

The Doorbell Buffer Config command is used to provide two separate memory buffers that mirror the controller's doorbell registers defined in section 3. This command is intended for emulated controllers and is not typically supported by a physical NVMe controller. The two buffers are known as “Shadow Doorbell” and “EventIdx”, respectively. Refer to section 7.13 for an example of how these buffers may be used.

The Doorbell Buffer Config command uses the PRP Entry 1 and PRP Entry 2 fields. All other command specific fields are reserved. The command is not namespace specific, does not support metadata, and does not support SGLs. The settings are not retained across a Controller Level Reset.

Each buffer supplied with the Doorbell Buffer Config command shall be a single physical memory page as defined by the CC.MPS field. The controller shall ensure that the following condition is satisfied:

(4 << CAP.DSTRD) * (max(NSQA, NCQA)+1) <= (2^(12+CC.MPS))

Figure 164: Doorbell Buffer Config – Shadow Doorbell and EventIdx

Start (Offset in Buffer)[1, 2]	End (Offset in Buffer)[1, 2]	Description [2]
00h	03h	Submission Queue 0 Tail Doorbell or EventIdx (Admin)
00h + (1 * (4 << CAP.DSTRD))	03h + (1 * (4 << CAP.DSTRD))	Completion Queue 0 Head Doorbell or EventIdx (Admin)
00h + (2 * (4 << CAP.DSTRD))	03h + (2 * (4 << CAP.DSTRD))	Submission Queue 1 Tail Doorbell or EventIdx
00h + (3 * (4 << CAP.DSTRD))	03h + (3 * (4 << CAP.DSTRD))	Completion Queue 1 Head Doorbell or EventIdx
…	…	...
00h + (2y * (4 << CAP.DSTRD))	03h + (2y * (4 << CAP.DSTRD))	Submission Queue y Tail Doorbell or EventIdx
00h + ((2y + 1) * (4 << CAP.DSTRD))	03h + ((2y + 1) * (4 << CAP.DSTRD))	Completion Queue y Head Doorbell or EventIdx

NOTES:
1. The offsets in Start and End are referenced to the value provided in PRP1 for the doorbell buffer and to the value provided in PRP2 for the EventIdx buffer.
2. The value of y is equal to max(NSQA, NCQA).

Figure 165: Doorbell Buffer Config – PRP Entry 1

Bits	Description
63:00	**PRP Entry 1 (PRP1):** This field specifies a 64-bit base memory address pointer to the Shadow Doorbell buffer with the definition specified in Figure 164. The Shadow Doorbell buffer is updated by the host. This buffer shall be memory page aligned.

Figure 166: Doorbell Buffer Config – PRP Entry 2

Bits	Description
63:00	**PRP Entry 2 (PRP2):** This field specifies a 64-bit base memory address pointer to the EventIdx buffer with the definition specified in Figure 164. The EventIdx buffer is updated by the para-virtualized controller. This buffer shall be memory page aligned.

5.7.1 Command Completion

When the command is completed, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command. If the Shadow Doorbell buffer or EventIdx buffer memory addresses are invalid, then a status code of Invalid Field in Command shall be returned.

5.8 Device Self-test command

The Device Self-test command is used to start a device self-test operation or abort a device self-test operation (refer to section 8.11). The Device Self-test command is used specifically to:

a) start a short device self-test operation;
b) start an extended device self-test operation;
c) start a vendor specific device self-test operation; or
d) abort a device self-test operation already in process.

The device self-test operation is performed by the controller that the Device Self-test command was submitted to. The Namespace Identifier field controls which namespaces are included in the device self-test operation as specified in Figure 167.

Figure 167: Device Self-test Namespace Test Action

Value	Description
00000000h	Specifies that the device self-test operation shall not include any namespaces, and only the controller is included as part of the device self-test operation.
00000001h to FFFFFFFEh	Specifies that the device self-test operation shall include the namespace specified by this field. If this field specifies an invalid namespace ID, then the controller shall abort the command with status of Invalid Namespace or Format. If this field specifies an inactive namespace ID, then the controller shall abort the command with status of Invalid Field in Command.
FFFFFFFFh	Specifies that the device self-test operation shall include all active namespaces accessible through the controller at the time the device self-test operation is started.

The Device Self-test command uses the Command Dword 10 field. All other command specific fields are reserved.

Figure 168: Device Self-test – Command Dword 10

Bits	Description
31:04	Reserved

Figure 168: Device Self-test – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>03:00</td><td>Self-test Code (STC): This field specifies the action taken by the Device Self-test command.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Reserved</td></tr>
<tr><td>1h</td><td>Start a short device self-test operation</td></tr>
<tr><td>2h</td><td>Start an extended device self-test operation</td></tr>
<tr><td>3h to Dh</td><td>Reserved</td></tr>
<tr><td>Eh</td><td>Vendor specific</td></tr>
<tr><td>Fh</td><td>Abort device self-test operation</td></tr>
</table></td></tr>
</table>

The processing of a Device Self-test command and interactions with a device self-test operation already in progress is defined in Figure 169.

Figure 169: Device Self-test – Command Processing

<table>
<tr><th>Self-test in Progress[1]</th><th>Self-test Code value in new Drive Self-test command</th><th>Controller Action</th></tr>
<tr><td rowspan="4">Yes</td><td>1h – Short device self-test</td><td rowspan="2">Abort the new Device Self-test command with status Device Self-test in Progress.</td></tr>
<tr><td>2h – Extended device self-test</td></tr>
<tr><td>Eh – Vendor specific</td><td>Vendor specific</td></tr>
<tr><td>Fh – Abort device self-test</td><td>The controller takes the following actions in order:
1. Abort device self-test operation in progress;
2. Create log entry in the Newest Self-test Result Data Structure in the Device Self-test Log;
3. Set the Current Device Self-test Status field in the Device Self-test Log to 0h; and
4. Completes command successfully.</td></tr>
<tr><td rowspan="4">No</td><td>1h – Short device self-test</td><td>The controller takes the following actions in order:
1. Validate the command parameters;
2. Set the Current Device Self-test Status field in the Device Self-test Log to 1h;
3. Start a device self-test operation; and
4. Completes command successfully.</td></tr>
<tr><td>2h – Extended device self-test</td><td>The controller takes the following actions in order:
1. Validate the command parameters;
2. Set the Current Device Self-test Status field in the Device Self-test Log to 2h;
3. Start a device self-test operation; and
4. Completes command successfully.</td></tr>
<tr><td>Eh – Vendor specific</td><td>Vendor specific</td></tr>
<tr><td>Fh – Abort device self-test</td><td>Completes command successfully. The Device Self-test Log is not modified.</td></tr>
<tr><td colspan="3">NOTES:
1. If bit 0 is cleared to ‘0’ in the Device Self-test Options (DSTO) of the Identify Controller data structure (refer to Figure 251), then the Self-test in Progress column represents that a device self-test operation is in progress on the controller that the new Device Self-test command was received on. If bit 0 is set to ‘1’ in the Device Self-test Options (DSTO) of the Identify Controller data structure, then the Self-test in Progress column represents that a device self-test operation is in progress on the NVM subsystem.</td></tr>
</table>

5.8.1 Command Completion

A completion queue entry is posted to the Admin Completion Queue after the appropriate actions are taken as specified in Figure 169. Device Self-test command specific status values are defined in Figure 170.

Figure 170: Device Self-test – Command Specific Status Values

Value	Description
1Dh	**Device Self-test in Progress:** The controller or NVM subsystem already has a device self-test operation in process.

5.9 Directive Receive command

The Directive Receive command returns a data buffer that is dependent on the Directive Type. Refer to section 9.

The Directive Receive command uses the Data Pointer, Command Dword 10, and Command Dword 11 fields. Command Dword 12 and Dword 13 may be used based on the Directive Type field and the Directive Operation field. All other command specific fields are reserved.

If the Number of Dwords (NUMD) field corresponds to a length that is less than the size of the data structure to be returned, then only that specified portion of the data structure is transferred. If the NUMD field corresponds to a length that is greater than the size of the associated data structure, then the entire contents of the data structure are transferred and no additional data is transferred.

Figure 171: Directive Receive – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field.

Figure 172: Directive Receive – Command Dword 10

Bits	Description
31:00	**Number of Dwords (NUMD):** This field specifies the number of dwords to transfer. This is a 0's based value.

Figure 173: Directive Receive – Command Dword 11

Bits	Description
31:16	**Directive Specific (DSPEC):** The interpretation of this field is Directive Type dependent. Refer to section 9.
15:08	**Directive Type (DTYPE):** This field specifies the Directive Type. Refer to Figure 510 for the list of Directive Types.
07:00	**Directive Operation (DOPER):** This field specifies the Directive Operation to perform. The interpretation of this field is Directive Type dependent. Refer to section 9.

5.9.1 Command Completion

When the command is completed, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command. Command specific status values that may be returned are dependent on the Directive Type, refer to section 9.

Directive Receive command specific status values are defined in Figure 174.

Figure 174: Directive Receive – Command Specific Status Value

Value	Description
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).

5.10 Directive Send command

The Directive Send command transfers a data buffer that is dependent on the Directive Type to the controller. Refer to section 9.

The Directive Send command uses the Data Pointer, Command Dword 10, and Command Dword 11 fields. Command Dword 12 and Command Dword 13 may be used based on the Directive Type field and the Directive Operation field. All other command specific fields are reserved.

Figure 175: Directive Send – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field.

Figure 176: Directive Send – Command Dword 10

Bits	Description
31:00	**Number of Dwords (NUMD):** This field specifies the number of dwords to transfer. This is a 0's based value.

Figure 177: Directive Send – Command Dword 11

Bits	Description
31:16	**Directive Specific (DSPEC):** The interpretation of this field is Directive Type dependent. Refer to section 9.
15:08	**Directive Type (DTYPE):** This field specifies the Directive Type. Refer to Figure 510 for the list of Directive Types.
07:00	**Directive Operation (DOPER):** This field specifies the Directive Operation to perform. The interpretation of this field is Directive Type dependent. Refer to section 9.

5.10.1 Command Completion

When the command is completed, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command. Command specific status values that may be returned are dependent on the Directive Type, refer to section 9.

5.11 Firmware Commit command

Note: This command was known in NVM Express revision 1.0 and 1.1 as "Firmware Activate."

The Firmware Commit command is used to modify the firmware image or Boot Partitions.

When modifying a firmware image, the Firmware Commit command verifies that a valid firmware image has been downloaded and commits that revision to a specific firmware slot. The host may select the firmware image to activate on the next Controller Level Reset as part of this command. The host may determine the currently executing firmware revision by examining the Firmware Revision field in the Identify Controller data structure in Figure 251. The host may determine the firmware revision to be executed on

the next Controller Level Reset by examining the Firmware Slot Information log page. All controllers in the NVM subsystem share firmware slots and the same firmware image is applied to all controllers.

Activation of a firmware image may result in a change in controller behavior that is not expected by the host (e.g., an incompatible change in the UUID List (refer to section 8.24.2)). In this case, if the Commit Action field is set to 011b, then the controller shall abort the command with a status of Firmware Activation Requires Conventional Reset.

When modifying Boot Partitions, the host may select the Boot Partition to mark as active or replace. A Boot Partition is only able to be written when unlocked (refer to section 8.13).

The Firmware Commit command uses the Command Dword 10 field. All other command specific fields are reserved.

Figure 178: Firmware Commit – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31</td><td>Boot Partition ID (BPID): Specifies the Boot Partition that shall be used for the Commit Action, if applicable.</td></tr>
<tr><td>30:06</td><td>Reserved</td></tr>
<tr><td>05:03</td><td>Commit Action (CA): This field specifies the action that is taken (refer to section 8.1) on the image downloaded with the Firmware Image Download command or on a previously downloaded and placed image. The actions are indicated in the following table.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>Downloaded image replaces the existing image, if any, in the specified Firmware Slot. The newly placed image is not activated.</td></tr>
<tr><td>001b</td><td>Downloaded image replaces the existing image, if any, in the specified Firmware Slot. The newly placed image is activated at the next Controller Level Reset.</td></tr>
<tr><td>010b</td><td>The existing image in the specified Firmware Slot is activated at the next Controller Level Reset.</td></tr>
<tr><td>011b</td><td>Downloaded image replaces the existing image, if any, in the specified Firmware Slot and is then activated immediately. If there is not a newly downloaded image, then the existing image in the specified firmware slot is activated immediately.</td></tr>
<tr><td>100b to 101b</td><td>Reserved</td></tr>
<tr><td>110b</td><td>Downloaded image replaces the Boot Partition specified by the Boot Partition ID field.</td></tr>
<tr><td>111b</td><td>Mark the Boot Partition specified in the BPID field as active and update BPINFO.ABPID.</td></tr>
</table></td></tr>
<tr><td>02:00</td><td>Firmware Slot (FS): Specifies the firmware slot that shall be used for the Commit Action, if applicable. If the value specified is 0h, then the controller shall choose the firmware slot (i.e., slot 1 to slot 7) to use for the operation.</td></tr>
</table>

5.11.1 Command Completion

Upon completion of the Firmware Commit command, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.

For Firmware Commit commands that specify activation of a new firmware image at the next Controller Level Reset (i.e., the CA field was set to 001b or 010b) and complete with a status code value of 0h (i.e., Success Completion), a Controller Level Reset initiated by any of the methods defined in section 7.3.2 activates the specified firmware.

Firmware Commit command specific status values are defined in Figure 179.

Figure 179: Firmware Commit – Command Specific Status Values

Value	Description
06h	**Invalid Firmware Slot:** The firmware slot indicated is invalid or read only. This error is indicated if the firmware slot exceeds the number supported.
07h	**Invalid Firmware Image:** The firmware image specified for activation is invalid and not loaded by the controller.
0Bh	**Firmware Activation Requires Conventional Reset:** The firmware commit was successful, however, activation of the firmware image requires a Conventional Reset. If an FLR or Controller Reset occurs prior to a Conventional Reset, the controller shall continue operation with the currently executing firmware image.
10h	**Firmware Activation Requires NVM Subsystem Reset:** The firmware commit was successful, however, activation of the firmware image requires an NVM Subsystem Reset. If any other type of Controller Level Reset occurs prior to an NVM Subsystem Reset, the controller shall continue operation with the currently executing firmware image.
11h	**Firmware Activation Requires Controller Level Reset:** The firmware commit was successful; however, the image specified does not support being activated without a Controller Level Reset. The image shall be activated at the next Controller Level Reset. This status code should be returned only if the Commit Action field in the Firmware Commit command is set to 011b (i.e., activate immediately).
12h	**Firmware Activation Requires Maximum Time Violation:** The image specified if activated immediately would exceed the Maximum Time for Firmware Activation (MTFA) value reported in the Identify Controller data structure (refer to Figure 251). To activate the firmware, the Firmware Commit command needs to be re-issued and the image activated using a reset.
13h	**Firmware Activation Prohibited:** The image specified is being prohibited from activation by the controller for vendor specific reasons (e.g., controller does not support down revision firmware).
14h	**Overlapping Range**: This error is indicated if the firmware image has overlapping ranges.
1Eh	**Boot Partition Write Prohibited:** This error is indicated if a command attempts to modify a Boot Partition while locked (refer to section 8.13.3).

5.12 Firmware Image Download command

The Firmware Image Download command is used to download all or a portion of an image for a future update to the controller. The Firmware Image Download command may be submitted while other commands on the Admin Submission Queue or I/O Submission Queues are outstanding. The Firmware Image Download command downloads a new image (in whole or in part) to the controller.

The image may be constructed of multiple pieces that are individually downloaded with separate Firmware Image Download commands. Each Firmware Image Download command includes a Dword Offset and Number of Dwords that specify a dword range. The host software should ensure that image pieces do not have dword ranges that overlap and that the NUMD field and OFST field meet the alignment and granularity requirements indicated in the FWUG field (refer to Figure 251). Firmware portions may be submitted out of order to the controller. Host software shall submit image portions in order when updating a Boot Partition. If ranges overlap, the controller may return an error of Overlapping Range.

The new firmware image is not activated as part of the Firmware Image Download command. Refer to section 8.1 for details on the firmware update process. The firmware update process does not modify the contents of Boot Partitions. Refer to section 8.13.2 for details on the Boot Partition update process.

Host software should not update Boot Partitions and firmware images simultaneously. After downloading an image, host software issues a Firmware Commit command before downloading another image. Processing of the first Firmware Image Download command after completion of a Firmware Commit command shall cause the controller to discard all remaining portion(s), if any, of downloaded images. If a reset occurs between a firmware download and completion of the Firmware Commit command, then the controller shall discard all portion(s), if any, of downloaded images.

The Firmware Image Download command uses the Data Pointer, Command Dword 10, and Command Dword 11 fields. All other command specific fields are reserved.

Figure 180: Firmware Image Download – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the location where data should be transferred from. Refer to Figure 106 for the definition of this field.

Figure 181: Firmware Image Download – Command Dword 10

Bits	Description
31:00	**Number of Dwords (NUMD):** This field specifies the number of dwords to transfer for this portion of the firmware. This is a 0's based value. If the value specified in this field does not meet the requirement indicated by the FWUG field (refer to Figure 251), the firmware update may abort with status of Invalid Field in Command.

Figure 182: Firmware Image Download – Command Dword 11

Bits	Description
31:00	**Offset (OFST):** This field specifies the number of dwords offset from the start of the firmware image being downloaded to the controller. The offset is used to construct the complete firmware image when the firmware is downloaded in multiple pieces. The piece corresponding to the start of the firmware image shall have an Offset of 0h. If the value specified in this field does not meet the requirement indicated by the FWUG field (refer to Figure 251), the firmware update may fail with status of Invalid Field in Command.

5.12.1 Command Completion

Upon completion of the Firmware Image Download command, the controller posts a completion queue entry to the Admin Completion Queue. Firmware Image Download command specific status values are defined in Figure 183.

Figure 183: Firmware Image Download – Command Specific Status Values

Value	Description
14h	**Overlapping Range:** This error is indicated if the firmware image has overlapping ranges. This error may indicate that the granularity or alignment of the firmware image downloaded does not conform to the Firmware Update Granularity field indicated in the Identify Controller data structure.

5.13 Get Features command

The Get Features command retrieves the attributes of the Feature specified.

The Get Features command uses the Data Pointer, Command Dword 10, and Command Dword 14 fields. The use of Command Dword 11 fields is Feature specific. If not used by a Feature, then Command Dword 11 is reserved unless otherwise stated. All other command specific fields are reserved.

Figure 184: Get Features – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field. If no data structure is used as part of this specified feature, then this field is ignored.

Figure 185: Get Features – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:11</td><td>Reserved</td></tr>
<tr><td>10:08</td><td>Select (SEL): This field specifies which value of the attributes to return in the provided data:

<table><tr><th>Select</th><th>Description</th></tr><tr><td>000b</td><td>Current</td></tr><tr><td>001b</td><td>Default</td></tr><tr><td>010b</td><td>Saved</td></tr><tr><td>011b</td><td>Supported Capabilities</td></tr><tr><td>100b to 111b</td><td>Reserved</td></tr></table>
Refer to section 5.13.1 and section 7.8 for details on the value returned in each case.

The controller indicates in bit 4 of the Optional NVM Command Support field of the Identify Controller data structure in Figure 251 whether this field is supported.

If a Get Features command is received with the Select field set to 010b (i.e., saved) and the controller does not support the Feature Identifier being saved or does not currently have any saved values, then the controller shall operate as if the Select field is set to 001b (i.e., default).</td></tr>
<tr><td>07:00</td><td>Feature Identifier (FID): This field specifies the identifier of the Feature for which to provide data.</td></tr>
</table>

If the controller supports selection of a UUID by the Get Features command (refer to Figure 275 and section 8.24) and the controller supports selection of a UUID for the specified vendor specific feature identifier (refer to Figure 275), then Command Dword 14 is used to specify a UUID Index value (refer to Figure 186). If the controller does not support selection of a UUID by the Get Features command or the controller does not support selection of a UUID for the specified vendor specific feature identifier, then Command Dword 14 does not specify a UUID Index value.

Figure 186: Get Features – Command Dword 14

Bits	Description
31:07	Reserved
06:00	**UUID Index:** Refer to Figure 502.

Figure 187 describes the Feature Identifiers whose attributes may be retrieved using the Get Features command. The definition of the attributes returned and the associated format is specified in the section indicated.

Figure 187: Get Features – Feature Identifiers

Description	Section Defining Format of Attributes Returned
Arbitration	5.21.1.1
Power Management	5.21.1.2
LBA Range Type	5.21.1.3
Temperature Threshold	5.21.1.4
Error Recovery	5.21.1.5
Volatile Write Cache	5.21.1.6
Number of Queues	5.21.1.7
Interrupt Coalescing	5.21.1.8
Interrupt Vector Configuration	5.21.1.9
Write Atomicity Normal	5.21.1.10
Asynchronous Event Configuration	5.21.1.11

Figure 187: Get Features – Feature Identifiers

Description	Section Defining Format of Attributes Returned
Autonomous Power State Transition	5.21.1.12
Host Memory Buffer	5.21.1.13
Timestamp	5.21.1.14
Keep Alive Timer	5.21.1.15
Host Controlled Thermal Management	5.21.1.16
Non-Operational Power State Config	5.21.1.17
Read Recovery Level Config	5.21.1.18
Predictable Latency Mode Config	5.21.1.19
Predictable Latency Mode Window	5.21.1.20
LBA Status Information Report Interval	5.21.1.21
Host Behavior Support	5.21.1.22
Sanitize Config	5.21.1.23
Endurance Group Event Configuration	5.21.1.24
NVM Command Set Specific	
Software Progress Marker	5.21.1.25
Host Identifier	5.21.1.26
Reservation Notification Mask	5.21.1.27
Reservation Persistence	5.21.1.28
Namespace Write Protection Config	5.21.1.29

5.13.1 Select field

A Select field cleared to 000b (i.e., current) returns the current operating attribute value for the Feature Identifier specified.

A Select field set to 001b (i.e., default) returns the default attribute value for the Feature Identifier specified.

A Select field set to 010b (i.e., saved) returns the last saved attribute value for the Feature Identifier specified (i.e., the last Set Features command completed without error, with the Save bit set to ‘1’ for the Feature Identifier specified).

A Select field set to 011b (i.e., supported capabilities) returns the capabilities supported for this Feature Identifier. The capabilities supported are returned in Dword 0 of the completion entry of the Get Features command (refer to Figure 188).

5.13.2 Command Completion

Upon completion of the Get Features command, the controller posts a completion queue entry to the Admin Completion Queue. If the Select is not set to 11b, then Dword 0 of the completion queue entry may contain feature-dependent information (refer to section 5.21.1).

If the Select field is set to 11b, then Figure 188 describes the contents of Dword 0 of the completion queue entry.

Figure 188: Completion Queue Entry Dword 0 when Select=11b

Bits	Description
31:3	Reserved
2	**Changeable**: If set to ‘1’, then the feature values are changeable. If cleared to ‘0’, then the feature values are not changeable.
1	**NS Specific**: If set to ‘1’, then the Feature Identifier is namespace specific and settings are applied to individual namespaces. If cleared to ‘0’, then the Feature Identifier is not namespace specific and its settings apply to the entire controller.
0	**Saveable**: If set to ‘1’, then the feature values are saveable. If cleared to ‘0’, then the feature values are not saveable.

5.14 Get Log Page command

The Get Log Page command returns a data buffer containing the log page requested.

The Get Log Page command uses the Data Pointer, Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 13, and Command Dword 14 fields. All other command specific fields are reserved.

There are mandatory and optional Log Identifiers defined in Figure 195 and Figure 196. If a Get Log Page command is processed that specifies a Log Identifier that is not supported, then the controller should abort the command with status Invalid Field in Command.

The controller indicates support for the Log Page Offset and extended Number of Dwords (32 bits rather than 12 bits) in the Log Page Attributes field of the Identify Controller data structure. If extended data is not supported, then bits 27:16 of the Number of Dwords Lower field specify the Number of Dwords to transfer.

Figure 189: Get Log Page – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field.

Figure 190: Get Log Page – Command Dword 10

Bits	Description
31:16	**Number of Dwords Lower (NUMDL):** This field specifies the lower 16 bits of the number of dwords to return. If host software specifies a size larger than the log page requested, the controller returns the complete log page with undefined results for dwords beyond the end of the log page. The combined NUMDL and NUMDU fields form a 0's based value.
15	**Retain Asynchronous Event (RAE):** This bit specifies when to retain or clear an Asynchronous Event. If this bit is cleared to '0', the corresponding Asynchronous Event is cleared after the command completes successfully. If this bit is set to '1', the corresponding Asynchronous Event is retained (i.e., not cleared) after the command completes successfully. Host software should clear this bit to '0' for log pages that are not used with Asynchronous Events. Refer to section 5.2.
14:12	Reserved
11:08	**Log Specific Field (LSP):** If not defined for the log specified by the Log Page Identifier field, this field is reserved**.**
07:00	**Log Page Identifier (LID):** This field specifies the identifier of the log page to retrieve.

Figure 191: Get Log Page – Command Dword 11

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:16</td><td>Log Specific Identifier: This field specifies an identifier that is required for a particular log page. The log pages that require a log specific identifier are indicated in the table below.
<table>
<tr><th>Log Page</th><th>Definition</th></tr>
<tr><td>Endurance Group Information</td><td>Endurance Group Identifier (refer to section 8.17)</td></tr>
<tr><td>Predictable Latency Per NVM Set</td><td>NVM Set Identifier (refer to section 4.9)</td></tr>
</table></td></tr>
<tr><td>15:00</td><td>Number of Dwords (NUMDU): This field specifies the upper 16 bits of the number of dwords to return.</td></tr>
</table>

Figure 192: Get Log Page – Command Dword 12

Bits	Description
31:00	**Log Page Offset Lower (LPOL):** The log page offset specifies the location within a log page to start returning data from. This field specifies the lower 32 bits of the log page offset. The offset shall be dword aligned, indicated by bits 1:0 being cleared to 00b. The controller is not required to check that bits 1:0 are cleared to 00b. The controller may report an error of Invalid Field in Command if bits 1:0 are not cleared to 00b. If the controller does not report an error of Invalid Field in Command, then the controller shall operate as if bits 1:0 are cleared to 00b. If the host specifies an offset (i.e., LPOL and LPOU) that is greater than the size of the log page requested (e.g., a log page containing 100 bytes is requested starting at offset 200), then the controller shall abort the command with a status of Invalid Field in Command.

Figure 193: Get Log Page – Command Dword 13

Bits	Description
31:00	**Log Page Offset Upper (LPOU):** This field specifies the upper 32 bits of the log page offset. Refer to the Log Page Offset Lower definition.

If the controller supports selection of a UUID by the Get Log Page command (refer to Figure 195 and section 8.24), then Command Dword 14 is used to specify a UUID Index value (refer to Figure 194).

Figure 194: Get Log Page – Command Dword 14

Bits	Description
31:07	Reserved
06:00	**UUID Index:** Refer to Figure 502.

5.14.1 Log Specific Information

Figure 195 and Figure 196 define the log pages that may be retrieved with the Get Log Page command and the scope of the information that is returned in those log pages. Refer to section 7.1 for mandatory, optional, and prohibited log pages for the various controller types.

Log pages that indicate a scope of NVM subsystem return information that is global to the NVM subsystem. Log pages that indicate a scope of controller return information that is specific to the controller that is processing the command. Log pages that indicate a scope of Namespace return information that is specific to the specified namespace. For log pages that indicate multiple scopes, the namespace identifier that is specified determines which information is returned. The definition of any individual field within a log page may indicate a different scope that is specific to that individual field.

For log pages with a scope of NVM subsystem or controller (as shown in Figure 195 and Figure 196), the controller should abort commands that specify namespace identifiers other than 0h or FFFFFFFFh with status Invalid Field in Command. Otherwise the rules for namespace identifier usage in Figure 106 apply.

Figure 195: Get Log Page – Log Page Identifiers

Log Identifier	Scope	Log Page Name	Reference Section
00h	Reserved		
01h	Controller	Error Information	5.14.1.1

Figure 195: Get Log Page – Log Page Identifiers

Log Identifier	Scope	Log Page Name	Reference Section
02h	Controller [1] Namespace [2]	SMART / Health Information	5.14.1.2
03h	NVM subsystem	Firmware Slot Information	5.14.1.3
04h	Controller	Changed Namespace List	5.14.1.4
05h	Controller	Commands Supported and Effects	5.14.1.5
06h	Controller [3] NVM subsystem [4]	Device Self-test [5]	5.14.1.6
07h	Controller	Telemetry Host-Initiated [5]	5.14.1.7
08h	Controller	Telemetry Controller-Initiated [5]	5.14.1.8
09h	NVM subsystem	Endurance Group Information	5.14.1.9
0Ah	NVM subsystem	Predictable Latency Per NVM Set	5.14.1.10
0Bh	NVM subsystem	Predictable Latency Event Aggregate	5.14.1.11
0Ch	Controller	Asymmetric Namespace Access	5.14.1.12
0Dh	NVM subsystem	Persistent Event Log [5]	5.14.1.13
0Eh	Controller	LBA Status Information	5.14.1.14
0Fh	NVM subsystem	Endurance Group Event Aggregate	5.14.1.15
10h to 6Fh	Reserved		
70h	Discovery (refer to the NVMe over Fabrics specification)		
71h to 7Fh	Reserved for NVMe over Fabrics implementations		
80h to BFh	I/O Command Set Specific		
C0h to FFh	Vendor specific [5]		

KEY:
Namespace = The log page contains information about a specific namespace.
Controller = The log page contains information about the controller that is processing the command.
NVM subsystem = The log page contains information about the NVM subsystem.

NOTES:
1. For namespace identifiers of 0h or FFFFFFFFh.
2. For namespace identifiers other than 0h or FFFFFFFFh.
3. Bit 0 is cleared to ‘0’ in the DSTO field in the Identify Controller data structure (refer to Figure 251).
4. Bit 0 is set to ‘1’ in the DSTO field in the Identify Controller data structure.
5. Selection of a UUID may be supported. Refer to section 8.24.

Figure 196: Get Log Page – Log Page Identifiers, NVM Command Set Specific

Log Identifier	Scope	Description	Reference Section
80h	Controller	Reservation Notification	5.14.1.16.1
81h	NVM subsystem	Sanitize Status	5.14.1.16.2
82h to BFh	Reserved		

KEY:
Controller = The log page contains information about the controller that is processing the command.
NVM subsystem = The log page contains information about the NVM subsystem.

5.14.1.1 Error Information (Log Identifier 01h)

This log page is used to describe extended error information for a command that completed with error or report an error that is not specific to a particular command. Extended error information is provided when the More (M) bit is set to '1' in the Status Field for the completion queue entry associated with the command that completed with error or as part of an asynchronous event with an Error status type. This log page is global to the controller.

This error log may return the last *n* errors. If host software specifies a data transfer of the size of *n* error logs, then the error logs for the most recent *n* errors are returned. The ordering of the entries is based on the time when the error occurred, with the most recent error being returned as the first log entry.

Each entry in the log page returned is defined in Figure 197. The log page is a set of 64-byte entries; the maximum number of entries supported is indicated in the ELPE field in the Identify Controller data structure (refer to Figure 251). If the log page is full when a new entry is generated, the controller should insert the new entry into the log and discard the oldest entry.

The controller should clear this log page by removing all entries on power cycle and Controller Level Reset.

Figure 197: Get Log Page – Error Information Log Entry (Log Identifier 01h)

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>07:00</td><td>Error Count: This is a 64-bit incrementing error count, indicating a unique identifier for this error. The error count starts at 1h, is incremented for each unique error log entry, and is retained across power off conditions. A value of 0h indicates an invalid entry; this value is used when there are lost entries or when there are fewer errors than the maximum number of entries the controller supports.
If the value of this field is FFFFFFFFh, then the field shall be set to 1h when incremented (i.e., rolls over to 1h). Prior to NVMe 1.4, processing of incrementing beyond FFFFFFFFh is unspecified.</td></tr>
<tr><td>09:08</td><td>Submission Queue ID: This field indicates the Submission Queue Identifier of the command that the error information is associated with. If the error is not specific to a particular command, then this field shall be set to FFFFh.</td></tr>
<tr><td>11:10</td><td>Command ID: This field indicates the Command Identifier of the command that the error is associated with. If the error is not specific to a particular command, then this field shall be set to FFFFh.</td></tr>
<tr><td>13:12</td><td>
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>15:1</td><td>Status Field: This field indicates the Status Field for the command that completed. If the error is not specific to a particular command, then this field reports the most applicable status value.</td></tr>
<tr><td>0</td><td>Phase Tag: This field may indicate the Phase Tag posted for the command.</td></tr>
</table>
</td></tr>
<tr><td>15:14</td><td>Parameter Error Location: This field indicates the byte and bit of the command parameter that the error is associated with, if applicable. If the parameter spans multiple bytes or bits, then the location indicates the first byte and bit of the parameter.
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>15:11</td><td>Reserved</td></tr>
<tr><td>10:08</td><td>Bit in command that contained the error. Valid values are 0 to 7.</td></tr>
<tr><td>07:00</td><td>Byte in command that contained the error. Valid values are 0 to 63.</td></tr>
</table>
If the error is not specific to a particular command, then this field shall be set to FFFFh.</td></tr>
<tr><td>23:16</td><td>LBA: This field indicates the first LBA that experienced the error condition, if applicable.</td></tr>
<tr><td>27:24</td><td>Namespace: This field indicates the NSID of the namespace that the error is associated with, if applicable.</td></tr>
<tr><td>28</td><td>Vendor Specific Information Available: If there is additional vendor specific error information available, this field provides the log page identifier associated with that page. A value of 0h indicates that no additional information is available. Valid values are in the range of 80h to FFh.</td></tr>
</table>

Figure 197: Get Log Page – Error Information Log Entry (Log Identifier 01h)

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>29</td><td>Transport Type (TRTYPE): This field indicates the Transport Type of the transport associated with the error. The values in this field are the same as the TRTYPE values in the Discovery Log Page Entry (refer to the NVMe over Fabrics specification). If the error is not transport related, this field shall be cleared to 0h. If the error is transport related, this field shall be set to the type of the transport as follows:

<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0h</td><td>The transport type is not indicated or the error is not transport related.</td></tr>
<tr><td>1h</td><td>RDMA Transport (refer to the NVMe over Fabric specification).</td></tr>
<tr><td>2h</td><td>Fibre Channel Transport (refer to INCITS 540).</td></tr>
<tr><td>3h</td><td>TCP Transport (refer to the NVMe over Fabrics specification).</td></tr>
<tr><td>FEh</td><td>Intra-host Transport (i.e., loopback) (Note: This is a reserved value for use by host software).</td></tr>
<tr><td>All others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>31:30</td><td>Reserved</td></tr>
<tr><td>39:32</td><td>Command Specific Information: This field contains command specific information. If used, the command definition specifies the information returned.</td></tr>
<tr><td>41:40</td><td>Transport Type Specific Information: This field indicates additional transport type specific error information. If multiple errors exist, then this field indicates additional information about the first error. This field is transport type dependent (refer to TRTYPE) as follows:

<table>
<tr><th>Transport Type</th><th>Description</th></tr>
<tr><td>All others</td><td>Reserved</td></tr>
<tr><td>3h</td><td>This field indicates, the offset, in bytes, from the start of the Transport Header to the start of the field that is in error. If multiple errors exist, then this field indicates the lowest offset that is in error.</td></tr>
</table></td></tr>
<tr><td>63:42</td><td>Reserved</td></tr>
</table>

5.14.1.2 SMART / Health Information (Log Identifier 02h)

This log page is used to provide SMART and general health information. The information provided is over the life of the controller and is retained across power cycles. To request the controller log page, the namespace identifier specified is FFFFFFFFh or 0h. For compatibility with implementations compliant with revision 1.4 of this specification and earlier, hosts should use a namespace identifier of FFFFFFFFh to request the controller log page. The controller may also support requesting the log page on a per namespace basis, as indicated by bit 0 of the LPA field in the Identify Controller data structure in Figure 251.

If the log page is not supported on a per namespace basis, specifying a namespace identifier other than 0h or FFFFFFFFh should abort the command with status Invalid Field in Command. If the controller does not abort the command, then implementations compliant with this revision and earlier revisions of this specification return the controller log page. There is no namespace specific information defined in the SMART / Health log page in this revision of the specification, thus the controller log page and namespaces specific log page contain identical information.

Critical warnings regarding the health of the NVM subsystem may be indicated via an asynchronous event notification to the host. The warnings that results in an asynchronous event notification to the host are configured using the Set Features command; refer to section 5.21.1.11.

Performance may be calculated using parameters returned as part of the SMART / Health Information log. Specifically, the number of Read or Write commands, the amount of data read or written, and the amount of controller busy time enables both I/Os per second and bandwidth to be calculated.

The log page returned is defined in Figure 198.

Figure 198: Get Log Page – SMART / Health Information Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Critical Warning: This field indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set to ‘1’. If a bit is cleared to ‘0’, then that critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent.

<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>7:6</td><td>Reserved</td></tr>
<tr><td>5</td><td>If set to ‘1’, then the Persistent Memory Region has become read-only or unreliable (refer to section 4.8).</td></tr>
<tr><td>4</td><td>If set to ‘1’, then the volatile memory backup device has failed. This field is only valid if the controller has a volatile memory backup solution.</td></tr>
<tr><td>3</td><td>If set to ‘1’, then all of the media has been placed in read only mode. The controller shall not set this bit to '1' if the read-only condition on the media is a result of a change in the write protection state of a namespace (refer to section 8.19.1).</td></tr>
<tr><td>2</td><td>If set to ‘1’, then the NVM subsystem reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability.</td></tr>
<tr><td>1</td><td>If set to ‘1’, then a temperature is:

a) greater than or equal to an over temperature threshold; or
b) less than or equal to an under temperature threshold,

(refer to section 5.21.1.4).</td></tr>
<tr><td>0</td><td>If set to ‘1’, then the available spare capacity has fallen below the threshold.</td></tr>
</table></td></tr>
<tr><td>02:01</td><td>Composite Temperature: Contains a value corresponding to a temperature in Kelvins that represents the current composite temperature of the controller and namespace(s) associated with that controller. The manner in which this value is computed is implementation specific and may not represent the actual temperature of any physical point in the NVM subsystem. The value of this field may be used to trigger an asynchronous event (refer to section 5.21.1.4).

Warning and critical overheating composite temperature threshold values are reported by the WCTEMP and CCTEMP fields in the Identify Controller data structure in Figure 251.</td></tr>
<tr><td>03</td><td>Available Spare: Contains a normalized percentage (0% to 100%) of the remaining spare capacity available.</td></tr>
<tr><td>04</td><td>Available Spare Threshold: When the Available Spare falls below the threshold indicated in this field, an asynchronous event completion may occur. The value is indicated as a normalized percentage (0% to 100%). The values 101 to 255 are reserved.</td></tr>
<tr><td>05</td><td>Percentage Used: Contains a vendor specific estimate of the percentage of NVM subsystem life used based on the actual usage and the manufacturer’s prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed, but may not indicate an NVM subsystem failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state).

Refer to the JEDEC JESD218A standard for SSD device life and endurance measurement techniques.</td></tr>
</table>

Figure 198: Get Log Page – SMART / Health Information Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>06</td><td>Endurance Group Critical Warning Summary: This field indicates critical warnings for the state of Endurance Groups. Each bit corresponds to a critical warning type, multiple bits may be set to ‘1’. If a bit is cleared to ‘0’, then that critical warning does not apply to any Endurance Group. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent.

If a bit is set to ‘1’ in one or more Endurance Groups, then the corresponding bit shall be set to ‘1’ in this field.

<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>7:4</td><td>Reserved</td></tr>
<tr><td>3</td><td>If set to ‘1’, then the namespaces in one or more Endurance Groups have been placed in read only mode not as a result of a change in the write protection state of a namespace (refer to section 8.19.1).</td></tr>
<tr><td>2</td><td>If set to ‘1’, then the reliability of one or more Endurance Groups has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>If set to ‘1’, then the available spare capacity of one or more Endurance Groups has fallen below the threshold.</td></tr>
</table>
</td></tr>
<tr><td>31:07</td><td>Reserved</td></tr>
<tr><td>47:32</td><td>Data Units Read: Contains the number of 512 byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1,000 units of 512 bytes read) and is rounded up (e.g., one indicates the that number of 512 byte data units read is from 1 to 1,000, three indicates that the number of 512 byte data units read is from 2,001 to 3,000). When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data read to 512 byte units.

For the NVM command set, logical blocks read as part of Compare, Read, and Verify operations shall be included in this value.

A value of 0h in this field indicates that the number of Data Units Read is not reported.</td></tr>
<tr><td>63:48</td><td>Data Units Written: Contains the number of 512 byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (i.e., a value of 1 corresponds to 1,000 units of 512 bytes written) and is rounded up (e.g., one indicates that the number of 512 byte data units written is from 1 to 1,000, three indicates that the number of 512 byte data units written is from 2,001 to 3,000). When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data written to 512 byte units.

For the NVM command set, logical blocks written as part of Write operations shall be included in this value. Write Uncorrectable commands and Write Zeroes commands shall not impact this value.

A value of 0h in this field indicates that the number of Data Units Written is not reported.</td></tr>
<tr><td>79:64</td><td>Host Read Commands: Contains the number of read commands completed by the controller.

For the NVM command set, this value is the sum of the number of Compare commands and the number of Read commands.</td></tr>
<tr><td>95:80</td><td>Host Write Commands: Contains the number of write commands completed by the controller.

For the NVM command set, this is the number of Write commands.</td></tr>
<tr><td>111:96</td><td>Controller Busy Time: Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O Queue (specifically, a command was issued via an I/O Submission Queue Tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O Completion Queue). This value is reported in minutes.</td></tr>
<tr><td>127:112</td><td>Power Cycles: Contains the number of power cycles.</td></tr>
</table>

Figure 198: Get Log Page – SMART / Health Information Log

Bytes	Description
143:128	**Power On Hours:** Contains the number of power-on hours. This may not include time that the controller was powered and in a non-operational power state.
159:144	**Unsafe Shutdowns:** Contains the number of unsafe shutdowns. This count is incremented when a Shutdown Notification (CC.SHN) is not received prior to loss of power.
175:160	**Media and Data Integrity Errors:** Contains the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field. Errors introduced as a result of a Write Uncorrectable command (refer to section 6.16) may or may not be included in this field.
191:176	**Number of Error Information Log Entries:** Contains the number of Error Information log entries over the life of the controller.
195:192	**Warning Composite Temperature Time:** Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Warning Composite Temperature Threshold (WCTEMP) field and less than the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure in Figure 251. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
199:196	**Critical Composite Temperature Time:** Contains the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure in Figure 251. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
201:200	**Temperature Sensor 1:** Contains the current temperature reported by temperature sensor 1. This field is defined by Figure 199.
203:202	**Temperature Sensor 2:** Contains the current temperature reported by temperature sensor 2. This field is defined by Figure 199.
205:204	**Temperature Sensor 3:** Contains the current temperature reported by temperature sensor 3. This field is defined by Figure 199.
207:206	**Temperature Sensor 4:** Contains the current temperature reported by temperature sensor 4. This field is defined by Figure 199.
209:208	**Temperature Sensor 5:** Contains the current temperature reported by temperature sensor 5. This field is defined by Figure 199.
211:210	**Temperature Sensor 6:** Contains the current temperature reported by temperature sensor 6. This field is defined by Figure 199.
213:212	**Temperature Sensor 7:** Contains the current temperature reported by temperature sensor 7. This field is defined by Figure 199.
215:214	**Temperature Sensor 8:** Contains the current temperature reported by temperature sensor 8. This field is defined by Figure 199.
219:216	**Thermal Management Temperature 1 Transition Count:** Contains the number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature (refer to section 8.4.5) (i.e., the Composite Temperature rose above the Thermal Management Temperature 1). This counter shall not wrap once the value FFFFFFFFh is reached. A value of 0h, indicates that this transition has never occurred or this field is not implemented.
223:220	**Thermal Management Temperature 2 Transition Count:** Contains the number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature (refer to section 8.4.5) (i.e., the Composite Temperature rose above the Thermal Management Temperature 2). This counter shall not wrap once the value FFFFFFFFh is reached. A value of 0h, indicates that this transition has never occurred or this field is not implemented.

Figure 198: Get Log Page – SMART / Health Information Log

Bytes	Description
227:224	**Total Time For Thermal Management Temperature 1:** Contains the number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature (refer to section 8.4.5). This counter shall not wrap once the value FFFFFFFFh is reached. A value of 0h, indicates that this transition has never occurred or this field is not implemented.
231:228	**Total Time For Thermal Management Temperature 2:** Contains the number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature because of the host controlled thermal management feature (refer to section 8.4.5). This counter shall not wrap once the value FFFFFFFFh is reached. A value of 0h, indicates that this transition has never occurred or this field is not implemented.
511:232	Reserved

Figure 199: Get Log Page – Temperature Sensor Data Structure

Bits	Description
15:00	**Temperature Sensor Temperature (TST):** Contains the current temperature in degrees Kelvin reported by the temperature sensor. The physical point in the NVM subsystem whose temperature is reported by the temperature sensor and the temperature accuracy is implementation specific. An implementation that does not implement the temperature sensor reports a value of 0h. The temperature reported by a temperature sensor may be used to trigger an asynchronous event (refer to section 5.21.1.4).

5.14.1.3 Firmware Slot Information (Log Identifier 03h)

This log page is used to describe the firmware revision stored in each firmware slot supported. The firmware revision is indicated as an ASCII string. The log page also indicates the active slot number. The log page returned is defined in Figure 200.

Figure 200: Get Log Page – Firmware Slot Information Log

Bytes	Description
00	**Active Firmware Info (AFI):** Specifies information about the active firmware revision. Bit 7 is reserved. Bits 6:4 indicates the firmware slot that is going to be activated at the next Controller Level Reset. If this field is 0h, then the controller does not indicate the firmware slot that is going to be activated at the next Controller Level Reset. Bit 3 is reserved. Bits 2:0 indicates the firmware slot from which the actively running firmware revision was loaded.
07:01	Reserved
15:08	**Firmware Revision for Slot 1 (FRS1):** Contains the revision of the firmware downloaded to firmware slot 1. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.
23:16	**Firmware Revision for Slot 2 (FRS2):** Contains the revision of the firmware downloaded to firmware slot 2. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.

Figure 200: Get Log Page – Firmware Slot Information Log

Bytes	Description
31:24	**Firmware Revision for Slot 3 (FRS3):** Contains the revision of the firmware downloaded to firmware slot 3. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.
39:32	**Firmware Revision for Slot 4 (FRS4):** Contains the revision of the firmware downloaded to firmware slot 4. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.
47:40	**Firmware Revision for Slot 5 (FRS5):** Contains the revision of the firmware downloaded to firmware slot 5. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.
55:48	**Firmware Revision for Slot 6 (FRS6):** Contains the revision of the firmware downloaded to firmware slot 6. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.
63:56	**Firmware Revision for Slot 7 (FRS7):** Contains the revision of the firmware downloaded to firmware slot 7. If no valid firmware revision is present or if this slot is unsupported, this field shall be cleared to 0h.
511:64	Reserved

5.14.1.4 Changed Namespace List (Log Identifier 04h)

This log page is used to describe namespaces attached to the controller that have:

a) changed information in their Identify Namespace data structure since the last time the log page was read;
b) been added; and
c) been deleted.

The log page contains a Namespace List with up to 1,024 entries. If more than 1,024 namespaces have changed attributes since the last time the log page was read, the first entry in the log page shall be set to FFFFFFFFh and the remainder of the list shall be zero filled.

5.14.1.5 Commands Supported and Effects (Log Identifier 05h)

This log page is used to describe the commands that the controller supports and the effects of those commands on the state of the NVM subsystem. The log page is 4,096 bytes in size. There is one Commands Supported and Effects data structure per Admin command and one Commands Supported and Effects data structure per I/O command (based on the I/O Command Set selected in CC.CSS).

Figure 201: Get Log Page – Commands Supported and Effects Log

Bytes	Description
03:00	**Admin Command Supported 0 (ACS0):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the Admin command with an opcode value of 0h.
07:04	**Admin Command Supported 1 (ACS1):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the Admin command with an opcode value of 1h.
…	…
1019:1016	**Admin Command Supported 254 (ACS254):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the Admin command with an opcode value of 254.
1023:1020	**Admin Command Supported 255 (ACS255):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the Admin command with an opcode value of 255.
1027:1024	**I/O Command Supported 0 (IOCS0):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the I/O command with an opcode value of 0h.
1031:1028	**I/O Command Supported 1 (IOCS1):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the I/O command with an opcode value of 1h.

Figure 201: Get Log Page – Commands Supported and Effects Log

Bytes	Description
…	…
2043:2040	**I/O Command Supported 254 (IOCS254):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the I/O command with an opcode value of 254.
2047:2044	**I/O Command Supported 255 (IOCS255):** Contains the Commands Supported and Effects data structure (refer to Figure 202) for the I/O command with an opcode value of 255.
4095:2048	Reserved

The Commands Supported and Effects data structure describes the overall possible effect of a command, including any optional features of the command.

Host software may take command effects into account when determining how to submit commands and actions to take after the command is complete. It is recommended that if a command may change a particular capability that host software re-enumerate and/or re-initialize the associated capability after the command is complete. For example, if a namespace capability change may occur, then host software is recommended to pause the use of the associated namespace, submit the command that may cause a namespace capability change and wait for its completion, and then re-issue the Identify command.

If the namespace is attached to multiple controllers, the host(s) associated with those controllers should coordinate their commands to meet the Command Submission and Execution requirements (refer to Figure 202). The details of this coordination are outside the scope of this specification.

Figure 202: Get Log Page – Commands Supported and Effects Data Structure

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:20</td><td>Reserved</td></tr>
<tr><td>19</td><td>UUID Selection Supported: If set to ‘1’, then the controller supports selection of a UUID by this command (refer to section 8.24). If cleared to ‘0’, then the controller does not support selection of a UUID by this command.</td></tr>
<tr><td>18:16</td><td>Command Submission and Execution (CSE): This field defines the command submission and execution recommendations for the associated command.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>No command submission or execution restriction</td></tr>
<tr><td>001b</td><td>The command associated with this structure may be submitted when there is no other outstanding command to the same namespace and another command should not be submitted to the same namespace until this command is complete</td></tr>
<tr><td>010b</td><td>The command associated with this structure may be submitted when there is no other outstanding command to any namespace and another command should not be submitted to any namespace until this command is complete</td></tr>
<tr><td>011b to 111b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>15:05</td><td>Reserved</td></tr>
<tr><td>04</td><td>Controller Capability Change (CCC): If this bit is set to ‘1’, then this command may change controller capabilities. If this bit is cleared to ‘0’, then this command does not modify controller capabilities. Controller capability changes include a firmware update that changes the capabilities reported in the CAP register.</td></tr>
<tr><td>03</td><td>Namespace Inventory Change (NIC): If this bit is set to ‘1’, then this command may change the number of namespaces or capabilities for multiple namespaces. If this bit is cleared to ‘0’, then this command does not modify the number of namespaces or capabilities for multiple namespaces. Namespace inventory changes include adding or removing namespaces.</td></tr>
<tr><td>02</td><td>Namespace Capability Change (NCC): If this bit is set to ‘1’, then this command may change the capabilities of a single namespace. If this bit is cleared to ‘0’, then this command does not modify any namespace capabilities for the specified namespace. Namespace capability changes include a logical format change.</td></tr>
</table>

Figure 202: Get Log Page – Commands Supported and Effects Data Structure

Bits	Description
01	**Logical Block Content Change (LBCC):** If this bit is set to '1', then this command may modify logical block content in one or more namespaces. If this bit is cleared to '0', then this command does not modify logical block content in any namespace. Logical block content changes include a write to a logical block.
00	**Command Supported (CSUPP):** If this bit is set to '1', then this command is supported by the controller. If this bit is cleared to '0', then this command is not supported by the controller and all other fields in this structure shall be cleared to 0h.

5.14.1.6 Device Self-test (Log Identifier 06h)

This log page is used to indicate:

a) the status of any device self-test operation in progress and the percentage complete of that operation; and
b) the results of the last 20 device self-test operations.

The Self-test Result Data Structure contained in the Newest Self-test Result Data Structure field is always the result of the last completed or aborted self-test operation. The next Self-test Result Data Structure field in the Device Self-test Log contains the results of the second newest self-test operation and so on. If fewer than 20 self-test operations have completed or been aborted, then the Device Self-test Status field shall be set to Fh in the unused Self-test Result Data Structure fields and all other fields in that Self-test Result Data Structure are ignored.

Figure 203: Get Log Page – Device Self-test Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Current Device Self-Test Operation: This field defines the current device self-test operation.

Bits 7:4 are reserved.

Bits 3:0 indicates the status of the current device self-test operation as defined in the following table. If a device self-test operation is in process (i.e., this field is set to 1h or 2h), then the controller shall not set this field to 0h until a new Self-test Result Data Structure is created (i.e., if a device self-test operation completes or is aborted, then the controller shall create a Self-test Result Data Structure prior to setting this field to 0h).

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>No device self-test operation in progress</td></tr>
<tr><td>1h</td><td>Short device self-test operation in progress</td></tr>
<tr><td>2h</td><td>Extended device self-test operation in progress</td></tr>
<tr><td>3h to Dh</td><td>Reserved</td></tr>
<tr><td>Eh</td><td>Vendor specific</td></tr>
<tr><td>Fh</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>Current Device Self-Test Completion: This field defines the completion status of the current device self-test.

Bit 7 is reserved.

Bits 6:0 indicates the percentage of the device self-test operation that is complete (e.g., a value of 25 indicates that 25% of the device self-test operation is complete and 75% remains to be tested). If bits 3:0 in the Current Device Self-Test Operation field are cleared to 0h (indicating there is no device self-test operation in progress), then this field is ignored.</td></tr>
<tr><td>03:02</td><td>Reserved</td></tr>
<tr><td>31:04</td><td>Newest Self-test Result Data Structure (refer to Figure 204)</td></tr>
<tr><td>59:32</td><td>2nd newest Self-test Result Data Structure (refer to Figure 204)</td></tr>
<tr><td>…</td><td>…</td></tr>
</table>

Figure 203: Get Log Page – Device Self-test Log

Bytes	Description
535:508	19th newest Self-test Result Data Structure (refer to Figure 204)
563:536	20th newest Self-test Result Data Structure (refer to Figure 204)

Figure 204: Get Log Page – Self-test Result Data Structure

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Device Self-test Status: This field indicates the device self-test code and the status of the operation.

Bits 7:4 indicates the Self-test Code value that was specified in the Device Self-test command that started the device self-test operation that this Self-test Result Data Structure describes.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Reserved</td></tr>
<tr><td>1h</td><td>Short device self-test operation</td></tr>
<tr><td>2h</td><td>Extended device self-test operation</td></tr>
<tr><td>3h to Dh</td><td>Reserved</td></tr>
<tr><td>Eh</td><td>Vendor specific</td></tr>
<tr><td>Fh</td><td>Reserved</td></tr>
</table>
Bits 3:0 indicates the result of the device self-test operation that this Self-test Result Data Structure describes.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Operation completed without error</td></tr>
<tr><td>1h</td><td>Operation was aborted by a Device Self-test command</td></tr>
<tr><td>2h</td><td>Operation was aborted by a Controller Level Reset</td></tr>
<tr><td>3h</td><td>Operation was aborted due to a removal of a namespace from the namespace inventory</td></tr>
<tr><td>4h</td><td>Operation was aborted due to the processing of a Format NVM command</td></tr>
<tr><td>5h</td><td>A fatal error or unknown test error occurred while the controller was executing the device self-test operation and the operation did not complete</td></tr>
<tr><td>6h</td><td>Operation completed with a segment that failed and the segment that failed is not known</td></tr>
<tr><td>7h</td><td>Operation completed with one or more failed segments and the first segment that failed is indicated in the Segment Number field</td></tr>
<tr><td>8h</td><td>Operation was aborted for unknown reason</td></tr>
<tr><td>9h</td><td>Operation was aborted due to a sanitize operation</td></tr>
<tr><td>Ah to Eh</td><td>Reserved</td></tr>
<tr><td>Fh</td><td>Entry not used (does not contain a test result)</td></tr>
</table></td></tr>
<tr><td>01</td><td>Segment Number: This field indicates the segment number (refer to section 8.11) where the first self-test failure occurred. If Device Self-test Status field bits [3:0] are not set to 7h, then this field should be ignored.</td></tr>
</table>

Figure 204: Get Log Page – Self-test Result Data Structure

Bytes	Description
02	**Valid Diagnostic Information:** This field indicates the diagnostic failure information that is reported. Bits 7:4 are reserved. Bit 3 **(SC Valid):** If set to '1', then the contents of Status Code field is valid. If cleared to '0', then the contents of Status Code field is invalid. Bit 2 **(SCT Valid):** If set to '1', then the contents of Status Code Type field is valid. If cleared to '0', then the contents of Status Code Type field is invalid. Bit 1 **(FLBA Valid):** If set to '1', then the contents of Failing LBA field is valid. If cleared to '0', then the contents of Failing LBA field is invalid. Bit 0 **(NSID Valid):** If set to '1', then the contents of Namespace Identifier field is valid. If cleared to '0', then the contents of Namespace Identifier field is invalid.
03	Reserved
11:04	**Power On Hours (POH):** This field indicates the number of power-on hours at the time the device self-test operation was completed or aborted. This does not include time that the controller was powered and in a low power state condition.
15:12	**Namespace Identifier (NSID):** This field indicates the namespace that the Failing LBA occurred on. The contents of this field are valid only when the NSID Valid bit is set to '1'.
23:16	**Failing LBA:** This field indicates the LBA of the logical block that caused the test to fail. If the device encountered more than one failed logical block during the test, then this field only indicates one of those failed logical blocks. The contents of this field are valid only when the FLBA Valid bit is set to '1'.
24	**Status Code Type:** This field may contain additional information related to errors or conditions. Bits 7:3 are reserved. Bits 2:0 may contain additional information relating to errors or conditions that occurred during the device self-test operation represented in the same format used in the Status Code Type field of the Completion Queue Entry (refer to section 4.6.1.1). The contents of this field are valid only when the SCT Valid bit is set to '1'.
25	**Status Code:** This field may contain additional information relating to errors or conditions that occurred during the device self-test operation represented in the same format used in the Status Code field of the Completion Queue Entry (refer to section 4.6.1.2). The contents of this field are valid only when the SC Valid bit is set to '1'.
27:26	Vendor Specific

5.14.1.7 Telemetry Host-Initiated (Log Identifier 07h)

This log consists of a header describing the log and zero or more Telemetry Data Blocks (refer to section 8.14). All Telemetry Data Blocks are 512 bytes in size. The controller shall initiate a capture of the controller's internal controller state to this log when the controller processes a Get Log Page command for this log with the Create Telemetry Host-Initiated Data bit set to '1' in the Log Specific Field. If the host specifies a Log Page Offset Lower value that is not a multiple of 512 bytes in the Get Log Page command for this log, then the controller shall return an error of Invalid Field in Command. This log page is global to the controller.

Figure 205: Command Dword 10 – Log Specific Field

Bits	Description
11:09	Reserved

Figure 205: Command Dword 10 – Log Specific Field

Bits	Description
08	**Create Telemetry Host-Initiated Data:** If set to '1', then the controller shall capture the Telemetry Host-Initiated Data representing the internal state of the controller at the time the associated Get Log Page command is processed. If cleared to '0', then the controller shall not update the Telemetry Host-Initiated Data. The Host-Initiated Data shall not change until the controller processes: a) a subsequent Telemetry Host-Initiated Log with this bit set to '1'; b) a Firmware Commit command; or c) a power on reset.

The Telemetry Host-Initiated Data consists of three areas: Telemetry Host-Initiated Data Area 1, Telemetry Host-Initiated Data Area 2, and Telemetry Host-Initiated Data Area 3. All three areas start at Telemetry Host-Initiated Data Area Block 1. The last block of each area is indicated in Telemetry Host-Initiated Data Area y Last Block, respectively. The telemetry data captured and its size is implementation dependent. The size of the log page is variable and may be calculated using the Telemetry Host-Initiated Data Area 3 Last Block field.

The controller shall return data for all blocks requested. The data beyond the last block in Telemetry Host-Initiated Data Area 3 Last Block is undefined. If the host requests a data transfer that is not a multiple of 512 bytes, then the controller shall return an error of Invalid Field in Command.

Figure 206: Get Log Page – Telemetry Host-Initiated Log (Log Identifier 07h)

Bytes	Description
00	**Log Identifier:** This field shall be set to 07h.
04:01	Reserved
07:05	**IEEE OUI Identifier (IEEE):** Contains the Organization Unique Identifier (OUI) for the controller vendor that is able to interpret the data. If cleared to 0h, no IEEE OUI Identifier is present. The OUI shall be a valid IEEE/RAC assigned identifier that is registered at http://standards.ieee.org/develop/regauth/oui/public.html.
09:08	**Telemetry Host-Initiated Data Area 1 Last Block:** Contains the value of the last block of Telemetry Host-Initiated Data Area 1. If the Telemetry Host-Initiated Data Area 1 does not contain data, then this field shall be cleared to 0h. If this field is not 0h, then Telemetry Host-Initiated Data Area 1 begins at block 1h and ends at the block indicated in this field.
11:10	**Telemetry Host-Initiated Data Area 2 Last Block:** Contains the value of the last block of Telemetry Host-Initiated Data Area 2. This value shall be greater than or equal to the value in the Telemetry Host-Initiated Data Area 1 Last Block field. If this field is not 0h, then Telemetry Host-Initiated Data Area 2 begins at block 1h and ends at the block indicated in this field.
13:12	**Telemetry Host-Initiated Data Area 3 Last Block:** Contains the value of the last block of Telemetry Host-Initiated Data Area 3. This value shall be greater than or equal to the value in the Telemetry Host-Initiated Data Area 2 Last Block field. If this field is not 0h, then Telemetry Host-Initiated Data Area 3 begins at block 1h and ends at the block contained in this field.
381:14	Reserved
382	**Telemetry Controller-Initiated Data Available:** Contains the value of Telemetry Controller-Initiated Data Available field in the Telemetry Controller-Initiated log (refer to Figure 207).
383	**Telemetry Controller-Initiated Data Generation Number:** Contains the value of the Telemetry Controller-Initiated Data Generation Number field in the Telemetry Controller-Initiated log (refer to Figure 207).

Figure 206: Get Log Page – Telemetry Host-Initiated Log (Log Identifier 07h)

Bytes	Description
511:384	**Reason Identifier:** Contains a vendor specific identifier that describes the operating conditions of the controller at the time of capture. The Reason Identifier field should provide an identification of unique operating conditions of the controller.
1023:512	**Telemetry Host-Initiated Data Block 1:** Contains Telemetry Data Block 1 for the Telemetry Host-Initiated Log.
1535:1024	**Telemetry Host-Initiated Data Block 2:** Contains Telemetry Data Block 2 for the Telemetry Host-Initiated Log.
…	…
(*n**512)+511:(*n**512)	**Telemetry Host-Initiated Data Block *n*:** Contains Telemetry Data Block *n* for the Telemetry Host-Initiated Log.

5.14.1.8 Telemetry Controller-Initiated (Log Identifier 08h)

This log consists of a header describing the log and zero or more Telemetry Data Blocks (refer to section 8.14). All Telemetry Data Blocks are 512 bytes in size. This log is a controller initiated capture of the controller's internal state. The Telemetry Controller-Initiated Data shall persist across all resets. If the host specifies a Log Page Offset Lower value that is not a multiple of 512 bytes in the Get Log Page command for this log, then the controller shall return an error of Invalid Field in Command. This log page is global to the controller.

The Telemetry Controller-Initiated Data consists of three areas: Telemetry Controller-Initiated Data Area 1, Telemetry Controller-Initiated Data Area 2, and Telemetry Controller-Initiated Data Area 3. All three areas start at Telemetry Controller-Initiated Data Area Block 1. The last block of each area is indicated in the Telemetry Controller-Initiated Data Area y Last Block, respectively. The telemetry data captured and its size is implementation dependent. The size of the log page is variable and may be calculated using the Telemetry Controller-Initiated Data Area 3 Last Block field.

The controller shall return data for all blocks requested. The data beyond the last block in Telemetry Controller-Initiated Data Area 3 Last Block is undefined. If the host requests a data transfer that is not a multiple of 512 bytes, then the controller shall return an error of Invalid Field in Command.

Figure 207: Get Log Page – Telemetry Controller-Initiated Log (Log Identifier 08h)

Bytes	Description
00	**Log Identifier:** This field shall be set to 08h.
04:01	Reserved
07:05	**IEEE OUI Identifier (IEEE):** Contains the Organization Unique Identifier (OUI) for the controller vendor that is able to interpret the data. If cleared to 0h, no IEEE OUI Identifier is present. The OUI shall be a valid IEEE/RAC assigned identifier that is registered at http://standards.ieee.org/develop/regauth/oui/public.html.
09:08	**Telemetry Controller-Initiated Data Area 1 Last Block:** Contains the value of the last block of Telemetry Controller-Initiated Data Area 1. If the Telemetry Controller-Initiated Data Area 1 does not contain data, then this field shall be cleared to 0h. If this field is not 0h, then Telemetry Controller-Initiated Data Area 1 begins at block 1 and ends at the block indicated in this field.
11:10	**Telemetry Controller-Initiated Data Area 2 Last Block:** Contains the value of the last block of Telemetry Controller-Initiated Data Area 2. This value shall be greater than or equal to the value in the Telemetry Controller-Initiated Data Area 1 Last Block field. If this field is not 0h, then Telemetry Controller-Initiated Data Area 2 begins at block 1h and ends at the block indicated in this field.

Figure 207: Get Log Page – Telemetry Controller-Initiated Log (Log Identifier 08h)

Bytes	Description
13:12	**Telemetry Controller-Initiated Data Area 3 Last Block:** Contains the value of the last block of Telemetry Controller-Initiated Data Area 3. This value shall be greater than or equal to the value in the Telemetry Controller-Initiated Data Area 2 Last Block field. If this field is not 0h, then Telemetry Controller-Initiated Data Area 3 begins at block 1h and ends at the block indicated in this field.
381:14	Reserved
382	**Telemetry Controller-Initiated Data Available:** If this field is cleared to 0h, the log does not contain saved internal controller state. If this field is set to 1h, the log contains saved internal controller state. If this field is set to 1h, it shall not be cleared to 0h until a Get Log Page command with Retain Asynchronous Event bit cleared to '0' for the Telemetry Controller-Initiated log completes successfully. This value is persistent across power states and reset. Other values are reserved.
383	**Telemetry Controller-Initiated Data Generation Number:** Contains a value that is incremented each time the controller initiates a capture of its internal controller state into the Telemetry Controller-Initiated Data Blocks. If the value of this field is FFh, then the field shall be cleared to 0h when incremented (i.e., rolls over to 0h). This field is persistent across power cycles.
511:384	**Reason Identifier:** Contains a vendor specific identifier that describes the operating conditions of the controller at the time of capture. The Controller-Initiated Reason Identifier field should provide an identification of unique operating conditions of the controller.
1023:512	**Telemetry Controller-Initiated Data Block 1:** Contains Telemetry Data Block 1 for the Telemetry Controller -Initiated Log captured at a vendor specific time.
1535:1024	**Telemetry Controller-Initiated Data Block 2:** Contains Telemetry Data Block 2 for the Telemetry Controller -Initiated Log captured at a vendor specific time.
…	…
(*n**512)+511:(*n**512)	**Telemetry Controller-Initiated Data Block *n*:** Contains Telemetry Data Block *n* for the Telemetry Controller-Initiated log captured at a vendor specific time.

5.14.1.9 Endurance Group Information (Log Identifier 09h)

This log page is used to provide endurance information based on the Endurance Group (refer to section 8.17). An Endurance Group consists of zero or more NVM Sets. The information provided is over the life of the Endurance Group. The Endurance Group Identifier is specified in the Log Specific Identifier field in Command Dword 11 of the Get Log Page command. The log page is 512 bytes in size.

Figure 208: Get Log Page – Endurance Group Log (Log Identifier 09h)

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Critical Warning: This field indicates critical warnings for the state of the Endurance Group. Each bit corresponds to a critical warning type; multiple bits may be set to '1'. If a bit is cleared to '0', then that critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent.
If a bit is set to '1' in all Endurance Groups in the NVM subsystem, then the corresponding bit shall be set to '1' in the Critical Warning field of the SMART / Health Information log page (refer to Figure 198).
<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>7:4</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

Figure 208: Get Log Page – Endurance Group Log (Log Identifier 09h)

Bytes	Description		
	3	If set to '1', then all namespaces in the Endurance Group have been placed in read only mode for reasons other than a change in the write protect state of the namespace. The controller shall not set this bit to '1' if the read-only condition on the Endurance Group is a result of a change in the write protection state of all namespaces in the Endurance Group.	
	2	If set to '1', then the Endurance Group reliability has been degraded due to significant media related errors or any internal error that degrades NVM subsystem reliability.	
	1	Reserved	
	0	If set to '1', then the available spare capacity of the Endurance Group has fallen below the threshold.	
02:01	Reserved		
03	**Available Spare:** Contains a normalized percentage (0% to 100%) of the remaining spare capacity available for the Endurance Group.		
04	**Available Spare Threshold:** If the Available Spare falls below the threshold indicated in this field, an asynchronous event completion may occur. The value is indicated as a normalized percentage (0% to 100%). The values 101 to 255 are reserved.		
05	**Percentage Used:** Contains a vendor specific estimate of the percentage of life used for the Endurance Group based on the actual usage and the manufacturer's prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the Endurance Group has been consumed, but may not indicate an NVM failure. The value is allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour when the controller is not in a sleep state. Refer to the JEDEC JESD218A standard for SSD device life and endurance measurement techniques.		
31:06	Reserved		
47:32	**Endurance Estimate:** This field is an estimate of the total number of data bytes that may be written to the Endurance Group over the lifetime of the Endurance Group assuming a write amplification of 1 (i.e., no increase in the number of write operations performed by the device beyond the number of write operations requested by a host). This value is reported in billions (i.e., a value of 1 corresponds to 1,000,000,000 bytes written) and is rounded up (e.g., one indicates the number of bytes written is from 1 to 1,000,000,000, three indicates the number of bytes written is from 2,000,000,001 to 3,000,000,000). A value of 0h indicates that the controller does not report an Endurance Estimate.		
63:48	**Data Units Read:** Contains the total number of data bytes that have been read from the Endurance Group. This value does not include controller reads due to internal operations such as garbage collection. This value is reported in billions (i.e., a value of 1 corresponds to 1,000,000,000 bytes read) and is rounded up (e.g., one indicates the number of bytes read is from 1 to 1,000,000,000, three indicates the number of bytes read is from 2,000,000,001 to 3,000,000,000). A value of 0h indicates that the controller does not report the number of Data Units Read.		
79:64	**Data Units Written:** Contains the total number of data bytes that have been written to the Endurance Group. This value does not include controller writes due to internal operations such as garbage collection. This value is reported in billions (i.e., a value of 1 corresponds to 1,000,000,000 bytes written) and is rounded up (e.g., one indicates the number of bytes written is from 1 to 1,000,000,000, three indicates the number of bytes written is from 2,000,000,001 to 3,000,000,000). A value of 0h indicates that the controller does not report the number of Data Units Written.		
95:80	**Media Units Written:** Contains the total number of data bytes that have been written to the Endurance Group including both host and controller writes (e.g., garbage collection). This value is reported in billions (i.e., a value of 1 corresponds to 1,000,000,000 bytes written) and is rounded up (e.g., one indicates the number of bytes written is from 1 to 1,000,000,000, three indicates the number of bytes written is from 2,000,000,001 to 3,000,000,000). A value of 0h indicates that controller does not report the number of Media Units Written.		

Figure 208: Get Log Page – Endurance Group Log (Log Identifier 09h)

Bytes	Description
111:96	**Host Read Commands:** Contains the number of read commands completed by all controllers in the NVM subsystem for the Endurance Group. For the NVM command set, this is the number of Compare commands, Read commands, and Verify commands.
127:112	**Host Write Commands:** Contains the number of write commands completed by all controllers in the NVM subsystem for the Endurance Group. For the NVM command set, this is the number of Write commands.
143:128	**Media and Data Integrity Errors:** Contains the number of occurrences where the controller detected an unrecovered data integrity error for the Endurance Group. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field.
159:144	**Number of Error Information Log Entries:** Contains the number of Error Information log entries over the life of the controller for the Endurance Group.
511:160	Reserved

5.14.1.10 Predictable Latency Per NVM Set (Log Identifier 0Ah)

This log page may be used to determine the current window for the specified NVM Set when Predictable Latency Mode is enabled and any events that have occurred for the specified NVM Set. There is one log page for each NVM Set when Predictable Latency Mode is supported. Command Dword 11 (refer to Figure 191) specifies the NVM Set for which the log page is to be returned. The log page is 512 bytes in size.

The log page indicates typical values and reliable estimates for attributes associated with the Deterministic Window and the Non-Deterministic Window of the specified NVM Set. The Typical, Maximum, and Minimum values are static and worst case values over the lifetime of the NVM subsystem.

After the controller successfully completes a read of this log page with Retain Asynchronous Event bit cleared to ‘0’, then reported events are cleared to ‘0’ for the specified NVM Set and the field corresponding to the specified NVM Set is cleared to ‘0’ in the Predictable Latency Event Aggregate log page. Co-ordination between two or more hosts is beyond the scope of this specification.

Figure 209: Get Log Page – Predictable Latency Per NVM Set Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Status: This field indicates the status of the specified NVM Set.

Bits 7:3 are reserved.

Bits 2:0 indicate the window for the NVM Set when Predictable Latency Mode is enabled.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>Not used (Predictable Latency Mode not enabled)</td></tr>
<tr><td>001b</td><td>Deterministic Window (DTWIN)</td></tr>
<tr><td>010b</td><td>Non-Deterministic Window (NDWIN)</td></tr>
<tr><td>011b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>01</td><td>Reserved</td></tr>
<tr><td>03:02</td><td>Event Type: This field specifies the event(s) that occurred for the NVM Set indicated. Multiple bits may be set to ‘1’. All bits are cleared to ‘0’ after the log page is read with Retain Asynchronous Event bit cleared to ‘0’.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>00</td><td>DTWIN Reads Warning</td></tr>
<tr><td>01</td><td>DTWIN Writes Warning</td></tr>
<tr><td>02</td><td>DTWIN Time Warning</td></tr>
<tr><td>03 to 13</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

Figure 209: Get Log Page – Predictable Latency Per NVM Set Log

Bytes	Description
	14 – Autonomous transition from DTWIN to NDWIN due to typical or maximum value exceeded 15 – Autonomous transition from DTWIN to NDWIN due to Deterministic Excursion
31:04	Reserved
Typical, Maximum, and Minimum Values	
39:32	**DTWIN Reads Typical:** Indicates the typical number of 4 KiB random reads that may be performed in the Deterministic Window. Refer to section 8.18.
47:40	**DTWIN Writes Typical:** Indicates the typical number of writes in units of the Optimal Write Size that may be performed in the Deterministic Window. Refer to section 8.18.
55:48	**DTWIN Time Maximum:** Indicates the maximum time in milliseconds that the NVM Set is able to remain in a Deterministic Window before entering a Non-Deterministic Window. Refer to section 8.18.
63:56	**NDWIN Time Minimum High:** Indicates the minimum time in milliseconds that the NVM Set needs to remain in the Non-Deterministic Window before entering a Deterministic Window. This is the time necessary to prepare for remaining in the Deterministic Window for DTWIN Time Maximum. Refer to section 8.18.
71:64	**NDWIN Time Minimum Low:** Indicates the minimum time in milliseconds that the NVM Set needs to remain in the Non-Deterministic Window before entering a Deterministic Window. This is regardless of the amount of time spent in the previous Deterministic Window. Refer to section 8.18.
127:72	Reserved
Reliable Estimates	
135:128	**DTWIN Reads Estimate:** Indicates a reliable estimate of the number of 4 KiB random reads remaining in the current Deterministic Window, if applicable. This value decrements from DTWIN Reads Typical to 0h based on host read activity and operating conditions. Refer to section 8.18.1.
143:136	**DTWIN Writes Estimate:** Indicates a reliable estimate of the number of writes in units of the Optimal Write Size remaining in the current Deterministic Window, if applicable. This value decrements from DTWIN Writes Typical to 0h based on host write activity and operating conditions. Refer to section 8.18.1.
151:144	**DTWIN Time Estimate:** Indicates a reliable estimate of the time in milliseconds remaining in the current Deterministic Window, if applicable. Refer to section 8.18.1.
511:152	Reserved

5.14.1.11 Predictable Latency Event Aggregate Log Page (Log Identifier 0Bh)

This log page indicates if a Predictable Latency Event (refer to section 8.18) has occurred for a particular NVM Set. If a Predictable Latency Event has occurred, the details of the particular event are included in the Predictable Latency Per NVM Set log page for that NVM Set. An asynchronous event is generated when an entry for an NVM Set is newly added to this log page.

If there is an enabled Predictable Latency Event pending for an NVM Set, then the Predictable Latency Event Aggregate log page includes an entry for that NVM Set. The log page is an ordered list by NVM Set Identifier. For example, if Predictable Latency Events are pending for NVM Set 27, 13, and 17, then the log page shall have entries in numerical order of 13, 17, and 27. A particular NVM Set is removed from this log page after the Get Log Page is completed successfully with the Retain Asynchronous Event bit cleared to '0' for the Predictable Latency Per NVM Set log page for that NVM Set.

The log page size is limited by the NVM Set Identifier Maximum value reported in the Identify Controller data structure (refer to Figure 251). If the host reads beyond the end of the log page, zeroes are returned. The log page is defined in Figure 210.

Figure 210: Get Log Page – Predictable Latency Event Aggregate Log Page

Bytes	Description
07:00	**Number of Entries:** This field indicates the number of entries in the list. The maximum number of entries in the list corresponds to the NVM Set Identifier Maximum field reported in the Identify Controller data structure. A value of 0h indicates there are no entries in the list.
09:08	**Entry 1:** Indicates the NVM Set that has a Predictable Latency Event pending that has the numerically smallest NVM Set Identifier.
11:10	**Entry 2:** Indicates the NVM Set that has a Predictable Latency Event pending that has the second numerically smallest NVM Set Identifier, if any.
13:12	**Entry 3:** Indicates the NVM Set that has a Predictable Latency Event pending that has the third numerically smallest NVM Set Identifier, if any.
15:14	**Entry 4:** Indicates the NVM Set that has a Predictable Latency Event pending that has the fourth numerically smallest NVM Set Identifier, if any.
…	…

5.14.1.12 Asymmetric Namespace Access (Log Identifier 0Ch)

This log consists of a header describing the log and descriptors containing the asymmetric namespace access information for ANA Groups (refer to section 8.20.2) that contain namespaces that are attached to the controller processing the command. If ANA Reporting (refer to section 8.20) is supported, this log page is supported. ANA Group Descriptors shall be returned in ascending ANA Group Identifier order.

If the RGO bit is cleared to '0' in Command Dword 10, then the LPOL field in Command Dword 12 and the LPOU field in Command Dword 13 of the Get Log Page command should be cleared to 0h.

If the host performs multiple Get Log Page commands to read the ANA log page (e.g., using the LPOL field or the LPOU field), the host should re-read the header of the log page and ensure that the Change Count field in the Asymmetric Namespace Access log matches the original value read. If it does not match, then the data captured is not consistent and the ANA log page should be re-read.

Figure 211: Command Dword 10 – Log Specific Field

Bits	Description
11:09	Reserved
08	**Return Groups Only (RGO):** If set to '1', then the controller shall return ANA Group Descriptors with the Number of NSID Values field in each ANA Group Descriptor cleared to 0h (i.e., no Namespace Identifiers are returned). If cleared to '0', then the controller shall return ANA Group Descriptors that contain the Namespace Identifiers of attached namespaces that are members of the ANA Group described by that ANA Group Descriptor and the Number of NSID Values field set to the number of Namespace Identifier values in that ANA Group Descriptor.

Figure 212: Get Log Page – Asymmetric Namespace Access Log

Bytes	Description
07:00	**Change Count:** This field contains a 64-bit incrementing Asymmetric Namespace Access log change count, indicating an identifier for this set of asymmetric namespace access information. The count starts at 0h following a Controller Level Reset and is incremented each time the contents of the log page change (e.g., not only if an Asymmetric Namespace Access Change AEN is generated). If the value of this field is FFFFFFFF_FFFFFFFFh, then the field shall be cleared to 0h when incremented (i.e., rolls over to 0h).

Figure 212: Get Log Page – Asymmetric Namespace Access Log

Bytes	Description
09:08	**Number of ANA Group Descriptors:** This field indicates the number of ANA Group Descriptors available in the log page. The log page shall contain one ANA Group Descriptor for each ANA Group that contains Namespaces that are attached to the controller. If, for an ANA Group, there are no namespaces attached to the controller processing the command, then no ANA Group Descriptor is returned for that ANA Group (i.e., an ANA Group Descriptor is returned only if that ANA Group contains namespaces that are attached to the controller processing the command.
15:10	Reserved
n:16	ANA Group Descriptor 0
m:n+1	ANA Group Descriptor 1, if any
…	…
x:y	ANA Group Descriptor n, if any

The format of the ANA Group Descriptor is defined in Figure 213. Namespace Identifiers shall be listed in ascending NSID order.

Figure 213: ANA Group Descriptor format

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>03:00</td><td>ANA Group ID: The ANA Group Identifier associated with all namespaces in the ANA Group (refer to section 8.20.2) described by this ANA Group Descriptor.</td></tr>
<tr><td>07:04</td><td>Number of NSID Values: This field indicates the number of Namespace Identifier values in this ANA Group Descriptor.

If the RGO bit is set to ‘1’, then this field is cleared to 0h.</td></tr>
<tr><td>15:08</td><td>Change Count: This field contains a 64-bit incrementing count, indicating an identifier for the information contained in this ANA Group Descriptor. A value of 0h indicates that the controller does not report a Change Count for this ANA Group Descriptor. If a Change Count is reported, then the count starts at 1h following a Controller Level Reset and is incremented each time the data in this ANA Group Descriptor change. If the value of this field is FFFFFFFF_FFFFFFFFh, then the field shall be set to 1h when incremented (i.e., rolls over to 1h).

If this field contains 0h, the host should examine this ANA Group Descriptor for any changes and not use this field as an indicator that a change has occurred.</td></tr>
<tr><td>16</td><td>
<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>07:04</td><td>Reserved</td></tr>
<tr><td>03:00</td><td>Asymmetric Namespace Access State: This field indicates the Asymmetric Namespace Access state for all namespaces in this ANA Group when accessed through this controller.
<table>
<tr><th>Value</th><th>Description</th><th>Reference</th></tr>
<tr><td>01h</td><td>ANA Optimized state</td><td>8.20.3.1</td></tr>
<tr><td>02h</td><td>ANA Non-Optimized state</td><td>8.20.3.2</td></tr>
<tr><td>03h</td><td>ANA Inaccessible state</td><td>8.20.3.3</td></tr>
<tr><td>04h</td><td>ANA Persistent Loss state</td><td>8.20.3.4</td></tr>
<tr><td>0Fh</td><td>ANA Change state</td><td>8.20.3.5</td></tr>
<tr><td>All others</td><td>Reserved</td><td></td></tr>
</table>
</td></tr>
</table>
</td></tr>
<tr><td>31:17</td><td>Reserved</td></tr>
<tr><td>35:32</td><td>Namespace Identifier 0: The Namespace Identifier of the first namespace that is a member of this ANA Group.</td></tr>
<tr><td>39:36</td><td>Namespace Identifier 1: The Namespace Identifier of the second namespace, if any, that is a member of this ANA Group.</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>((n*4) + 35): ((n*4) + 32)</td><td>Namespace Identifier n: The Namespace Identifier of the n+1 namespace that is a member of this ANA Group.</td></tr>
</table>

5.14.1.13 Persistent Event Log (Log Identifier 0Dh)

The Persistent Event Log page contains information about significant events not specific to a particular command. The information in this log page shall be retained across power cycles and resets. NVM subsystems should be designed for minimal loss of event information upon power failure. This log consists of a header describing the log and zero or more Persistent Events (refer to section 5.14.1.13.1).

This log page is global to the NVM subsystem.

A sanitize operation may alter this log page (e.g., remove or modify events to prevent derivation of user data from log page information, refer to section 8.15). The events removed from this log page by a sanitize operation are unspecified.

Persistent Event Log events specified in this section should be reported in an order such that more recent events are generally reported earlier in the log data than older events. The method by which the NVM subsystem determines the order in which events occurred is vendor specific.

The number of events supported is vendor specific. The supported maximum size for the Persistent Event Log is indicated in the PELS field of Identify Controller. The number of events supported and the supported maximum size should be large enough that the number of events or the size of the Persistent Event Log data does not reach the maximum supported size over the usable life of the NVM subsystem.

The controller shall log all supported events at each event occurrence unless the controller determines that the same event is occurring at a frequency that exceeds a vendor specific threshold for the frequency of event creation. If the same event is occurring at a frequency that exceeds a vendor specific threshold then the vendor may suppress further entries for the same event. A controller may indicate if events have been suppressed in vendor specific event data.

It is vendor specific which events are deleted (e.g., important events may be retained and events that are newer than an important event that was retained may be deleted) to make room for future events if:

a) the size of the Persistent Event Log data reaches the maximum supported size;
b) the number of events reaches the largest reportable number of events; or
c) an event category reaches the largest reportable number of events for that category (e.g., information regarding 1,000 occurrences of changes to the timestamp is stored in internal data structures and extracted for reporting as Timestamp Change events in the Persistent Event Log and more than 1,000 Timestamp Change events have occurred).

Events that affect multiple controllers (e.g., an NVM Subsystem Reset) should be logged once by a controller selected by the vendor and not logged by any other controllers.

The Action field in the Log Specific Field (refer to Figure 214) specifies if:

a) A persistent event log reporting context is created at the start of processing this Get Log Page command and log page data, if any, is read from the log page data associated with that log reporting context;
b) Log page data is read from the log page data associated with a preexisting log reporting context; or
c) The persistent event log reporting context, if any, is released.

The persistent event log reporting context is vendor specific information that the controller creates for determining what information is included in the persistent event log page data (e.g., the persistent event log reporting context may be the persistent event log page data or may contain a set of pointers to the events to report).

The controller should retain the persistent event log reporting context:

a) Until the controller processes:
    a) A Get Log Page command requesting the Persistent Event Log page with the Action field set to 02h (i.e., Release Context);
    b) An NVM Subsystem Reset; or

c) A Controller Level Reset;
or

b) For a vendor specific time long enough to allow retrieval of the persistent event log page data.

Persistent Event Log events that occur while a persistent event log reporting context exists shall not be reported in the existing reporting context but shall be logged.

The host is expected to issue a Get Log Page command with the Action field set to 02h to release the persistent event log reporting context after reading the persistent event log page data.

Figure 214: Command Dword 10 – Log Specific Field

Bits	Description
11:10	Reserved
09:08	**Action:** This field specifies the action the controller shall take during processing this Get Log Page command. **Value** / **Definition** 00b: **Read Log Data:** Return persistent event log page data starting at the address indicated by the LPOU field and the LPOL field in the Get Log Page command. If the controller does not have a persistent event log reporting context, then the controller shall abort the command with a status code of Command Sequence Error. 01b: **Establish Context and Read Log Data:** The controller shall: a) determine the length of the persistent event log page data; b) determine the set of events to report in the persistent event log page data; and c) establish a persistent event log reporting context to store information describing the persistent event log data to be reported and track persistent event log page data accesses. After establishing a persistent event log reporting context the controller shall return persistent event log page data starting at the address indicated by the LPOU field and the LPOL field in the Get Log Page command. If a persistent event log reporting context already exists, then the controller shall abort the command with a status code of Command Sequence Error. 10b: **Release Context:** The controller shall release the persistent event log reporting context, if any. It is not an error if the controller does not have a persistent event log reporting context. 11b: Reserved

The log page returned is defined in Figure 215.

Figure 215: Get Log Page – Persistent Event Log (Log Identifier 0Dh)

Bytes	Description
	Persistent Event Log Header
00	**Log Identifier:** This field shall be set to 0Dh.
03:01	Reserved
07:04	**Total Number of Events (TNEV):** Contains the number of event entries in the log.
15:08	**Total Log Length (TLL):** Contains the total number of bytes of persistent event log page data available, including the header.
16	**Log Revision:** Contains a number indicating the revision of the Get Log Page data structure that this log page data complies with. Shall be set to 01h.
17	Reserved
19:18	**Log Header Length:** This field contains the length in bytes of the log header information that follows. The total length of the log header in bytes is the value in this field plus 20.

Figure 215: Get Log Page – Persistent Event Log (Log Identifier 0Dh)

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>27:20</td><td>Timestamp: Shall return a timestamp using the format Timestamp – Data Structure for Get Features defined in Figure 304 containing the timestamp for the time at which the persistent event log reporting context was established.</td></tr>
<tr><td>43:28</td><td>Power on Hours (POH): This field indicates the number of power-on hours at the time the Persistent Event log was retrieved. This may not include time that the controller was powered and in a non-operational state.</td></tr>
<tr><td>51:44</td><td>Power Cycle Count: Contains the number of power cycles for the controller.</td></tr>
<tr><td>53:52</td><td>PCI Vendor ID (VID): This is the same value as reported in the Identify Controller data structure PCI Vendor ID field (i.e., bytes 01:00).</td></tr>
<tr><td>55:54</td><td>PCI Subsystem Vendor ID (SSVID): This is the same value as reported in the Identify Controller data structure PCI Subsystem Vendor ID field (i.e., bytes 03:02).</td></tr>
<tr><td>75:56</td><td>Serial Number (SN): This field contains the same value as reported in the Serial Number field of the Identify Controller data structure, bytes 23:04.</td></tr>
<tr><td>115:76</td><td>Model Number (MN): This field contains the same value as reported in the Model Number field of the Identify Controller data structure, bytes 63:24.</td></tr>
<tr><td>371:116</td><td>NVM Subsystem NVMe Qualified Name (SUBNQN): This field contains the same value as reported in the NVM Subsystem NVMe Qualified Name field of the Identify Controller data structure, bytes 1023:768. If the NVM Subsystem NVMe Qualified Name field of the Identify Controller data structure is not supported, then all bytes of this field shall be cleared to 0h.</td></tr>
<tr><td>479:372</td><td>Reserved</td></tr>
<tr><td>511:480</td><td>Supported Events Bitmap: This field contains a bitmap indicating support for the persistent event log events. Each bit in the bitmap corresponds to the value for the event type (refer to Figure 217) (e.g., bit 222 decimal, DEh, corresponds to event type value DEh, Vendor Specific Event). A bit set to ‘1’ indicates that the corresponding event is supported. A bit cleared to ‘0’ indicates that the corresponding event is not supported.
<table>
<tr><th>Bits</th><th>Definition</th><th>Reference</th></tr>
<tr><td>255:224</td><td>Reserved</td><td></td></tr>
<tr><td>223</td><td>TCG Defined</td><td>TCG Storage Interface Interactions Specification</td></tr>
<tr><td>222</td><td>Vendor Specific Event Supported</td><td>5.14.1.13.1.14</td></tr>
<tr><td>221:14</td><td>Reserved</td><td></td></tr>
<tr><td>13</td><td>Thermal Excursion Event Support</td><td>5.14.1.13.1.13</td></tr>
<tr><td>12</td><td>Telemetry Log Create Event Support</td><td>5.14.1.13.1.12</td></tr>
<tr><td>11</td><td>Set Feature Event Support</td><td>5.14.1.13.1.11</td></tr>
<tr><td>10</td><td>Sanitize Completion Event Support</td><td>5.14.1.13.1.10</td></tr>
<tr><td>09</td><td>Sanitize Start Event Support</td><td>5.14.1.13.1.9</td></tr>
<tr><td>08</td><td>Format NVM Completion Event Support</td><td>5.14.1.13.1.8</td></tr>
<tr><td>07</td><td>Format NVM Start Event Support</td><td>5.14.1.13.1.7</td></tr>
<tr><td>06</td><td>Change Namespace Event Support</td><td>5.14.1.13.1.6</td></tr>
<tr><td>05</td><td>NVM Subsystem Hardware Error Event Support</td><td>5.14.1.13.1.5</td></tr>
<tr><td>04</td><td>Power-on or Reset Event Supported</td><td>5.14.1.13.1.4</td></tr>
<tr><td>03</td><td>Timestamp Change Event Supported</td><td>5.14.1.13.1.3</td></tr>
<tr><td>02</td><td>Firmware Commit Event Supported</td><td>5.14.1.13.1.2</td></tr>
<tr><td>01</td><td>SMART / Health Log Snapshot Event Supported</td><td>5.14.1.13.1.1</td></tr>
<tr><td>00</td><td>Reserved</td><td></td></tr>
</table></td></tr>
<tr><th colspan="2">Persistent Event Log Events</th></tr>
<tr><td>(M-1)+512:512</td><td>Persistent Event 0: This field contains the first persistent event log entry (refer to Figure 216) where M is the length of this persistent event.</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>(TLL-1):(TLL-K)</td><td>Persistent Event N: This field contains the last persistent event log entry (refer to Figure 216) where K is the length of this persistent event and TLL is the size specified in the Total Log Length field.</td></tr>
</table>

The format of the Persistent Events in the Persistent Event log is shown in Figure 216.

Figure 216: Persistent Event Format

Bytes	Description
Persistent Event Log Event Header	
00	**Event Type:** This field indicates the event type for this entry. Refer to section 5.14.1.13.1 for the definition of the event types.
01	**Event Type Revision:** This field contains a number indicating the revision of the event data structure for the event indicated by the Event Type field that this event data complies with.
02	**Event Header Length (EHL):** This field contains the length in bytes of the event header information that follows. The total length of the event header in bytes is the value in this field plus 3. The host should use the value in this field to calculate the offset to the start of the Vendor Specific Information field.
03	Reserved
05:04	**Controller Identifier:** This field contains the NVM subsystem unique controller identifier for the controller that created this event. If the event is controller specific, then the event data is associated with the controller. If the event is not controller specific, then this is the controller that the NVM subsystem selected for creating the event.
13:06	**Event Timestamp:** This field contains a timestamp using the format Timestamp – Data Structure for Get Features defined in Figure 304 containing the timestamp for the time when this event occurred.
19:14	Reserved
21:20	**Vendor Specific Information Length (VSIL):** This field indicates the length in bytes of the Vendor Specific Information. If no Vendor Specific Information is present, then this field shall be cleared to 0h. The length of the Vendor Specific Information is included in the Event Length field (bytes 23:22). Information associated with this event that is not able to be described in the event data structure fields may be reported in Vendor Specific Information fields in this event.
23:22	**Event Length (EL):** This field indicates the length in bytes of the vendor specific information, if any, and the persistent event log event data that follows. The total length of the event in bytes is the value in this field plus the value in the Event Header Length field plus 3.
Vendor Specific Information, if any	
EHL+2+VSIL:EHL+3	**Vendor Specific Information:** This field contains the vendor specific information, if any. This field is omitted if there is no vendor specific information (i.e., if VSIL is cleared to 0h).
Persistent Event Log Event Data	
EHL+EL+2: EHL+3+VSIL	**Event Data:** This field contains persistent event log events (refer to section 5.14.1.13.1).

5.14.1.13.1Persistent Event Log Events

The values that may be reported in the Event Type field (refer to section 5.14.1.13) of the event header for events in the Persistent Event log are defined in Figure 217.

Figure 217: Persistent Event Log Event Types

Type	O/M[1]	Event	Reference Section
00h		Reserved	
01h	NOTE 2	SMART / Health Log Snapshot	5.14.1.13.1.1
02h	M	Firmware Commit	5.14.1.13.1.2
03h	M	Timestamp Change	5.14.1.13.1.3
04h	M	Power-on or Reset	5.14.1.13.1.4
05h	M	NVM Subsystem Hardware Error	5.14.1.13.1.5
06h	NOTE 3	Change Namespace	5.14.1.13.1.6
07h	NOTE 3	Format NVM Start	5.14.1.13.1.7
08h	NOTE 3	Format NVM Completion	5.14.1.13.1.8
09h	NOTE 3	Sanitize Start	5.14.1.13.1.9

Figure 217: Persistent Event Log Event Types

Type	O/M[1]	Event	Reference Section
0Ah	NOTE 3	Sanitize Completion	5.14.1.13.1.10
0Bh	O	Set Feature	5.14.1.13.1.11
0Ch	O	Telemetry Log Created	5.14.1.13.1.12
0Dh	O	Thermal Excursion	5.14.1.13.1.13
0Eh to DDh		Reserved	
DEh	O	Vendor Specific Event	5.14.1.13.1.14
DFh	O	TCG Defined	5.14.1.13.1.15
E0h to FFh		Reserved	

NOTES:
1. O/M definition: O = Optional, M = Mandatory.
2. Mandatory for NVMe over PCIe implementations, Optional for NVMe over Fabrics implementations.
3. Mandatory if the command used to initiate the activity reported by the event is supported.

5.14.1.13.1.1 SMART / Health Log Snapshot Event (Event Type 01h)

NVM subsystems that support the Persistent Event Log shall create a SMART / Health Log Snapshot Event:

a) If virtualization management is not implemented, then for every controller in the NVM subsystem; or
b) If virtualization management is implemented, then for every primary controller,

at least once every 24 power on hours at a time determined by the controller.

The SMART / Health Log Snapshot Event shall set the Persistent Event Log Event Header:

a) Event Type field to 01h; and
b) Event Type Revision field to 01h.

The SMART / Health Log Snapshot Event data is specified in Figure 218.

Figure 218: SMART / Health Log Snapshot Event Data Format (Event Type 01h)

Bytes	Description
511:00	**Event Data:** Contains a snapshot of the SMART/Health Information Log data specified in Figure 198.

5.14.1.13.1.2 Firmware Commit Event (Event Type 02h)

A firmware commit event shall be recorded in the Persistent Event Log when a Firmware Commit command is completed. The Firmware Commit Event shall set the Persistent Event Log Event Format Header:

a) Event Type field to 02h; and
b) Event Type Revision field to 01h.

The Firmware Commit Event data is specified in Figure 219.

Figure 219: Firmware Commit Event Data Format (Event Type 02h)

Bytes	Description
07:00	**Old Firmware Revision:** Contains the firmware revision of the active firmware before this firmware commit event.
15:08	**New Firmware Revision:** Contains the firmware revision for the firmware that was requested to become active.
16	**Firmware Commit Action:** Contains the value from the Commit Action field in the Firmware Commit command.

Figure 219: Firmware Commit Event Data Format (Event Type 02h)

Bytes	Description
17	**Firmware Slot:** Contains the value from the Firmware Slot field in the Firmware Commit command.
18	**Status Code Type for Firmware Commit Command:** Contains the status code type from the completion queue entry for the Firmware Commit command.
19	**Status Returned for Firmware Commit Command:** Contains the status code from the completion queue entry for the Firmware Commit command.
21:20	**Vendor Assigned Firmware Commit Result Code:** Contains a vendor specific value that provides more information about the result of the firmware commit. A value of 0h indicates that no vendor assigned firmware commit result code is provided.

5.14.1.13.1.3 Timestamp Change Event (Event Type 03h)

The Timestamp Change Event (refer to Figure 220) contains the current timestamp, reported in the event header, and the timestamp from the time at which the timestamp was changed (i.e., the old timestamp).

The Timestamp Change Event shall set the Persistent Event Log Event Format Header:

a) Event Type field to 03h; and
b) Event Type Revision field to 01h.

The Timestamp Change Event data is specified in Figure 220.

Figure 220: Timestamp Change Event Format (Event Type 03h)

Bytes	Description
07:00	**Previous Timestamp:** Contains a timestamp using the format Timestamp – Data Structure for Get Features as defined in Figure 305 containing the timestamp for the time immediately before the timestamp was changed (i.e., the old timestamp).
15:08	**Milliseconds Since Reset:** Contains the time since the last Controller Level Reset reported in milliseconds.

5.14.1.13.1.4 Power-on or Reset Event (Event Type 04h)

A Power-on or Reset event shall be recorded in the Persistent Event Log when an NVM Subsystem Reset (e.g., due to a power-on) or a Controller Level Reset is completed. The Power-on or Reset Event reports information about resets due to power-on or other events that cause resets (refer to section 7.3) followed by descriptors reporting information about the controller at the time the reset occurred, including timestamp values for all controllers for use in synchronization of timestamp values across controllers.

The controller shall set the Persistent Event Log Event Format Header:

a) Event Type field to 04h; and
b) Event Type Revision field to 01h.

The Power-on or Reset Event data is specified in Figure 221.

Figure 221: Power-on or Reset Event (Event Type 04h)

Bytes	Description
07:00	**Firmware Revision:** Contains the firmware revision that becomes effective when CC.EN transitions from ‘0’ to ‘1’.

Figure 221: Power-on or Reset Event (Event Type 04h)

Bytes	Description
EL-VSIL-1:08 NOTE 1	**Reset Information List:** Contains a list of one or more Controller Reset Information descriptors (refer to Figure 222). If virtualization management is not implemented, then the list shall contain a Controller Reset Information descriptor for every controller in the NVM subsystem. If virtualization management is implemented, then the list shall contain a Controller Reset Information descriptor for every primary controller. The Controller Reset Information descriptor is shown in Figure 222.
NOTE: 1. Refer to Figure 216 for the definitions of EL and VSIL.	

Figure 222: Controller Reset Information descriptor

Bytes	Description
01:00	**Controller ID:** Contains the Controller ID for the controller with the timestamp in the Controller Timestamp field.
02	**Firmware Activation:** Contains a code indicating if this event triggered a firmware activation. Code / Definition: 00h – Indicates that this event did not trigger a firmware activation on the controller. 01h – Indicates that new firmware was activated on the controller due to this power on or reset. 02h – Indicates that an attempt to activate new firmware on the controller due to this power-on or reset failed. 03h to FFh – Reserved
03	**Operation in Progress:** Bits 7:1 are reserved. Bit 0: A value of '1' indicates that a Format NVM command was in progress for a namespace attached to the controller when this reset event occurred. A value of '0' indicates that no Format NVM commands were in progress for any namespace attached to the controller when this reset event occurred.
15:04	Reserved
19:16	**Controller Power Cycle:** Contains the power cycle count for the controller indicated in the Controller ID field.
27:20	**Power on milliseconds:** Contains the power on hours in milliseconds since being manufactured. This may not include time that the controller was powered and in a non-operational power state. The resolution of this field is vendor specific (e.g., an NVM subsystem that only counts power on time in hours only reports values corresponding to whole hours).
35:28	**Controller Timestamp:** Contains a timestamp using the format Timestamp – Data Structure for Get Features as defined in Figure 304 containing the timestamp for the controller specified in the Controller ID field at the time when this event occurred.

5.14.1.13.1.5 NVM Subsystem Hardware Error Event (Event Type 05h)

An NVM Subsystem Hardware Error event shall be recorded in the Persistent Event Log when a supported NVM subsystem hardware error event is detected. Which of the NVM subsystem hardware error events are supported is vendor specific. The NVM subsystem hardware error event shall set the Persistent Event Log Event Format Header:

- Event Type field to 05h; and
- Event Type Revision Field to 01h.

All detected NVM Subsystem Hardware Error events supported by the NVM subsystem shall be logged unless otherwise specified (e.g., suppressed due to reoccurrence frequency (refer to section 5.14.1.13)). NVM Subsystem Hardware Error event fields reporting information that is not available (e.g., due to a PCIe optional feature that is not implemented) shall be set to 0h unless otherwise specified in the NVM Subsystem Hardware Error Event code description.

The NVM Subsystem Hardware Error Event data is specified in Figure 223.

Figure 223: NVM Subsystem Hardware Error Event Format (Event Type 05h)

Bytes	Description
01:00	**NVM Subsystem Hardware Error Event Code:** This field contains a code (refer to Figure 224) indicating the type of NVM subsystem hardware error that is being reported.
03:02	Reserved
M+3:04	**Additional Hardware Error Information:** This field contains additional information about the hardware error event indicated in the NVM Subsystem Hardware Error Event Code field (refer to Figure 224). Where M is the number of bytes of additional hardware error information. This field is omitted if the subsystem hardware error being reported does not contain additional hardware error information (i.e., if the number of bytes of additional hardware error information, M, is 0h).

Figure 224: NVM Subsystem Hardware Error Event Codes

Code	Description
00h	Reserved
01h	**PCIe Correctable Error:** Indicates that the NVM subsystem has detected that a PCIe correctable error occurred. Refer to Figure 225 for the format of the Additional Hardware Error Information field.
02h	**PCIe Uncorrectable Non fatal Error:** Indicates that the NVM subsystem has detected that a PCIe uncorrectable non-fatal error occurred. Refer to Figure 225 for the format of the Additional Hardware Error Information field.
03h	**PCIe Uncorrectable Fatal Error:** Indicates that the NVM subsystem has detected that a PCIe uncorrectable fatal error occurred. Refer to Figure 225 for the format of the Additional Hardware Error Information field.
04h	**PCIe Link Status Change:** Indicates that a change in the values reported in the PCI Express Link Status register (refer to section 2.5.8) have changed due to an attempt to correct unreliable link operation. The Additional Hardware Error Information field shall be set to the contents of the PCI Express Link Status register at the time of the event.
05h	**PCIe Link Not Active:** Indicates that the Data Link Control and Management State Machine (refer to PCI Express Base specification) has transitioned out of the DL_Active state without a corresponding event (e.g., without an indication from the host that the link is to be disabled). This NVM subsystem hardware error event does not contain additional hardware error information.
06h	**Critical Warning Condition:** Indicates the NVM subsystem has detected a condition that causes a bit in the Critical Warning field of the SMART / Health Information log (refer to section 5.14.1.2) to be set to '1'. Bits in this field represent the associated state at the time of this event. The Additional Hardware Error Information field shall be set at the time of the event using the same format as is specified for the Critical Warning field of the SMART / Health Information log.

Figure 224: NVM Subsystem Hardware Error Event Codes

<table>
<tr><th>Code</th><th>Description</th></tr>
<tr><td>07h</td><td>Endurance Group Critical Warning Condition: Indicates that the NVM subsystem has detected a condition that causes a bit in the Critical Warning field of an Endurance Group Information log (refer to section 5.14.1.9) to be set to ‘1’.

Bits in this field represent the associated state at the time of this event.
The Additional Hardware Error Information field shall be four bytes long.

<table>
<tr><th>Bytes</th><th>Definition</th></tr>
<tr><td>0</td><td>Shall be set at the time of the event using the same format as is specified for the Critical Warning field of the Endurance Group Information log page.</td></tr>
<tr><td>1</td><td>Reserved</td></tr>
<tr><td>3:2</td><td>Shall be set to the Endurance Group Identifier for the associated endurance group.</td></tr>
</table>
</td></tr>
<tr><td>08h</td><td>Unsafe Shutdown: Indicates that the controller incremented the Unsafe Shutdowns field value in the SMART / Health Information Log.

The Additional Hardware Error Information field shall be set to the value from the Unsafe Shutdowns field in the SMART / Health Information log at the time of the event.</td></tr>
<tr><td>09h</td><td>Controller Fatal Status: Indicates that the Controller Fatal Status (CSTS.CFS) bit has been set to ‘1’.

This NVM subsystem hardware error event does not contain additional hardware error information.</td></tr>
<tr><td>0Ah</td><td>Media and Data Integrity Status: Indicates that a completion queue entry contained a Media and Data Integrity status code (refer to Figure 133) other than 86h (i.e., Access Denied) or 87h (i.e., Deallocated or Unwritten logical Block).

The Additional Hardware Error Information field shall be set to the contents of the completion queue entry.</td></tr>
<tr><td>0Bh to FFh</td><td>Reserved</td></tr>
</table>

Figure 225: Additional Hardware Error Information for correctable and uncorrectable PCIe errors

Bytes	Value
01:00	**PCIe Device Status Register:** Contains the contents of the PCI Device Status Register (refer to the PCI Express specification) at the time of the event.
02	Bits 7:1 Reserved Bit 0 **PCIe AER Supported:** set to ‘1’ indicates that PCIe AER (refer to the PCI Express specification) is supported and that the PCIe AER Error Status field, PCIe AER Error Mask field, PCIe AER Header Log Register field, and the PCIe AER TLP Prefix Log Register field is reported. Bit 0 cleared to ‘0’ indicates that PCIe AER is not supported and that the PCIe AER Error Status field, PCIe AER Error Mask field, PCIe AER Header Log Register field, and PCIe AER TLP Prefix Log Register field is not reported (i.e., bytes 80:16 are not reported).
15:03	Reserved
31:16	**PCIe AER Error Status:** Contains the contents of: a) the PCIe AER Correctable Error Status Register (refer to section 2.6.5) at the time of the event if the error is a correctable error; or b) The PCIe AER Uncorrectable Error Status Register (refer to section 2.6.2), at the time of the event if the error is an uncorrectable error.
47:32	**PCIe AER Error Mask:** Contains the contents of: a) the PCIe AER Correctable Error Mask Register (refer to section 2.6.6) at the time of the event if the error is a correctable error; or b) the PCIe AER Uncorrectable Error Mask Register (refer to section 2.6.3) at the time of the event if the error is an uncorrectable error.

Figure 225: Additional Hardware Error Information for correctable and uncorrectable PCIe errors

Bytes	Value
63:48	**PCIe AER Header Log Register:** Contains the contents of the PCIe AER Header Log Register (refer to section 2.6.8), if supported, at the time of the event.
79:64	**PCIe AER TLP Prefix Log Register:** Contains the contents of the PCIe AER TLP Prefix Log Register (refer to section 2.6.9), if supported, at the time of the event.

5.14.1.13.1.6 Change Namespace Event (Event Type 06h)

The Changed Namespace Event (refer to Figure 226) persists the host parameters used for successful namespace management commands. The event contains a Persistent Event Log Event header and the Change Namespace Event data.

The Changed Namespace Event shall set the Persistent Event Log Event Format Header:

- Event Type field to 06h; and
- Event Type Revision Field to 01h.

Figure 226: Change Namespace Event Data Format (Event Type 06h)

Bytes	Value
03:00	**Namespace Management CDW10:** Contains the value from command Dword 10 of the Namespace Management command that initiated the namespace change event (refer to Figure 268).
07:04	Reserved
15:08	**Namespace Size (NSZE):** For a create operation, contains the NSZE value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269). For a delete operation that specifies a single namespace this field contains the value from the NSZE field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved.
23:16	Reserved
31:24	**Namespace Capacity (NCAP):** For a creation operation, contains the NCAP value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269). For a delete operation that specifies a single namespace this field contains the value from the NCAP field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved.
32	**Formatted LBA Size (FLBAS):** For a create operation, contains the FLBAS value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269). For a delete operation that specifies a single namespace this field contains the value from the FLBAS field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved.
33	**End-to-end Data Protection Type Settings (DPS):** For a create operation, contains the DPS value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269). For a delete operation that specifies a single namespace this field contains the value from the DPS field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved.
34	**Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC):** For a create operation, contains the NMIC value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269). For a delete operation that specifies a single namespace this field contains the value from the NMIC field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved.
35	Reserved

Figure 226: Change Namespace Event Data Format (Event Type 06h)

Bytes	Value
39:36	**ANA Group Identifier (ANAGRPID):** For a create operation, contains the ANAGRPID value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269), if specified, or contains the ANAGRPID value from the Identify Namespace data (refer to Figure 249) after the namespace was created if an ANA Group Identifier was not specified in the command. For a delete operation that specifies a single namespace this field contains the value from the ANAGRPID field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved. If ANA Groups are not supported, then the ANAGRPID field shall be cleared to 0h.
41:40	**NVM Set Identifier (NVMSETID):** For a create operation, contains the NVMSETID value from the Identify Namespace data structure in the Namespace Management command (refer to Figure 269). For a delete operation that specifies a single namespace this field contains the value from the NVMSETID field of the Identify Namespace data (refer to Figure 249) for the namespace being deleted. For a delete operation that specifies all namespaces this field is reserved.
43:42	Reserved
47:44	**Namespace ID (NSID):** For a create operation, contains the NSID for the namespace that was created. For a delete operation, contains the NSID for the namespace being deleted or FFFFFFFFh for a delete operation specifying all namespaces.

5.14.1.13.1.7 Format NVM Start Event (Event Type 07h)

A Format NVM Start event shall be recorded in the Persistent Event Log after successfully validating the command parameters of a Format NVM Command (refer to section 5.23) and before modifying any of the contents of the NVM.

The Format NVM Start event shall set the Persistent Event Log Event Format Header:

- Event Type field to 07h; and
- Event Type Revision field to 01h.

Figure 227: Format NVM Start Event Data Format (Event Type 07h)

Bytes	Description
03:00	**Namespace Identifier:** Contains the namespace identifier specified in the Format NVM command.
04	**Format NVM Attributes (FNA):** Contains the value from the identify controller FNA field.
07:05	Reserved
11:08	**Format NVM CDW10:** Contains the value from command Dword 10 of the Format NVM command (refer to Figure 332).

5.14.1.13.1.8 Format NVM Completion Event (Event Type 08h)

A Format NVM Completion event shall be recorded in the Persistent Event Log at the completion of a Format NVM command that resulted in modification of the contents of the NVM.

The Format NVM Completion event shall set the Persistent Event Log Event Format Header:

- Event Type field to 08h; and
- Event Type Revision field to 01h.

Figure 228: Format NVM Completion Event Data Format (Event Type 08h)

Bytes	Description
03:00	**Namespace Identifier:** Contains the namespace identifier specified in the Format NVM command.

Figure 228: Format NVM Completion Event Data Format (Event Type 08h)

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>04</td><td>Smallest Format Progress Indicator: For a Format NVM command that formats a single namespace this field contains the lowest numerical value that was available for reporting in the FPI field of the Identify Namespace data structure (i.e., if the format did not complete successfully and the FPI field is supported then this field contains the percentage of the namespace that remained to be formatted at the time the Format NVM command completed, refer to Figure 249) during the format operation. For a Format NVM command that formats all namespaces this field shall be cleared to 0h.</td></tr>
<tr><td>05</td><td>Format NVM Status: Contains the status of the format operation.
<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>7:2</td><td>Reserved</td></tr>
<tr><td>1</td><td>Incomplete Format: If set to ‘1’, then the format operation modified one or more LBAs but did not complete successfully. If set to ‘1’, then the Format NVM Error bit shall be set to ‘1’. If cleared to ‘0’ then then the format operation either did not modify any LBAs or the format operation completed successfully.</td></tr>
<tr><td>0</td><td>Format NVM Error: If set to ‘1’, then the format operation did not complete successfully. If cleared to ‘0’, then the format operation completed successfully.</td></tr>
</table></td></tr>
<tr><td>07:06</td><td>Completion Information: Contains a vendor specific value that may provide more information about the completion of the format operation (e.g., if the format operation did not complete successfully, then this field may contain a vendor specific code that indicates a vendor specific reason).</td></tr>
<tr><td>11:08</td><td>Status Field: Contains the value that was reported in the status code field for the completion queue entry, if any, for the Format NVM command associated with this event. If no completion queue entry was reported, then this field shall be cleared to 0h.</td></tr>
</table>

5.14.1.13.1.9 Sanitize Start Event (Event Type 09h)

A Sanitize Start event shall be recorded in the Persistent Event Log at the start of a sanitize operation.

The Sanitize Start event shall set the Persistent Event Log Event Format Header:

- Event Type field to 09h; and
- Event Type Revision field to 01h.

Figure 229: Sanitize Start Event Data Format (Event Type 09h)

Bytes	Description
03:00	**SANICAP:** Contains the contents of the SANICAP field from the Identify Controller data structure.
07:04	**Sanitize CDW10:** Contains the value from command Dword 10 of the Sanitize command (refer to Figure 334).
11:08	**Sanitize CDW11:** Contains the value from command Dword 11 of the Sanitize command (refer to Figure 335).

5.14.1.13.1.10 Sanitize Completion Event (Event Type 0Ah)

A Sanitize Completion event shall be recorded in the Persistent Event Log at the completion of a sanitize operation.

The Sanitize Completion event shall set the Persistent Event Log Event Format Header:

- Event Type field to 0Ah; and
- Event Type Revision field to 01h.

Figure 230: Sanitize Completion Event Data Format (Event Type 0Ah)

Bytes	Description
1:0	**Sanitize Progress:** Contains the sanitize progress at the time of this event using the format specified for the SPROG field in the Sanitize Status log page (refer to section 5.14.1.16.2).
3:2	**Sanitize Status:** Contains the sanitize status for the time of this event using the format specified for the SSTAT field in the Sanitize Status log page. (e.g., the Global Data Erase bit indicates the status at the time of this event).
5:4	**Completion Information:** Contains a vendor specific value that may provide more information about the completion of the sanitize operation (e.g., if the sanitize operation did not complete successfully, then this field may contain a vendor specific code that indicates a vendor specific reason).
7:6	Reserved

5.14.1.13.1.11 Set Feature Event (Event Type 0Bh)

The Set Feature Event persists the data of a successful Set Features command. The event contains a Persistent Event Log Event header and the Set Feature Event data (refer to Figure 231).

The Set Feature Event shall set the Persistent Event Log Event Format Header:

- Event Type field to 0Bh; and
- Event Type Revision Field to 01h.

A Set Feature Event shall be recorded in the Persistent Event Log when the following criteria are met:

a) A Set Features command completes successfully;
b) The Feature Identifier in that Set Features command is supported to be logged in the Persistent Event Log; and
c) There is a change to the controller settings for the Feature Identifier in that Set Features s (i.e., the same setting is not set again).

A Set Feature Event may be recorded in the Persistent Event Log when there is no change to the controller settings for the Feature Identifier in that Set Features command if the following criteria are met:

a) A Set Features command completes successfully; and
b) The Feature Identifier in that Set Features command is supported to be logged in the Persistent Event Log.

The Feature Identifiers that may be supported to be logged in the Persistent Event Log are shown in Figure 426, Figure 427, Figure 434, and Figure 435.

The Command Dwords and Memory Buffer logged in the Set Feature Event data use the same formats as the formats defined by the Set Features and Get Features commands.

Figure 231: Set Feature Event Data Format

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>03:00</td><td>Set Feature Event Layout: Defines the number of Command Dwords and the amount of data in the Memory Buffer from the Set Features command associated with this event.
<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>31:16</td><td>Memory Buffer Count: Defines the number of bytes from the memory buffer that are logged in the Memory Buffer field. A value of 0h indicates that the Memory Buffer field does not exist.</td></tr>
<tr><td>15:04</td><td>Reserved</td></tr>
<tr><td>03</td><td>Logged Command Completion Dword 0: If set to ‘1’, then Dword 0 of the command completion for the Set Features command is included in the log. If cleared to ‘0’, then Dword 0 of the command completion command for the Set Features command is not included in the log.</td></tr>
<tr><td>02:00</td><td>Dword Count: Contains the number of consecutive Dwords starting with Dword 10 from the Set Features command that are reported in the Command Dwords field. The values 0h and 7h are reserved.</td></tr>
</table></td></tr>
<tr><td>(Dword Count * 4)+3: 4</td><td>Command Dwords: Contains a sequential list of Command Dwords from the Set Features command starting with Command Dword 10. The number of entries in the list is specified by the Command Dword Count field. All non-reserved Command Dwords specified by the Set Features command for the Feature Identifier shall be logged. The Command Dwords are ordered as defined by command format for the Admin Command Set and NVM Command in Figure 106.</td></tr>
<tr><td>Data Buffer Count + (Dword Count * 4)+4: (Dword Count * 4)+4</td><td>Memory Buffer: Contains the data in the memory buffer for the Set Features command.

If the Memory Buffer Count field is cleared to a value on 0h, then this field does not exist in the logged event.</td></tr>
<tr><td>Data Buffer Count + (Dword Count * 4)+8: Data Buffer Count + (Dword Count * 4)+5</td><td>Command Completion Dword 0: If the Logged Command Completion Dword 0 bit is set to ‘1’, then this field contains the Dword 0 value from the Set Features command completion. If the Logged Command Completion Dword 0 bit is cleared to ‘0’, then this field is not logged.</td></tr>
</table>

5.14.1.13.1.12 Telemetry Log Create Event (Event Type 0Ch)

A Telemetry Log Create event may be created if the controller determines that a host-initiated telemetry log (refer to section 5.14.1.7) or that a controller-initiated telemetry log (refer to section 5.14.1.8) has been generated.

The Telemetry Log Create Event shall set the Persistent Event Log Event Format Header:

- Event Type field to 0Ch; and
- Event Type Revision Field to 01h.

Figure 232: Telemetry Log Create Event Data Format (Event Type 0Ch)

Bytes	Description
511:00	**Telemetry Initiated Log:** Contains a copy of the values from the first 512 bytes of the Host Initiated Log or the first 512 bytes of the Controller Initiated Log (refer to Figure 206 and Figure 207).

5.14.1.13.1.13 Thermal Excursion Event (Event Type 0Dh)

A Thermal Excursion event shall be recorded in the Persistent Event Log if the Composite Temperature has transitioned from a temperature that is less than:

a) the WCTEMP, if any, (refer to Figure 251) to a temperature that is greater than or equal to the WCTEMP, if any; or
b) the CCTEMP, if any, (refer to Figure 251), to a temperature that is greater than or equal to the CCTEMP, if any,

unless recording of the event causes a vendor specific frequency of threshold reports for this threshold to be exceeded.

A Thermal Excursion event may be recorded in the Persistent Event Log if the Composite Temperature has transitioned from a temperature:

a) that is less than TMT1 (refer to section 5.21.1.16), if any, to a temperature that is greater than or equal to TMT1, if any (i.e., light throttling has started);
b) that is less than TMT2 (refer to section 5.21.1.16), if any, to a temperature that is greater than or equal to TMT2, if any (i.e., heavy throttling has started);
c) that is less than a vendor specific temperature where thermal throttling occurs due to self-throttling to a temperature that is greater than that vendor specific temperature (i.e., self-throttling has started);
d) outside of a temperature threshold to a value that is within all temperature thresholds (i.e., the temperature returns to normal);
e) at which thermal throttling is occurring to a temperature at which thermal throttling is stopped; or
f) that is greater than an under temperature threshold (refer to section 5.21.1.4) to a temperature that is less than or equal to an under temperature threshold,

unless recording of the event causes a vendor specific frequency of threshold reports for this threshold to be exceeded.

The Thermal Excursion event shall set the Persistent Event Log Event Format Header;

- Event Type field to 0Dh; and
- Event Type Revision field to 01h.

Figure 233: Thermal Excursion Event Data Format (Event Type 0Dh)

Bytes	Description
0	**Over Temperature:** Contains the difference (delta) in degrees Kelvin between the temperature indicated in the threshold field and temperature measured at the time of the event.

Figure 233: Thermal Excursion Event Data Format (Event Type 0Dh)

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>1</td><td>Threshold: Contains an indicator for the temperature threshold crossing that is being reported.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><th colspan="2">High Temperature Transitions</th></tr>
<tr><td>1h</td><td>The Composite Temperature has transitioned from a temperature that is less than WCTEMP to a temperature that is greater than or equal to WCTEMP.</td></tr>
<tr><td>2h</td><td>The Composite Temperature has transitioned from a temperature that is less than CCTEMP to a temperature that is greater than or equal to CCTEMP.</td></tr>
<tr><td>3h</td><td>The Composite Temperature has transitioned from a temperature that is less than TMT1 to a temperature is greater than or equal to TMT1 (i.e., vendor specific thermal management actions that minimize the impact on performance, such as light throttling, have started).</td></tr>
<tr><td>4h</td><td>The Composite Temperature has transitioned from a temperature that is less than TMT2 to a temperature that is greater than or equal to TMT2 (i.e., vendor specific thermal management actions that may impact performance, such as heavy throttling, have started).</td></tr>
<tr><td>5h</td><td>The Composite Temperature has transitioned from a temperature where no vendor specific thermal management actions are taken to a temperature that is greater than or equal to a vendor specific temperature at which vendor specific thermal management actions have started (e.g., self-throttling).</td></tr>
<tr><th colspan="2">Normal Temperature Transitions</th></tr>
<tr><td>88h</td><td>The Composite Temperature has transitioned from a temperature that is greater than or equal to WCTEMP or is less than or equal to an under temperature threshold to a temperature that is between WCTEMP and that under temperature threshold (i.e., the temperature has transitioned to a normal temperature).</td></tr>
<tr><td>89h</td><td>The Composite Temperature has transitioned from a temperature that is greater than a temperature where thermal management actions are being performed and that is not greater than or equal to WCTEMP to a temperature where thermal management actions are stopped.</td></tr>
<tr><th colspan="2">Low Temperature Transitions</th></tr>
<tr><td>B0h</td><td>The Composite Temperature has transition from a temperature that is greater than an under temperature threshold to a temperature that is less than or equal to an under temperature threshold.</td></tr>
<tr><td>F0h to FFh</td><td>Vendor specific</td></tr>
<tr><td>All others</td><td>Reserved</td></tr>
</table></td></tr>
</table>

5.14.1.13.1.14 Vendor Specific Event (Event Type DEh)

The Vendor Specific Event (refer to Figure 234) contains a set of Vendor Specific Event Descriptors that describe an event that the vendor has determined is a significant event which should be reported to a host in the persistent event log and that is not described by any of the other persistent event log events.

The Vendor Specific Event Descriptors follow the format shown in Figure 235 and contain vendor specific data of the type indicated in the Vendor Specific Event Data Type field of the Vendor Specific Event Descriptor.

If a UUID Index is specified in the Get Log Page command (refer to section 5.14), then the controller shall return:

a) Vendor specific events defined by the vendor identified by the specified UUID index; and
b) Vendor specific events defined by the NVM subsystem manufacturer.

The controller shall set the Vendor Specific Event Format Header:

a) Event Type field to DEh; and

b) Event Type Revision field to 01h.

The Vendor Specific Event data is specified in Figure 234.

Figure 234: Vendor Specific Event Format (Event Type DEh)

Bytes	Description
M-1:0	**Vendor Specific Event Descriptor 0:** Contains the first vendor specific event descriptor (refer to Figure 235). Where M is the length of this vendor specific event descriptor.
…	
EL-VSIL-1: EL-VSIL-K NOTE 1	**Vendor Specific Event Descriptor N:** Contains the last vendor specific event descriptor (refer to Figure 235), where K is the length of this vendor specific event descriptor (refer to Figure 235).
NOTE: 1. Refer to Figure 216 for the definition of EL and VSIL.	

The format of the Vendor Specific Event Descriptor is shown in Figure 235.

Figure 235: Vendor Specific Event Descriptor Format

Bytes	Description
01:00	**Vendor Specific Event Code:** Contains a vendor specific code that uniquely identifies the type of event that is described in the data that follows. All vendor specific events of the same type should report the same Vendor Specific Event Code field value.
02	**Vendor Specific Event Data Type:** Contains a code indicating the type of data reported in the Vendor Specific Event Data field (refer to Figure 236).
03	**UUID Index:** UUID Index (refer to Figure 502) at the time of this event for the vendor that defined this event.
05:04	**Vendor Specific Event Data Length (VSEDL):** Contains the length in bytes of the Vendor Specific Event Data field.
Vendor Specific Event Data, if any (i.e., VSEDL > 0)	
VSEDL+5:06	**Vendor Specific Event Data:** Contains vendor specific data that is associated with this event and is of the type specified in the Vendor Specific Event Data Type field.

The Vendor Specific Event Data Types that are able to be reported in a Vendor Specific Event Descriptor are shown in Figure 236.

Figure 236: Vendor Specific Event Data Type Codes

Code	Description
00h	Reserved
01h	**Event Name:** The Vendor Specific Event Data field contains a null terminated ASCII string with a vendor specific name for the value in the Vendor Specific Event Code field. The value reported in this field shall be the same for every vendor specific event containing a vendor specific event code that is the same as the value in the Vendor Specific Event Code field in this event. If a Vendor Specific Event Descriptor specifying this data type is reported, then that descriptor shall be the first Vendor Specific Event Descriptor in that event.
02h	**ASCII String:** The Vendor Specific Event Data field contains a null terminated ASCII string.
03h	**Binary:** The Vendor Specific Event Data field contains binary data. The byte ordering in the binary data is determined by the NVM subsystem vendor.
04h	**Signed Integer:** The Vendor Specific Event Data field contains a 64-bit signed integer in two's complement form.
05h to FFh	Reserved

5.14.1.13.1.15 TCG Defined Event (Event Type DFh)

The TCG Defined Event shall set the Persistent Event Log Event Format Header:

- Event Type field to DFh.

The Event Type Revision Field and the TCG Defined Event data are reserved for TCG.

5.14.1.14 LBA Status Information (Log Identifier 0Eh)

This log page is used to provide information about subsequent actions the host may take to discover which logical blocks, in namespaces that are attached to the controller, may no longer be recoverable when read. It contains zero or more LBA Status Log Namespace Elements (refer to Figure 238). If the controller is unaware of any potentially unrecoverable logical blocks in a given namespace attached to the controller, then this log page does not return an LBA Status Log Namespace Element for that namespace. This log page shall not return any LBA Status Log Namespace Elements for namespaces which are not attached to the controller.

Each LBA Status Log Namespace Element contains zero or more LBA Range Descriptors (refer to Figure 239). Each LBA Range Descriptor describes a range of LBAs that have been detected as being potentially unrecoverable and should be examined by the host using the mechanism specified in the Recommended Action Type field (refer to Figure 237) in that LBA Status Log Namespace Element in a subsequent Get LBA Status command.

The host may identify logical blocks that may no longer be recoverable through the subsequent issuing of one or more Get LBA Status commands. Once identified, the host may then recover the user data from an alternative source and write that data to the original logical block address in the namespace. If the user data is written successfully, subsequent reads should not cause unrecoverable read errors (e.g., as a result of the write changing the physical location of the user data).

Upon receiving an LBA Status Information Alert asynchronous event, the host should send one or more Get Log Page commands for Log Identifier 0Eh with the Retain Asynchronous Event bit set to '1' until the entire log page is read. To clear the event, the host sends a Get Log Page command for Log Identifier 0Eh with the Retain Asynchronous Event bit cleared to '0'. The host decides when to send Get LBA Status commands and when to recover the LBAs identified by the Get LBA Status commands, relative to when the host clears the event. Section 8.22.1 describes example host implementations. Clearing the event causes the LBA Status Information Report Interval to be restarted and allows the contents of the log page to be updated.

Figure 237: LBA Status Information Log

Bytes	Description
03:00	**LBA Status Log Page Length (LSLPLEN):** This field indicates the length in bytes of the LBA Status Information log page.
07:04	**Number of LBA Status Log Namespace Elements (NLSLNE):** This field indicates the number of LBA Status Log Namespace Elements (refer to Figure 238) contained in this log. If this field is cleared to 0h and the Estimate of Unrecoverable Logical Blocks (ESTULB) field contains a non-zero value, the host should send Get LBA Status commands for the entire LBA range of each namespace attached to the controller. If both this field and the Estimate of Unrecoverable Logical Blocks (ESTULB) are cleared to 0h, the host should not send any Get LBA Status commands for any LBA ranges on any namespaces attached to the controller as there are no known potentially unrecoverable logical blocks in any namespace attached to the controller.
11:08	**Estimate of Unrecoverable Logical Blocks (ESTULB):** This field is an estimate of the sum of the total number of potentially unrecoverable logical blocks in all of the namespaces identified in the LBA Status Log Namespace Elements in this log page. A value of 0h in this field is valid. A value of FFFFFFFFh indicates no information regarding an estimate of the total number of potentially unrecoverable logical blocks is available.
13:12	Reserved

Figure 237: LBA Status Information Log

Bytes	Description
15:14	**LBA Status Generation Counter (LSGC):** Contains a value that is incremented each time the LBA Status Log contains one or more LBA Range Descriptors which specify any potentially unrecoverable logical blocks which were not included in any LBA Range Descriptors the last time the host read the LBA Status Information log. This field is persistent across power on. If the value of this field is FFFFh, then the field shall be cleared to 0h when incremented (i.e., rolls over to 0h).
n:16	**LBA Status Log Namespace Element List:** This field contains the list of LBA Status Log Namespace Elements that are present in the log page, if any. LBA Status Log Namespace Elements are of variable length (refer to Figure 238).

Figure 238: LBA Status Log Namespace Element

Bytes	Description
03:00	**Namespace Element Identifier (NEID):** This field indicates the Namespace Identifier (NSID) of the namespace that this LBA Status Log Namespace Element applies to.
07:04	**Number of LBA Range Descriptors (NLRD):** This field indicates the number of LBA Range Descriptors (refer to Figure 239) returned by the controller in this LBA Status Log Namespace Element. A value of FFFFFFFFh indicates that: a) no LBA Range Descriptors are present; b) there is no information available regarding the location of known potentially unrecoverable blocks in the namespace; and c) the host should examine all LBAs in the namespace.
08	**Recommended Action Type (RATYPE):** This field indicates the value the host should set the Action Type (ATYPE) field to in Get LBA Status commands associated with LBA Range Descriptors contained in this LBA Status Log Namespace Element.
15:09	Reserved
31:16	**LBA Range Descriptor 0:** This field contains the first LBA Range Descriptor in this LBA Status Log Namespace Element, if present.
47:32	**LBA Range Descriptor 1:** This field contains the second LBA Range Descriptor in this LBA Status Log Namespace Element, if present.
…	…
(N*16+31): (N*16+16)	**LBA Range Descriptor N:** This field contains the N+1 LBA Range Descriptor in this LBA Status Log Namespace Element, if present.

Figure 239: LBA Range Descriptor

Bytes	Description
07:00	**Range Starting LBA (RSLBA):** This field specifies the 64-bit address of the first logical block of this LBA Range.
11:08	**Range Number of Logical Blocks (RNLB):** This field contains the number of logical blocks in this LBA Range. The controller should return the largest possible value in this field. This is a 0's based value.
15:12	Reserved

For a given LBA Status Log Namespace Element, if the value in the Recommended Action Type (RATYPE) field is 10h, then the controller shall not report the same LBA Status Log Namespace Element once the host issues a Get Log Page command for Log Identifier 0Eh with the Retain Asynchronous Event bit cleared to '0' unless an additional component failure has occurred that may have created additional Untracked LBAs.

5.14.1.15 Endurance Group Event Aggregate (Log Identifier 0Fh)

This log page indicates if an Endurance Group Event (refer to section 8.17) has occurred for a particular Endurance Group. If an Endurance Group Event has occurred, the details of the particular event are included in the Endurance Group Information log page for that Endurance Group. An asynchronous event is generated when an entry for an Endurance Group is newly added to this log page.

If there is an enabled Endurance Group Event pending for an Endurance Group, then the Endurance Group Event Aggregate log page includes an entry for that Endurance Group. The log page is an ordered list by Endurance Group Identifier. For example, if Endurance Group Events are pending for Endurance Group 2, 1, and 7, then the log page shall have entries in numerical order of 1, 2, and 7. A particular Endurance Group entry is removed from this log page after the Get Log Page is completed successfully with the Retain Asynchronous Event bit cleared to '0' for the Endurance Group Information log page for that Endurance Group.

The log page size is limited by the Endurance Group Identifier Maximum value reported in the Identify Controller data structure (refer to Figure 251). If the host reads beyond the end of the log page, zeroes are returned. The log page is defined in Figure 240.

Figure 240: Get Log Page – Endurance Group Event Aggregate Log Page

Bytes	Description
07:00	**Number of Entries:** This field indicates the number of entries in the list. The maximum number of entries in the list corresponds to the Endurance Group Identifier Maximum field reported in the Identify Controller data structure. A value of 0h indicates there are no entries in the list.
09:08	**Entry 1:** Indicates the Endurance Group that has an Endurance Group Event pending that has the numerically smallest Endurance Group Identifier, if any.
11:10	**Entry 2:** Indicates the Endurance Group that has an Endurance Group Event pending that has the second numerically smallest Endurance Group Identifier, if any.
13:12	**Entry 3:** Indicates the Endurance Group that has an Endurance Group Event pending that has the third numerically smallest Endurance Group Identifier, if any.
15:14	**Entry 4:** Indicates the Endurance Group that has an Endurance Group Event pending that has the fourth numerically smallest Endurance Group Identifier, if any.
…	…
2*n+7:2*n+6	**Entry n:** Indicates the Endurance Group that has an Endurance Group Event pending that has the numerically largest Endurance Group Identifier, if any.

5.14.1.16 NVM Command Set Specific Log Page Identifiers

This section describes NVM Command Set Specific log pages.

5.14.1.16.1 Reservation Notification (Log Identifier 80h)

The Reservation Notification log page reports one log page from a time ordered queue of reservation notification log pages, if available. A new Reservation Notification log page is created and added to the end of the queue of reservation notifications whenever an unmasked reservation notification occurs on any namespace that is attached to the controller. The Get Log Page command:

- returns a data buffer containing a log page corresponding to the oldest log page in the reservation notification queue (i.e., the log page containing the lowest Log Page Count field; accounting for wrapping); and
- removes that Reservation Notification log page from the queue.

If there are no available Reservation Notification log page entries when a Get Log command is issued, then an empty log page (i.e., all fields in the log page cleared to 0h) shall be returned.

If the controller is unable to store a reservation notification in the Reservation Notification log due to the size of the queue, that reservation notification is lost. If a reservation notification is lost, then the controller

shall increment the Log Page Count field of the last reservation notification in the queue (i.e., the Log Page Count field in the last reservation notification in the queue shall contain the value associated with the most recent reservation notification that has been lost).

The format of the log page is defined in Figure 241.

Figure 241: Get Log Page – Reservation Notification Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>07:00</td><td>Log Page Count: This is a 64-bit incrementing Reservation Notification log page count, indicating a unique identifier (modulo 64 bit) for this notification. The count starts at 0h following a Controller Level Reset and is incremented for every event that causes a reservation notification regardless of whether that notification is added to the queue. If the value of this field is FFFFFFFF_FFFFFFFFh, then the field is set to 1h when incremented (i.e., rolls over to 1h) and a new log page is created.

If there are no Reservation Notification log pages to return (i.e., the queue of reservation log pages is empty), then this field shall return the value 0h. Subsequent reservation notifications continue incrementing this unique identifier from the last non-zero value (i.e., the value that identified the previous Reservation Notification log page). A value of 0h indicates the log page is empty.</td></tr>
<tr><td>08</td><td>Reservation Notification Log Page Type: This field indicates the Reservation Notification type described by this log page.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>Empty Log Page: Get Log Page command was processed when no unread Reservation Notification log pages were available. All the fields of an empty log page shall have a value of 0h.</td></tr>
<tr><td>1h</td><td>Registration Preempted</td></tr>
<tr><td>2h</td><td>Reservation Released</td></tr>
<tr><td>3h</td><td>Reservation Preempted</td></tr>
<tr><td>4h to FFh</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>09</td><td>Number of Available Log Pages: This field indicates the number of additional available Reservation Notification log pages (i.e., the number of unread log pages not counting this one). If there are more than 255 additional available log pages, then a value of 255 is returned. A value of 0h indicates that there are no additional available log pages.</td></tr>
<tr><td>11:10</td><td>Reserved</td></tr>
<tr><td>15:12</td><td>Namespace ID: This field indicates the namespace ID of the namespace associated with the Reservation Notification described by this log page.</td></tr>
<tr><td>63:16</td><td>Reserved</td></tr>
</table>

5.14.1.16.2Sanitize Status (Log Identifier 81h)

The Sanitize Status log page is used to report sanitize operation time estimates and information about the most recent sanitize operation (refer to section 8.15). The Get Log Page command returns a data buffer containing a log page formatted as defined in Figure 242. This log page shall be retained across power cycles and resets. This log page shall contain valid data whenever CSTS.RDY is set to '1'.

If the Sanitize Capabilities (SANICAP) field in the Identify Controller data structure is not cleared to 0h (i.e., the Sanitize command is supported), then this log page shall be supported. If the Sanitize Capabilities field in the Identify Controller data structure is cleared to 0h, then this log page is reserved.

Figure 242: Get Log Page – Sanitize Status Log

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>01:00</td><td>Sanitize Progress (SPROG): This field indicates the fraction complete of the sanitize operation. The value is a numerator of the fraction complete that has 65,536 (10000h) as its denominator. This value shall be set to FFFFh if bits 2:0 of the SSTAT field are not set to 010b.

If a sanitize operation has been started by a Sanitize command with the No-Deallocate After Sanitize bit set to ‘1’ (refer to section 5.24) and if NODMMAS field in the Identify Controller data structure is set to 10b (refer to Figure 251), then the fraction reported shall include the time related to the additional media modification.</td></tr>
<tr><td>03:02</td><td>Sanitize Status (SSTAT): This field indicates the status associated with the most recent sanitize operation.

Bits 15:9 are reserved.

Bit 8 (Global Data Erased): If set to ‘1’, then no namespace logical block in the NVM subsystem has been written to and no Persistent Memory Region in the NVM subsystem has been enabled:
a) since being manufactured and the NVM subsystem has never been sanitized; or
b) since the most recent successful sanitize operation.

If cleared to ‘0’, then a namespace logical block in the NVM subsystem has been written to or a Persistent Memory Region in the NVM subsystem has been enabled:
a) since being manufactured and the NVM subsystem has never been sanitized; or
b) since the most recent successful sanitize operation of the NVM subsystem.

Bits 7:3 contains the number of completed passes if the most recent sanitize operation was an Overwrite. This field shall be cleared to 0h if the most recent sanitize operation was not an Overwrite.

Bits 2:0 contains the status of the most recent sanitize operation as shown below.

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>The NVM subsystem has never been sanitized.</td></tr>
<tr><td>001b</td><td>The most recent sanitize operation completed successfully including any additional media modification (refer to the No-Deallocate Modifies Media After Sanitize field in Figure 251).</td></tr>
<tr><td>010b</td><td>A sanitize operation is currently in progress.</td></tr>
<tr><td>011b</td><td>The most recent sanitize operation failed.</td></tr>
<tr><td>100b</td><td>The most recent sanitize operation for which No-Deallocate After Sanitize (refer to section 5.24) was requested has completed successfully with deallocation of all logical blocks (refer to section 5.21.1.23).</td></tr>
<tr><td>101b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>07:04</td><td>Sanitize Command Dword 10 Information (SCDW10): This field contains the value of the Command Dword 10 field of the Sanitize command that started the sanitize operation whose status is reported in the SSTAT field. Refer to Figure 334.</td></tr>
<tr><td>11:08</td><td>Estimated Time For Overwrite: This field indicates the number of seconds required to complete an Overwrite sanitize operation with 16 passes in the background (refer to section 5.24) when the No-Deallocate Modifies Media After Sanitize field (refer to Figure 251) is not set to 10b. A value of 0h indicates that the sanitize operation is expected to be completed in the background when the Sanitize command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.</td></tr>
<tr><td>15:12</td><td>Estimated Time For Block Erase: This field indicates the number of seconds required to complete a Block Erase sanitize operation in the background (refer to section 5.24) when the No-Deallocate Modifies Media After Sanitize field (refer to Figure 251) is not set to 10b. A value of 0h indicates that the sanitize operation is expected to be completed in the background when the Sanitize command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.</td></tr>
</table>

Figure 242: Get Log Page – Sanitize Status Log

Bytes	Description
19:16	**Estimated Time For Crypto Erase:** This field indicates the number of seconds required to complete a Crypto Erase sanitize operation in the background (refer to section 5.24) when the No-Deallocate Modifies Media After Sanitize field (refer to Figure 251) is not set to 10b. A value of 0h indicates that the sanitize operation is expected to be completed in the background when the Sanitize command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
23:20	**Estimated Time For Overwrite With No-Deallocate Media Modification:** This field indicates the number of seconds required to complete an Overwrite sanitize operation and the associated additional media modification after the Overwrite sanitize operation in the background (refer to section 5.24) when: a) the No-Deallocate After Sanitize bit was set to '1' in the Sanitize command that requested the Overwrite sanitize operation; and b) the No-Deallocate Modifies Media After Sanitize field (refer to Figure 251) is set to 10b. A value of 0h indicates that the sanitize operation is expected to be completed in the background when the Sanitize command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
27:24	**Estimated Time For Block Erase With No-Deallocate Media Modification:** This field indicates the number of seconds required to complete a Block Erase sanitize operation and the associated additional media modification after the Block Erase sanitize operation in the background (refer to section 5.24) when: a) the No-Deallocate After Sanitize bit was set to '1' in the Sanitize command that requested the Block Erase sanitize operation; and b) the No-Deallocate Modifies Media After Sanitize field (refer to Figure 251) is set to 10b. A value of 0h indicates that the sanitize operation is expected to be completed in the background when the Sanitize command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
31:28	**Estimated Time For Crypto Erase With No-Deallocate Media Modification:** This field indicates the number of seconds required to complete a Crypto Erase sanitize operation and the associated additional media modification after the Crypto Erase sanitize operation in the background (refer to section 5.24) when: a) the No-Deallocate After Sanitize bit was set to '1' in the Sanitize command that requested the Crypto Erase sanitize operation; and b) the No-Deallocate Modifies Media After Sanitize field (refer to Figure 251) is set to 10b. A value of 0h indicates that the sanitize operation is expected to be completed in the background when the Sanitize command that started that operation is completed. A value of FFFFFFFFh indicates that no time period is reported.
511:32	Reserved

5.14.2 Command Completion

Upon completion of the Get Log Page command, the controller posts a completion queue entry to the Admin Completion Queue. Get Log Page command specific status values are defined in Figure 243.

Figure 243: Get Log Page – Command Specific Status Values

Value	Description
9h	**Invalid Log Page:** The log page indicated is invalid or not supported. This error condition is also returned if a reserved log page is requested. Controllers compliant with versions 1.3 and earlier of the specification may return Invalid Field in Command for this condition.

5.15 Identify command

5.15.1 Identify command overview

The Identify command returns a data buffer that describes information about the NVM subsystem, the controller or the namespace(s). The data structure is 4,096 bytes in size.

The Identify command uses the Data Pointer, Command Dword 10, Command Dword 11, and Command Dword 14 fields. All other command specific fields are reserved.

Figure 244: Identify – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field. If using PRPs, this field shall not be a pointer to a PRP List as the data buffer may not cross more than one page boundary.

Figure 245: Identify – Command Dword 10

Bits	Description
31:16	**Controller Identifier (CNTID):** This field specifies the controller identifier used as part of some Identify operations. Whether the CNTID field is used for a particular Identify operation is indicated in Figure 248. If this field is not used as part of the Identify operation, then: • host software shall clear this field to 0h for backwards compatibility (0h is a valid controller identifier); and • the controller shall ignore this field. Controllers that support the Namespace Management capability (refer to section 8.12) shall support this field.
15:08	Reserved
07:00	**Controller or Namespace Structure (CNS):** This field specifies the information to be returned to the host. Refer to Figure 248.

Figure 246: Identify – Command Dword 11

Bits	Description
31:16	Reserved
15:00	**NVM Set Identifier (NVMSETID):** This field specifies the identifier of the NVM Set. This field is used for Identify operations with a CNS value of 04h. This field should be cleared to 0h for Identify operations with other CNS values.

If the controller supports selection of a UUID by the Identify command (refer to section 8.24), then Command Dword 14 is used to specify a UUID Index value (refer to Figure 247).

Figure 247: Identify – Command Dword 14

Bits	Description
31:07	Reserved
06:00	**UUID Index:** Refer to Figure 502.

The data structure returned is based on the Controller or Namespace Structure (CNS) field as shown in Figure 248. If there are fewer entries to return for the data structure indicated based on CNS value, then

the unused portion of the list is zero filled. If a controller does not support the specified CNS value, then the controller shall abort the command with a status of Invalid Field in Command.

Note: The CNS field was specified as a one bit field in revision 1.0 and as a two bit field in revision 1.1. Host software should only issue CNS values defined in revision 1.0 to controllers compliant with revision 1.0. Host software should only issue CNS values defined in revision 1.1 to controllers compliant with revision 1.1. The results of issuing other CNS values to controllers compliant with revision 1.0 or 1.1, respectively, are indeterminate.

The Identify Controller data structure and Identify Namespace data structure include several identifiers. The format and layout of these identifiers is described in section 7.10.

Figure 248: Identify – CNS Values

CNS Value	O/M [1]	Definition	NSID[2]	CNTID[3]	Reference Section
Active Namespace Management					
00h	M	Identify Namespace data structure for the specified NSID or the common namespace capabilities. [6]	Y	N	5.15.2.1
01h	M	Identify Controller data structure for the controller processing the command. [6]	N	N	5.15.2.2
02h	M	Active Namespace ID list.	Y	N	5.15.2.3
03h	M	Namespace Identification Descriptor list for the specified NSID.	Y	N	5.15.2.4
04h	O	An NVM Set List (refer to Figure 254) is returned to the host for up to 31 NVM Sets. The list contains entries for NVM Set identifiers greater than or equal to the value specified in the NVM Set Identifier (CDW11.NVMSETID) field.	N	N	5.15.2.5
05h to 0Fh		Reserved			
Controller and Namespace Management					
10h	O [4]	Allocated Namespace ID list.	Y	N	5.15.2.6
11h	O [4]	Identify Namespace data structure for the specified allocated NSID.	Y	N	5.15.2.7
12h	O [4]	Controller List of controllers attached to the specified NSID.	Y	Y	5.15.2.8
13h	O [4]	Controller List of controllers that exist in the NVM subsystem.	N	Y	5.15.2.9
14h	O [5]	Primary Controller Capabilities data structure for the specified primary controller.	N	Y	5.15.2.10
15h	O [5]	Secondary Controller list of controllers associated with the primary controller processing the command.	N	Y	5.15.2.11
16h	O	A Namespace Granularity List (refer to Figure 259) is returned to the host for up to sixteen Namespace Granularity Entries.	N	N	5.15.2.12
17h	O	A UUID List (refer to Figure 261) is returned to the host.	N	N	5.15.2.13
18h to 1Fh		Reserved			
Future Definition					
20h to FFh		Reserved			

NOTES:
1. O/M definition: O = Optional, M = Mandatory.
2. The NSID field is used: Y = Yes, N = No.
3. The CDW10.CNTID field is used: Y = Yes, N = No.
4. Mandatory for controllers that support the Namespace Management capability (refer to section 8.12).
5. Mandatory for controllers that support Virtualization Enhancements (refer to section 8.5).
6. Selection of a UUID may be supported. Refer to section 8.24.

5.15.2 Identify Data Structures

5.15.2.1 Identify Namespace data structure (CNS 00h)

If the Namespace Identifier (NSID) field specifies an active NSID, then the Identify Namespace data structure (refer to Figure 249) is returned to the host for that specified namespace. If that specified namespace is an inactive NSID, then the controller returns a zero filled data structure.

If the controller supports the Namespace Management capability (refer to section 8.12) and the NSID field is set to FFFFFFFFh, then the controller returns an Identify Namespace data structure that specifies capabilities that are common across namespaces for the controller. If the controller does not support the Namespace Management capability and the NSID field is set to FFFFFFFFh, then the controller shall abort the command with a status code of Invalid Namespace or Format.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
07:00	M	**Namespace Size (NSZE):** This field indicates the total size of the namespace in logical blocks. A namespace of size *n* consists of LBA 0 through (*n* - 1). The number of logical blocks is based on the formatted LBA size.
15:08	M	**Namespace Capacity (NCAP):** This field indicates the maximum number of logical blocks that may be allocated in the namespace at any point in time. The number of logical blocks is based on the formatted LBA size. Spare LBAs are not reported as part of this field. Refer to section 6.1.7 for details on the usage of this field.
23:16	M	**Namespace Utilization (NUSE):** This field indicates the current number of logical blocks allocated in the namespace. This field is smaller than or equal to the Namespace Capacity. The number of logical blocks is based on the formatted LBA size. Refer to section 6.1.7 for details on the usage of this field.
24	M	**Namespace Features (NSFEAT):** This field defines features of the namespace. Bits 7:5 are reserved. Bit 4 (**OPTPERF**) if set to '1' indicates that the fields NPWG, NPWA, NPDG, NPDA, and NOWS are defined for this namespace and should be used by the host for I/O optimization (refer to section 8.25). If cleared to '0', then the controller does not support the fields NPWG, NPWA, NPDG, NPDA, and NOWS for this namespace. Bit 3 (**UIDREUSE**) if set to '1' indicates that the value in the NGUID field for this namespace, if non-zero, is never reused by the controller and that the value in the EUI64 field for this namespace, if non-zero, is never reused by the controller. If cleared to '0', then the NGUID value may be reused and the EUI64 value may be reused by the controller for a new namespace created after this namespace is deleted. This bit shall be cleared to '0' if both NGUID and EUI64 fields are cleared to 0h. Refer to section 7.11. Bit 2 (**DAE**) if set to '1' indicates that the controller supports the Deallocated or Unwritten Logical Block error for this namespace. If cleared to '0', then the controller does not support the Deallocated or Unwritten Logical Block error for this namespace. Refer to section 6.7.1.1. Bit 1 (**NSABP**) if set to '1' indicates that the fields NAWUN, NAWUPF, and NACWU are defined for this namespace and should be used by the host for this namespace instead of the AWUN, AWUPF, and ACWU fields in the Identify Controller data structure. If cleared to '0', then the controller does not support the fields NAWUN, NAWUPF, and NACWU for this namespace. In this case, the host should use the AWUN, AWUPF, and ACWU fields defined in the Identify Controller data structure in Figure 251. Refer to section 6.4. Bit 0 (**THINP**) if set to '1' indicates that the namespace supports thin provisioning. If cleared to '0' indicates that thin provisioning is not supported. Refer to section 6.1.7 for details on the usage of this field.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
25	M	**Number of LBA Formats (NLBAF):** This field defines the number of supported LBA data size and metadata size combinations supported by the namespace. LBA formats shall be allocated in order (starting with 0) and packed sequentially. This is a 0's based value. The maximum number of LBA formats that may be indicated as supported is 16. The supported LBA formats are indicated in bytes 128 to 191 in this data structure. The LBA Format fields with an index beyond the value set in this field are invalid and not supported. LBA Formats that are valid, but not currently available may be indicated by setting the LBA Data Size for that LBA Format to 0h. The metadata may be either transferred as part of the LBA (creating an extended LBA which is a larger LBA size that is exposed to the application) or may be transferred as a separate contiguous buffer of data. The metadata shall not be split between the LBA and a separate metadata buffer. It is recommended that software and controllers transition to an LBA size that is 4 KiB or larger for ECC efficiency at the controller. If providing metadata, it is recommended that at least 8 bytes are provided per logical block to enable use with end-to-end data protection, refer to section 8.2.
26	M	**Formatted LBA Size (FLBAS):** This field indicates the LBA data size & metadata size combination that the namespace has been formatted with (refer to section 5.23). Bits 7:5 are reserved. Bit 4 if set to '1' indicates that the metadata is transferred at the end of the data LBA, creating an extended data LBA. Bit 4 if cleared to '0' indicates that all of the metadata for a command is transferred as a separate contiguous buffer of data. Bit 4 is not applicable when there is no metadata. Bits 3:0 indicates one of the 16 supported LBA Formats indicated in this data structure.
27	M	**Metadata Capabilities (MC):** This field indicates the capabilities for metadata. Bits 7:2 are reserved. Bit 1 if set to '1' indicates the namespace supports the metadata being transferred as part of a separate buffer that is specified in the Metadata Pointer. Bit 1 if cleared to '0' indicates that the namespace does not support the metadata being transferred as part of a separate buffer. Bit 0 if set to '1' indicates that the namespace supports the metadata being transferred as part of an extended data LBA. Bit 0 if cleared to '0' indicates that the namespace does not support the metadata being transferred as part of an extended data LBA.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

<table>
<tr><th>Bytes</th><th>O/M [1]</th><th>Description</th></tr>
<tr><td>28</td><td>M</td><td>End-to-end Data Protection Capabilities (DPC): This field indicates the capabilities for the end-to-end data protection feature. Multiple bits may be set in this field. Refer to section 8.3.

Bits 7:5 are reserved.

Bit 4 if set to ‘1’ indicates that the namespace supports protection information transferred as the last eight bytes of metadata. Bit 4 if cleared to ‘0’ indicates that the namespace does not support protection information transferred as the last eight bytes of metadata.

Bit 3 if set to ‘1’ indicates that the namespace supports protection information transferred as the first eight bytes of metadata. Bit 3 if cleared to ‘0’ indicates that the namespace does not support protection information transferred as the first eight bytes of metadata.

Bit 2 if set to ‘1’ indicates that the namespace supports Protection Information Type 3. Bit 2 if cleared to ‘0’ indicates that the namespace does not support Protection Information Type 3.

Bit 1 if set to ‘1’ indicates that the namespace supports Protection Information Type 2. Bit 1 if cleared to ‘0’ indicates that the namespace does not support Protection Information Type 2.

Bit 0 if set to ‘1’ indicates that the namespace supports Protection Information Type 1. Bit 0 if cleared to ‘0’ indicates that the namespace does not support Protection Information Type 1.</td></tr>
<tr><td>29</td><td>M</td><td>End-to-end Data Protection Type Settings (DPS): This field indicates the Type settings for the end-to-end data protection feature. Refer to section 8.3.

Bits 7:4 are reserved.

Bit 3 if set to ‘1’ indicates that the protection information, if enabled, is transferred as the first eight bytes of metadata. Bit 3 if cleared to ‘0’ indicates that the protection information, if enabled, is transferred as the last eight bytes of metadata.

Bits 2:0 indicate whether Protection Information is enabled and the type of Protection Information enabled. The values for this field have the following meanings:
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>Protection information is not enabled</td></tr>
<tr><td>001b</td><td>Protection information is enabled, Type 1</td></tr>
<tr><td>010b</td><td>Protection information is enabled, Type 2</td></tr>
<tr><td>011b</td><td>Protection information is enabled, Type 3</td></tr>
<tr><td>100b to 111b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>30</td><td>O</td><td>Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC): This field specifies multi-path I/O and namespace sharing capabilities of the namespace.

Bits 7:1 are reserved.

Bit 0: If set to ‘1’, then the namespace may be attached to two or more controllers in the NVM subsystem concurrently (i.e., may be a shared namespace). If cleared to ‘0’, then the namespace is a private namespace and is able to be attached to only one controller at a time.</td></tr>
</table>

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
31	O	**Reservation Capabilities (RESCAP):** This field indicates the reservation capabilities of the namespace. A value of 0h in this field indicates that reservations are not supported by this namespace. Refer to section 8.8 for more details. Bit 7 if set to '1' indicates that Ignore Existing Key is used as defined in revision 1.3 or later of this specification. Bit 7 if cleared to '0' indicates that Ignore Existing Key is used as defined in revision 1.2.1 or earlier of this specification. This bit shall be set to '1' if the controller supports revision 1.3 or later as indicated in the Version register. Bit 6 if set to '1' indicates that the namespace supports the Exclusive Access – All Registrants reservation type. If this bit is cleared to '0', then the namespace does not support the Exclusive Access – All Registrants reservation type. Bit 5 if set to '1' indicates that the namespace supports the Write Exclusive – All Registrants reservation type. If this bit is cleared to '0', then the namespace does not support the Write Exclusive – All Registrants reservation type. Bit 4 if set to '1' indicates that the namespace supports the Exclusive Access – Registrants Only reservation type. If this bit is cleared to '0', then the namespace does not support the Exclusive Access – Registrants Only reservation type. Bit 3 if set to '1' indicates that the namespace supports the Write Exclusive – Registrants Only reservation type. If this bit is cleared to '0', then the namespace does not support the Write Exclusive – Registrants Only reservation type. Bit 2 if set to '1' indicates that the namespace supports the Exclusive Access reservation type. If this bit is cleared to '0', then the namespace does not support the Exclusive Access reservation type. Bit 1 if set to '1' indicates that the namespace supports the Write Exclusive reservation type. If this bit is cleared to '0', then the namespace does not support the Write Exclusive reservation type. Bit 0 if set to '1' indicates that the namespace supports the Persist Through Power Loss capability. If this bit is cleared to '0', then the namespace does not support the Persist Through Power Loss Capability.
32	O	**Format Progress Indicator (FPI):** If a format operation is in progress, this field indicates the percentage of the namespace that remains to be formatted. Bit 7 if set to '1' indicates that the namespace supports the Format Progress Indicator defined by bits 6:0 in this field. If this bit is cleared to '0', then the namespace does not support the Format Progress Indicator and bits 6:0 in this field shall be cleared to 0h. Bits 6:0 indicate the percentage of the Format NVM command that remains to be completed (e.g., a value of 25 indicates that 75% of the Format NVM command has been completed and 25% remains to be completed). If bit 7 is set to '1', then a value of 0h indicates that the namespace is formatted with the format specified by the FLBAS and DPS fields in this data structure and there is no Format NVM command in progress.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

<table>
<tr><th>Bytes</th><th>O/M [1]</th><th>Description</th></tr>
<tr><td>33</td><td>O</td><td>Deallocate Logical Block Features (DLFEAT): This field indicates information about features that affect deallocating logical blocks for this namespace.

Bits 7:5 are reserved.

Bit 4 if set to ‘1’ indicates that the Guard field for deallocated logical blocks that contain protection information is set to the CRC for the value read from the deallocated logical block and its metadata (excluding protection information). If cleared to ‘0’ indicates that the Guard field for the deallocated logical blocks that contain protection information is set to FFFFh.

Bit 3 if set to ‘1’ indicates that the controller supports the Deallocate bit in the Write Zeroes command for this namespace. If cleared to ‘0’ indicates that the controller does not support the Deallocate bit in the Write Zeroes command for this namespace. This bit shall be set to the same value for all namespaces in the NVM subsystem.

Bits 2:0 indicate deallocated logical block read behavior. For a logical block that is deallocated, this field indicates the values read from that deallocated logical block and its metadata (excluding protection information). The values for this field have the following meanings:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>The read behavior is not reported</td></tr>
<tr><td>001b</td><td>A deallocated logical block returns all bytes cleared to 0h</td></tr>
<tr><td>010b</td><td>A deallocated logical block returns all bytes set to FFh</td></tr>
<tr><td>011b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>35:34</td><td>O</td><td>Namespace Atomic Write Unit Normal (NAWUN): This field indicates the namespace specific size of the write operation guaranteed to be written atomically to the NVM during normal operation. If the NSABP bit is cleared to ‘0’, then this field is reserved.

A value of 0h indicates that the size for this namespace is the same size as that reported in the AWUN field of the Identify Controller data structure. All other values specify a size in terms of logical blocks using the same encoding as the AWUN field. Refer to section 6.4.</td></tr>
<tr><td>37:36</td><td>O</td><td>Namespace Atomic Write Unit Power Fail (NAWUPF): This field indicates the namespace specific size of the write operation guaranteed to be written atomically to the NVM during a power fail or error condition. If the NSABP bit is cleared to ‘0’, then this field is reserved.

A value of 0h indicates that the size for this namespace is the same size as that reported in the AWUPF field of the Identify Controller data structure. All other values specify a size in terms of logical blocks using the same encoding as the AWUPF field. Refer to section 6.4.</td></tr>
<tr><td>39:38</td><td>O</td><td>Namespace Atomic Compare & Write Unit (NACWU): This field indicates the namespace specific size of the write operation guaranteed to be written atomically to the NVM for a Compare and Write fused command. If the NSABP bit is cleared to ‘0’, then this field is reserved.

A value of 0h indicates that the size for this namespace is the same size as that reported in the ACWU field of the Identify Controller data structure. All other values specify a size in terms of logical blocks using the same encoding as the ACWU field. Refer to section 6.4.</td></tr>
</table>

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
41:40	O	**Namespace Atomic Boundary Size Normal (NABSN):** This field indicates the atomic boundary size for this namespace for the NAWUN value. This field is specified in logical blocks. Writes to this namespace that cross atomic boundaries are not guaranteed to be atomic to the NVM with respect to other read or write commands. A value of 0h indicates that there are no atomic boundaries for normal write operations. All other values specify a size in terms of logical blocks using the same encoding as the AWUN field. Refer to section 6.4. Refer to section 8.25 for how this field is utilized.
43:42	O	**Namespace Atomic Boundary Offset (NABO):** This field indicates the LBA on this namespace where the first atomic boundary starts. If the NABSN and NABSPF fields are cleared to 0h, then the NABO field shall be cleared to 0h. NABO shall be less than or equal to NABSN and NABSPF. Refer to section 6.4. Refer to section 8.25 for how this field is utilized.
45:44	O	**Namespace Atomic Boundary Size Power Fail (NABSPF):** This field indicates the atomic boundary size for this namespace specific to the Namespace Atomic Write Unit Power Fail value. This field is specified in logical blocks. Writes to this namespace that cross atomic boundaries are not guaranteed to be atomic with respect to other read or write commands and there is no guarantee of data returned on subsequent reads of the associated logical blocks. A value of 0h indicates that there are no atomic boundaries for power fail or error conditions. All other values specify a size in terms of logical blocks using the same encoding as the AWUPF field. Refer to section 6.4.
47:46	O	**Namespace Optimal I/O Boundary (NOIOB):** This field indicates the optimal I/O boundary for this namespace. This field is specified in logical blocks. The host should construct Read and Write commands that do not cross the I/O boundary to achieve optimal performance. A value of 0h indicates that no optimal I/O boundary is reported. Refer to section 8.25 for how this field is utilized to improve performance and endurance.
63:48	O	**NVM Capacity (NVMCAP):** This field indicates the total size of the NVM allocated to this namespace. The value is in bytes. This field shall be supported if the Namespace Management capability (refer to section 8.12) is supported. Note: This field may not correspond to the logical block size multiplied by the Namespace Size field. Due to thin provisioning or other settings (e.g., endurance), this field may be larger or smaller than the product of the logical block size and the Namespace Size reported. If the controller supports Asymmetric Namespace Access Reporting (refer to the CMIC field), and the relationship between the controller and the namespace is in the ANA Inaccessible state (refer to section 8.20.3.3) or the ANA Persistent Loss state (refer to section 8.20.3.4), then this field shall be cleared to 0h.
65:64	O	**Namespace Preferred Write Granularity (NPWG):** This field indicates the smallest recommended write granularity in logical blocks for this namespace. This is a 0's based value. If the OPTPEFT bit is cleared to '0', then this field is reserved. The size indicated should be less than or equal to Maximum Data Transfer Size (MDTS) that is specified in units of minimum memory page size. The value of this field may change if the namespace is reformatted. The size should be a multiple of Namespace Preferred Write Alignment (NPWA). Refer to section 8.25 for how this field is utilized to improve performance and endurance.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
67:66	O	**Namespace Preferred Write Alignment (NPWA):** This field indicates the recommended write alignment in logical blocks for this namespace. This is a 0's based value. The value of this field may change if the namespace is reformatted. Refer to section 8.25 for how this field is utilized to improve performance and endurance.
69:68	O	**Namespace Preferred Deallocate Granularity (NPDG):** This field indicates the recommended granularity in logical blocks for the Dataset Management command with the Attribute – Deallocate bit set to '1' in Dword 11.This is a 0's based value. If the OPTPEFT bit is cleared to '0', then this field is reserved. The value of this field may change if the namespace is reformatted. The size should be a multiple of Namespace Preferred Deallocate Alignment (NPDA). Refer to section 8.25 for how this field is utilized to improve performance and endurance.
71:70	O	**Namespace Preferred Deallocate Alignment (NPDA):** This field indicates the recommended alignment in logical blocks for the Dataset Management command with the Attribute – Deallocate bit set to '1' in Dword 11.This is a 0's based value. If the OPTPEFT bit is cleared to '0', then this field is reserved. The value of this field may change if the namespace is reformatted. Refer to section 8.25 for how this field is utilized to improve performance and endurance.
73:72	O	**Namespace Optimal Write Size (NOWS):** This field indicates the size in logical blocks for optimal write performance for this namespace. This is a 0's based value. If the OPTPEFT bit is cleared to '0', then this field is reserved. The size indicated should be less than or equal to Maximum Data Transfer Size (MDTS) that is specified in units of minimum memory page size. The value of this field may change if the namespace is reformatted. The value of this field should be a multiple of Namespace Preferred Write Granularity (NPWG). If the namespace is associated with an NVM set, NOWS defined for this namespace shall be set to the Optimal Write Size field setting defined in NVM Set Attributes Entry (refer to Figure 255) for the NVM Set with which this namespace is associated. If NOWS is not supported, the Optimal Write Size field in NVM Sets Attributes Entry (refer to Figure 255) for the NVM Set with which this namespace is associated should be used by the host for I/O optimization. Refer to section 8.25 for how this field is utilized to improve performance and endurance.
91:74		Reserved
95:92	O	**ANA Group Identifier (ANAGRPID):** This field indicates the ANA Group Identifier of the ANA group (refer to section 8.20.2) of which the namespace is a member. Each namespace that is attached to a controller that supports Asymmetric Namespace Access Reporting (refer to the CMIC field) shall report a valid ANAGRPID. If the controller does not support Asymmetric Namespace Access Reporting, then this field shall be cleared to 0h. If the value in this field changes and Asymmetric Namespace Access Change Notices are supported and enabled, then the controller shall issue an Asymmetric Namespace Access Change Notice.
98:96		Reserved
99	O	**Namespace Attributes (NSATTR):** This field specifies attributes of the namespace. Bits 7:1 are reserved. Bit 0: If set to '1', then the namespace is currently write protected due to any condition (e.g., namespace write protection set for the namespace, media errors) and all write access to the namespace shall fail. If cleared to '0', then the namespace is not currently write protected.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
101:100	O	**NVM Set Identifier (NVMSETID):** This field indicates the NVM Set with which this namespace is associated. If NVM Sets are not supported by the controller, then this field shall be cleared to 0h.
103:102	O	**Endurance Group Identifier (ENDGID):** This field indicates the Endurance Group with which this namespace is associated. If Endurance Groups are not supported by the controller, then this field shall be cleared to 0h.
119:104	O	**Namespace Globally Unique Identifier (NGUID):** This field contains a 128-bit value that is globally unique and assigned to the namespace when the namespace is created. This field remains fixed throughout the life of the namespace and is preserved across namespace and controller operations (e.g., Controller Level Reset, namespace format, etc.). This field uses the EUI-64 based 16-byte designator format. Bytes 114:112 contain the 24-bit Organizationally Unique Identifier (OUI) value assigned by the IEEE Registration Authority. Bytes 119:115 contain an extension identifier assigned by the corresponding organization. Bytes 111:104 contain the vendor specific extension identifier assigned by the corresponding organization. Refer to the IEEE EUI-64 guidelines for more information. This field is big endian (refer to section 7.10.5). The controller shall specify a globally unique namespace identifier in this field, the EUI64 field, or a Namespace UUID in the Namespace Identification Descriptor (refer to Figure 253) when the namespace is created. If the controller is not able to provide a globally unique identifier in this field, then this field shall be cleared to 0h. Refer to section 7.11.
127:120	O	**IEEE Extended Unique Identifier (EUI64):** This field contains a 64-bit IEEE Extended Unique Identifier (EUI-64) that is globally unique and assigned to the namespace when the namespace is created. This field remains fixed throughout the life of the namespace and is preserved across namespace and controller operations (e.g., Controller Level Reset, namespace format, etc.). The EUI-64 is a concatenation of a 24-bit or 36-bit Organizationally Unique Identifier (OUI or OUI-36) value assigned by the IEEE Registration Authority and an extension identifier assigned by the corresponding organization. Refer to the IEEE EUI-64 guidelines for more information. This field is big endian (refer to section 7.10.4). The controller shall specify a globally unique namespace identifier in this field, the NGUID field, or a Namespace UUID in the Namespace Identification Descriptor (refer to Figure 253) when the namespace is created. If the controller is not able to provide a globally unique 64-bit identifier in this field, then this field shall be cleared to 0h. Refer to section 7.11.
131:128	M	**LBA Format 0 Support (LBAF0):** This field indicates the LBA format 0 that is supported by the controller. The LBA format field is defined in Figure 250.
135:132	O	**LBA Format 1 Support (LBAF1):** This field indicates the LBA format 1 that is supported by the controller. The LBA format field is defined in Figure 250.
139:136	O	**LBA Format 2 Support (LBAF2):** This field indicates the LBA format 2 that is supported by the controller. The LBA format field is defined in Figure 250.
143:140	O	**LBA Format 3 Support (LBAF3):** This field indicates the LBA format 3 that is supported by the controller. The LBA format field is defined in Figure 250.
147:144	O	**LBA Format 4 Support (LBAF4):** This field indicates the LBA format 4 that is supported by the controller. The LBA format field is defined in Figure 250.
151:148	O	**LBA Format 5 Support (LBAF5):** This field indicates the LBA format 5 that is supported by the controller. The LBA format field is defined in Figure 250.
155:152	O	**LBA Format 6 Support (LBAF6):** This field indicates the LBA format 6 that is supported by the controller. The LBA format field is defined in Figure 250.
159:156	O	**LBA Format 7 Support (LBAF7):** This field indicates the LBA format 7 that is supported by the controller. The LBA format field is defined in Figure 250.
163:160	O	**LBA Format 8 Support (LBAF8):** This field indicates the LBA format 8 that is supported by the controller. The LBA format field is defined in Figure 250.

Figure 249: Identify – Identify Namespace Data Structure, NVM Command Set Specific

Bytes	O/M [1]	Description
167:164	O	**LBA Format 9 Support (LBAF9):** This field indicates the LBA format 9 that is supported by the controller. The LBA format field is defined in Figure 250.
171:168	O	**LBA Format 10 Support (LBAF10):** This field indicates the LBA format 10 that is supported by the controller. The LBA format field is defined in Figure 250.
175:172	O	**LBA Format 11 Support (LBAF11):** This field indicates the LBA format 11 that is supported by the controller. The LBA format field is defined in Figure 250.
179:176	O	**LBA Format 12 Support (LBAF12):** This field indicates the LBA format 12 that is supported by the controller. The LBA format field is defined in Figure 250.
183:180	O	**LBA Format 13 Support (LBAF13):** This field indicates the LBA format 13 that is supported by the controller. The LBA format field is defined in Figure 250.
187:184	O	**LBA Format 14 Support (LBAF14):** This field indicates the LBA format 14 that is supported by the controller. The LBA format field is defined in Figure 250.
191:188	O	**LBA Format 15 Support (LBAF15):** This field indicates the LBA format 15 that is supported by the controller. The LBA format field is defined in Figure 250.
383:192		Reserved
4095:384	O	Vendor Specific

NOTES:
1. O/M definition: O = Optional, M = Mandatory.

The LBA format data structure is described in Figure 250.

Figure 250: Identify – LBA Format Data Structure, NVM Command Set Specific

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:26</td><td>Reserved</td></tr>
<tr><td>25:24</td><td>Relative Performance (RP): This field indicates the relative performance of the LBA format indicated relative to other LBA formats supported by the controller. Depending on the size of the LBA and associated metadata, there may be performance implications. The performance analysis is based on better performance on a queue depth 32 with 4 KiB read workload. The meanings of the values indicated are included in the following table.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>Best performance</td></tr>
<tr><td>01b</td><td>Better performance</td></tr>
<tr><td>10b</td><td>Good performance</td></tr>
<tr><td>11b</td><td>Degraded performance</td></tr>
</table></td></tr>
<tr><td>23:16</td><td>LBA Data Size (LBADS): This field indicates the LBA data size supported. The value is reported in terms of a power of two (2^n). A value smaller than 9 (i.e., 512 bytes) is not supported. If the value reported is 0h, then the LBA format is not supported / used or is not currently available.</td></tr>
<tr><td>15:00</td><td>Metadata Size (MS): This field indicates the number of metadata bytes provided per LBA based on the LBA Data Size indicated. If there is no metadata supported, then this field shall be cleared to 0h.

If metadata is supported, then the namespace may support the metadata being transferred as part of an extended data LBA or as part of a separate contiguous buffer. If end-to-end data protection is enabled, then the first eight bytes or last eight bytes of the metadata is the protection information (refer to the DPS field in the Identify Namespace data structure).</td></tr>
</table>

5.15.2.2 Identify Controller data structure (CNS 01h)

The Identify Controller data structure (refer to Figure 251) is returned to the host for the controller.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
Controller Capabilities and Features		
01:00	M	**PCI Vendor ID (VID):** Contains the company vendor identifier that is assigned by the PCI SIG. This is the same value as reported in the ID register in section 2.1.1.
03:02	M	**PCI Subsystem Vendor ID (SSVID):** Contains the company vendor identifier that is assigned by the PCI SIG for the subsystem. This is the same value as reported in the SS register in section 2.1.17.
23:04	M	**Serial Number (SN):** Contains the serial number for the NVM subsystem that is assigned by the vendor as an ASCII string. Refer to section 7.10 for unique identifier requirements. Refer to section 1.5 for ASCII string requirements.
63:24	M	**Model Number (MN):** Contains the model number for the NVM subsystem that is assigned by the vendor as an ASCII string. Refer to section 7.10 for unique identifier requirements. Refer to section 1.5 for ASCII string requirements.
71:64	M	**Firmware Revision (FR):** Contains the currently active firmware revision, as an ASCII string, for the NVM subsystem. This is the same revision information that may be retrieved with the Get Log Page command, refer to section 5.14.1.3.
72	M	**Recommended Arbitration Burst (RAB):** This is the recommended Arbitration Burst size. The value is in commands and is reported as a power of two (2^*n*). This is the same units as the Arbitration Burst size. Refer to section 4.13.
75:73	M	**IEEE OUI Identifier (IEEE):** Contains the Organization Unique Identifier (OUI) for the controller vendor. The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.
76	O	**Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC):** This field specifies multi-path I/O and namespace sharing capabilities of the controller and NVM subsystem. Bits 7:4 are reserved. Bit 3 if set to '1', then the NVM subsystem supports Asymmetric Namespace Access Reporting (refer to section 8.20). If cleared to '0', then the NVM subsystem does not support Asymmetric Namespace Access Reporting. Bit 2 if set to '1', then the controller is associated with an SR-IOV Virtual Function. If cleared to '0', then the controller is associated with a PCI Function or a Fabrics connection. Bit 1 if set to '1', then the NVM subsystem may contain two or more controllers. If cleared to '0', then the NVM subsystem contains only a single controller. As described in section 1.4.1, an NVM subsystem that contains multiple controllers may be used by multiple hosts, or may provide multiple paths for a single host. Bit 0 if set to '1', then the NVM subsystem may contain more than one NVM subsystem port. If cleared to '0', then the NVM subsystem contains only a single NVM subsystem port.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
77	M	**Maximum Data Transfer Size (MDTS):** This field indicates the maximum data transfer size for a command that transfers data between host-accessible memory (refer to section 1.6.17) and the controller. The host should not submit a command that exceeds this maximum data transfer size. If a command is submitted that exceeds this transfer size, then the command is aborted with a status of Invalid Field in Command. The value is in units of the minimum memory page size (CAP.MPSMIN) and is reported as a power of two (2^*n*). A value of 0h indicates that there is no maximum data transfer size. This field includes the length of metadata, if metadata is interleaved with the logical block data. This field does not apply to commands that do not transfer data between host-accessible memory and the controller (e.g., the Verify command, the Write Uncorrectable command, and the Write Zeroes command); there is no maximum data transfer size for those commands. If SGL Bit Bucket descriptors are supported, their lengths shall be included in determining if a command exceeds the Maximum Data Transfer Size for destination data buffers. Their length in a source data buffer is not included for a Maximum Data Transfer Size calculation.
79:78	M	**Controller ID (CNTLID):** Contains the NVM subsystem unique controller identifier associated with the controller.
83:80	M	**Version (VER):** This field contains the value reported in the Version register defined in section 3.1.2. Implementations compliant to revision 1.2 or later of this specification shall report a non-zero value in this field.
87:84	M	**RTD3 Resume Latency (RTD3R):** This field indicates the expected latency in microseconds to resume from Runtime D3 (RTD3). Refer to section 8.4.4. A value of 0h indicates RTD3 Resume Latency is not reported.
91:88	M	**RTD3 Entry Latency (RTD3E):** This field indicates the typical latency in microseconds to enter Runtime D3 (RTD3). Refer to section 8.4.4. A value of 0h indicates RTD3 Entry Latency is not reported.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
95:92	M	**Optional Asynchronous Events Supported (OAES):** This field indicates the optional asynchronous events supported by the controller. A controller shall not send optional asynchronous events before they are enabled by host software. Bits 31:15 are reserved. Bit 14 is set to '1' if the controller supports the Endurance Group Event Aggregate Log Page Change Notices event. If cleared to '0', then the controller does not support the Endurance Group Event Aggregate Log Page Change Notices event. Bit 13 is set to '1' if the controller supports the LBA Status Information Notices event. If cleared to '0', then the controller does not support the LBA Status Information Notices event. Bit 12 is set to '1' if the controller supports the Predictable Latency Event Aggregate Log Change Notices event. If cleared to '0', then the controller does not support the Predictable Latency Event Aggregate Log Change Notices event. Bit 11 is set to '1' if the controller supports sending Asymmetric Namespace Access Change Notices. If cleared to '0', then the controller does not support the Asymmetric Namespace Access Change Notices event. Bit 10 is reserved. Bit 9 is set to '1' if the controller supports the Firmware Activation Notices event. If cleared to '0', then the controller does not support the Firmware Activation Notices event. Bit 8 is set to '1' if the controller supports the Namespace Attribute Notices event and the associated Changed Namespace List log page. If cleared to '0', then the controller does not support the Namespace Attribute Notices event nor the associated Changed Namespace List log page. Bits 7:0 are reserved.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
99:96	M	**Controller Attributes (CTRATT):** This field indicates attributes of the controller. Bits 31:10 are reserved. Bit 9 **(UUID List):** If set to '1', then the controller supports reporting of a UUID List (refer to Figure 261). If cleared to '0', then the controller does not support reporting of a UUID List (refer to section 8.24). Bit 8 **(SQ Associations):** If set to '1', then the controller supports SQ Associations (refer to section 8.23). If cleared to '0', then the controller does not support SQ Associations. Bit 7 **(Namespace Granularity):** If set to '1', then the controller supports reporting of Namespace Granularity (refer to section 5.15.2.12). If cleared to '0', the controller does not support reporting of Namespace Granularity. If the Namespace Management capability (refer to section 8.12) is not supported, then this bit shall be cleared to '0'. Bit 6 **(Traffic Based Keep Alive Support – TBKAS):** If set to '1', then the controller supports restarting the Keep Alive Timer if an Admin command or an I/O command is processed during the Keep Alive Timeout Interval (refer to section 7.12.2). If cleared to '0', then the controller supports restarting the Keep Alive Timer only if a Keep Alive command is processed during the Keep Alive Timeout Interval (refer to section 7.12.1). Bit 5 **(Predictable Latency Mode):** If set to '1', then the controller supports Predictable Latency Mode (refer to section 8.18). If cleared to '0', then the controller does not support Predictable Latency Mode. Bit 4 **(Endurance Groups):** If set to '1', then the controller supports Endurance Groups (refer to section 8.17). If cleared to '0', then the controller does not support Endurance Groups. Bit 3 **(Read Recovery Levels):** If set to '1', then the controller supports Read Recovery Levels (refer to section 8.16). If cleared to '0', then the controller does not support Read Recovery Levels. Bit 2 **(NVM Sets):** If set to '1', then the controller supports NVM Sets (refer to section 4.9). If cleared to '0', then the controller does not support NVM Sets. Bit 1 **(Non-Operational Power State Permissive Mode):** If set to '1', then the controller supports host control of whether the controller may temporarily exceed the power of a non-operational power state for the purpose of executing controller initiated background operations in a non-operational power state (i.e., Non-Operational Power State Permissive Mode supported). If cleared to '0', then the controller does not support host control of whether the controller may exceed the power of a non-operational state for the purpose of executing controller initiated background operations in a non-operational state (i.e., Non-Operational Power State Permissive Mode not supported). Refer to section 5.21.1.17. Bit 0 if set to '1', then the controller supports a 128-bit Host Identifier. Bit 0 if cleared to '0', then the controller does not support a 128-bit Host Identifier.

Figure 251: Identify – Identify Controller Data Structure

<table>
<tr><th>Bytes</th><th>O/M [1]</th><th>Description</th></tr>
<tr><td>101:100</td><td>O</td><td>Read Recovery Levels Supported (RRLS): If Read Recovery Levels (RRL) are supported, then this field shall be supported. If a bit is set to ‘1’, then the corresponding Read Recovery Level is supported. If a bit is cleared to ‘0’, then the corresponding Read Recovery Level is not supported.
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>0</td><td>Read Recovery Level 0</td></tr>
<tr><td>1</td><td>Read Recovery Level 1</td></tr>
<tr><td>2</td><td>Read Recovery Level 2</td></tr>
<tr><td>3</td><td>Read Recovery Level 3</td></tr>
<tr><td>4</td><td>Read Recovery Level 4 – Default[1]</td></tr>
<tr><td>5</td><td>Read Recovery Level 5</td></tr>
<tr><td>6</td><td>Read Recovery Level 6</td></tr>
<tr><td>7</td><td>Read Recovery Level 7</td></tr>
<tr><td>8</td><td>Read Recovery Level 8</td></tr>
<tr><td>9</td><td>Read Recovery Level 9</td></tr>
<tr><td>10</td><td>Read Recovery Level 10</td></tr>
<tr><td>11</td><td>Read Recovery Level 11</td></tr>
<tr><td>12</td><td>Read Recovery Level 12</td></tr>
<tr><td>13</td><td>Read Recovery Level 13</td></tr>
<tr><td>14</td><td>Read Recovery Level 14</td></tr>
<tr><td>15</td><td>Read Recovery Level 15 – Fast Fail[1]</td></tr>
<tr><td colspan="2">NOTE:
1. If Read Recovery Levels are supported, then this bit shall be set to ‘1’.</td></tr>
</table></td></tr>
<tr><td>110:102</td><td></td><td>Reserved</td></tr>
<tr><td>111</td><td>M</td><td>Controller Type (CNTRLTYPE): This field specifies the controller type. A value of 0h indicates that the controller type is not reported.

Implementations compliant to version 1.4 or later of this specification shall report a controller type (i.e., the value 0h is reserved and shall not be used). Implementations compliant to an earlier specification version may report a value of 0h to indicate that a controller type is not reported.
<table>
<tr><th>Value</th><th>Controller Type</th></tr>
<tr><td>0h</td><td>Reserved (controller type not reported)</td></tr>
<tr><td>1h</td><td>I/O Controller</td></tr>
<tr><td>2h</td><td>Discovery Controller</td></tr>
<tr><td>3h</td><td>Administrative Controller</td></tr>
<tr><td>4h to FFh</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
127:112	O	**FRU Globally Unique Identifier (FGUID):** This field contains a 128-bit value that is globally unique for a given Field Replaceable Unit (FRU). Refer to the NVM Express™ Management Interface (NVMe-MI™) specification for the definition of a FRU. This field remains fixed throughout the life of the FRU. This field shall contain the same value for each controller associated with a given FRU. This field uses the EUI-64 based 16-byte designator format. Bytes 122:120 contain the 24-bit Organizationally Unique Identifier (OUI) value assigned by the IEEE Registration Authority. Bytes 127:123 contain an extension identifier assigned by the corresponding organization. Bytes 119:112 contain the vendor specific extension identifier assigned by the corresponding organization. Refer to the IEEE EUI-64 guidelines for more information. This field is big endian (refer to section 7.10). When not implemented, this field contains a value of 0h.
129:128	O	**Command Retry Delay Time 1 (CRDT1):** If the Do Not Retry (DNR) bit is cleared to '0' in the CQE and the Command Retry Delay (CRD) field is set to 01b in the CQE, then this value indicates the command retry delay time in units of 100 milliseconds.
131:130	O	**Command Retry Delay Time 2 (CRDT2):** If the DNR bit is cleared to '0' in the CQE and the CRD field is set to 10b in the CQE, then this value indicates the command retry delay time in units of 100 milliseconds.
133:132	O	**Command Retry Delay Time 3 (CRDT3):** If the DNR bit is cleared to '0' in the CQE and CRD field is set to 11b in the CQE, then this value indicates the command retry delay time in units of 100 milliseconds.
239:134		Reserved
255:240		Refer to the NVMe Management Interface Specification for definition.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
Admin Command Set Attributes & Optional Controller Capabilities		
257:256	M	**Optional Admin Command Support (OACS):** This field indicates the optional Admin commands and features supported by the controller. Refer to section 5. Bits 15:10 are reserved. Bit 9 if set to '1', then the controller supports the Get LBA Status capability (refer to section 8.22). If cleared to '0', then the controller does not support the Get LBA Status capability. Bit 8 if set to '1', then the controller supports the Doorbell Buffer Config command. If cleared to '0', then the controller does not support the Doorbell Buffer Config command. Bit 7 if set to '1', then the controller supports the Virtualization Management command. If cleared to '0', then the controller does not support the Virtualization Management command. Bit 6 if set to '1', then the controller supports the NVMe-MI Send and NVMe-MI Receive commands. If cleared to '0', then the controller does not support the NVMe-MI Send and NVMe-MI Receive commands. Bit 5 if set to '1', then the controller supports Directives. If cleared to '0', then the controller does not support Directives. A controller that supports Directives shall support the Directive Send and Directive Receive commands. Refer to section 9. Bit 4 if set to '1', then the controller supports the Device Self-test command. If cleared to '0', then the controller does not support the Device Self-test command. Bit 3 if set to '1', then the controller supports the Namespace Management capability (refer to section 8.12). If cleared to '0', then the controller does not support the Namespace Management capability. Bit 2 if set to '1', then the controller supports the Firmware Commit and Firmware Image Download commands. If cleared to '0', then the controller does not support the Firmware Commit and Firmware Image Download commands. Bit 1 if set to '1', then the controller supports the Format NVM command. If cleared to '0', then the controller does not support the Format NVM command. Bit 0 if set to '1', then the controller supports the Security Send and Security Receive commands. If cleared to '0', then the controller does not support the Security Send and Security Receive commands.
258	M	**Abort Command Limit (ACL):** This field is used to convey the maximum number of concurrently executing Abort commands supported by the controller (refer to section 5.1). This is a 0's based value. It is recommended that implementations support concurrent execution of a minimum of four Abort commands.
259	M	**Asynchronous Event Request Limit (AERL):** This field is used to convey the maximum number of concurrently outstanding Asynchronous Event Request commands supported by the controller (refer to section 5.2). This is a 0's based value. It is recommended that implementations support a minimum of four Asynchronous Event Request Limit commands outstanding simultaneously.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
260	M	**Firmware Updates (FRMW):** This field indicates capabilities regarding firmware updates. Refer to section 8.1 for more information on the firmware update process. Bits 7:5 are reserved. Bit 4 if set to '1' indicates that the controller supports firmware activation without a reset. If cleared to '0', then the controller requires a reset for firmware to be activated. Bits 3:1 indicate the number of firmware slots that the controller supports. This field shall specify a value from one to seven, indicating that at least one firmware slot is supported and up to seven maximum. This corresponds to firmware slots 1 through 7. Bit 0 if set to '1' indicates that the first firmware slot (i.e., slot 1) is read only. If cleared to '0', then the first firmware slot (i.e., slot 1) is read/write. Implementations may choose to have a baseline read only firmware image.
261	M	**Log Page Attributes (LPA):** This field indicates optional attributes for log pages that are accessed via the Get Log Page command. Bits 7:5 are reserved. Bit 4 if set to '1', then the controller supports the Persistent Event log. If cleared to '0', then the controller does not support the Persistent Event log. Bit 3 if set to '1', then the controller supports the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and sending Telemetry Log Notices. If cleared to '0', then the controller does not support the Telemetry Host-Initiated and Telemetry Controller-Initiated log pages and Telemetry Log Notice events. Bit 2 if set to '1', then the controller supports extended data for the Get Log Page command (including extended Number of Dwords and Log Page Offset fields). Bit 2 if cleared to '0', then the controller does not support extended data for the Get Log Page command. Bit 1 if set to '1', then the controller supports the Commands Supported and Effects log page. Bit 1 if cleared to '0', then the controller does not support the Commands Supported and Effects log page. Bit 0 if set to '1', then the controller supports the SMART / Health Information log page on a per namespace basis. If cleared to '0', then the controller does not support the SMART / Health Information log page on a per namespace basis.
262	M	**Error Log Page Entries (ELPE):** This field indicates the maximum number of Error Information log entries that are stored by the controller. This field is a 0's based value.
263	M	**Number of Power States Support (NPSS):** This field indicates the number of NVM Express power states supported by the controller. This is a 0's based value. Refer to section 8.4. Power states are numbered sequentially starting at power state 0. A controller shall support at least one power state (i.e., power state 0) and may support up to 31 additional power states (i.e., up to 32 total).
264	M	**Admin Vendor Specific Command Configuration (AVSCC):** This field indicates the configuration settings for Admin Vendor Specific command handling. Refer to section 8.7. Bits 7:1 are reserved. Bit 0 if set to '1' indicates that all Admin Vendor Specific Commands use the format defined in Figure 107. If cleared to '0' indicates that the format of all Admin Vendor Specific Commands are vendor specific.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
265	O	**Autonomous Power State Transition Attributes (APSTA):** This field indicates the attributes of the autonomous power state transition feature. Refer to section 8.4.2. Bits 7:1 are reserved. Bit 0 if set to '1', then the controller supports autonomous power state transitions. If cleared to '0', then the controller does not support autonomous power state transitions.
267:266	M	**Warning Composite Temperature Threshold (WCTEMP):** This field indicates the minimum Composite Temperature field value (reported in the SMART / Health Information log in Figure 198) that indicates an overheating condition during which controller operation continues. Immediate remediation is recommended (e.g., additional cooling or workload reduction). The platform should strive to maintain a composite temperature less than this value. A value of 0h in this field indicates that no warning temperature threshold value is reported by the controller. Implementations compliant to revision 1.2 or later of this specification shall report a non-zero value in this field. It is recommended that implementations report a value of 0157h in this field.
269:268	M	**Critical Composite Temperature Threshold (CCTEMP):** This field indicates the minimum Composite Temperature field value (reported in the SMART / Health Information log in Figure 198) that indicates a critical overheating condition (e.g., may prevent continued normal operation, possibility of data loss, automatic device shutdown, extreme performance throttling, or permanent damage). A value of 0h in this field indicates that no critical temperature threshold value is reported by the controller. Implementations compliant to revision 1.2 or later of this specification shall report a non-zero value in this field.
271:270	O	**Maximum Time for Firmware Activation (MTFA):** Indicates the maximum time the controller temporarily stops processing commands to activate the firmware image. This field shall be valid if the controller supports firmware activation without a reset. This field is specified in 100 millisecond units. A value of 0h indicates that the maximum time is undefined.
275:272	O	**Host Memory Buffer Preferred Size (HMPRE):** This field indicates the preferred size that the host is requested to allocate for the Host Memory Buffer feature in 4 KiB units. This value shall be greater than or equal to the Host Memory Buffer Minimum Size. If this field is non-zero, then the Host Memory Buffer feature is supported. If this field is cleared to 0h, then the Host Memory Buffer feature is not supported.
279:276	O	**Host Memory Buffer Minimum Size (HMMIN):** This field indicates the minimum size that the host is requested to allocate for the Host Memory Buffer feature in 4 KiB units. If this field is cleared to 0h, then the host is requested to allocate any amount of host memory possible up to the HMPRE value.
295:280	O	**Total NVM Capacity (TNVMCAP):** This field indicates the total NVM capacity in the NVM subsystem. The value is in bytes. This field shall be supported if the Namespace Management capability (refer to section 8.12) is supported.
311:296	O	**Unallocated NVM Capacity (UNVMCAP):** This field indicates the unallocated NVM capacity in the NVM subsystem. The value is in bytes. This field shall be supported if the Namespace Management capability (refer to section 8.12) is supported.

Figure 251: Identify – Identify Controller Data Structure

<table>
<tr><th>Bytes</th><th>O/M [1]</th><th>Description</th></tr>
<tr><td>315:312</td><td>O</td><td>Replay Protected Memory Block Support (RPMBS): This field indicates if the controller supports one or more Replay Protected Memory Blocks (RPMBs) and the capabilities. Refer to section 8.10.

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:24</td><td>Access Size: If the Number of RPMB Units field is non-zero, then this field indicates the maximum number of 512B units of data that may be read or written per RPMB access by Security Send or Security Receive commands for the controller. This is a 0’s based value. A value of 0h indicates support for one unit of 512B of data.

If the Number of RPMB Units field is 0h, then this field shall be ignored.</td></tr>
<tr><td>23:16</td><td>Total Size: If the Number of RPMB Units field is non-zero, then this field indicates the number of 128 KiB units of data in each RPMB supported in the controller. This is a 0’s based value. A value of 0h indicates support for one unit of 128 KiB of data.

If the Number of RPMB Units field is 0h, this field shall be ignored.</td></tr>
<tr><td>15:06</td><td>Reserved</td></tr>
<tr><td>05:03</td><td>Authentication Method: This field indicates the authentication method used to access all RPMBs in the controller. The values for this field are:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>HMAC SHA-256 (refer to RFC 6234)</td></tr>
<tr><td>001b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>02:00</td><td>Number of RPMB Units: This field indicates the number of RPMB targets the controller supports. All RPMB targets supported shall have the same capabilities as defined in the RPMBS field. A value of 0h indicates the controller does not support Replay Protected Memory Blocks. If this value is non-zero, then the controller shall support the Security Send and Security Receive commands.</td></tr>
</table>
</td></tr>
<tr><td>317:316</td><td>O</td><td>Extended Device Self-test Time (EDSTT): If the Device Self-test command is supported, then this field indicates the nominal amount of time in one minute units that the controller takes to complete an extended device self-test operation when in power state 0. If the Device Self-test command is not supported, then this field is reserved.</td></tr>
<tr><td>318</td><td>O</td><td>Device Self-test Options (DSTO): This field indicates the optional Device Self-test command or operation behaviors supported by the controller or NVM subsystem.

Bits 7:1 are reserved.

Bit 0 if set to ‘1’, then the NVM subsystem supports only one device self-test operation in progress at a time. If cleared to ‘0’, then the NVM subsystem supports one device self-test operation per controller at a time.</td></tr>
<tr><td>319</td><td>M</td><td>Firmware Update Granularity (FWUG): This field indicates the granularity and alignment requirement of the firmware image being updated by the Firmware Image Download command (refer to section 5.12). If the values specified in the NUMD field or the OFST field in the Firmware Image Download command do not conform to this granularity and alignment requirement, then the firmware update may abort with status of Invalid Field in Command. For the broadest interoperability with host software, it is recommended that the controller set this value to the lowest value possible.

The value is reported in 4 KiB units (e.g., 1h corresponds to 4 KiB, 2h corresponds to 8 KiB). A value of 0h indicates that no information on granularity is provided. A value of FFh indicates there is no restriction (i.e., any granularity and alignment in dwords is allowed).</td></tr>
</table>

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
321:320	M	**Keep Alive Support (KAS):** This field indicates the granularity of the Keep Alive Timer in 100 millisecond units (refer to section 7.12). If this field is cleared to 0h, then the Keep Alive feature is not supported. The Keep Alive feature shall be supported for NVMe over Fabrics implementations as described in section 7.12.
323:322	O	**Host Controlled Thermal Management Attributes (HCTMA):** This field indicates the attributes of the host controlled thermal management feature. Refer to section 8.4.5. Bits 15:1 are reserved. Bit 0 if set to '1', then the controller supports host controlled thermal management. If cleared to '0', then the controller does not support host controlled thermal management. If this bit is set to '1', then the controller shall support the Set Features command and Get Features command with the Feature Identifier field set to 10h.
325:324	O	**Minimum Thermal Management Temperature (MNTMT):** This field indicates the minimum temperature, in degrees Kelvin, that the host may request in the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field of a Set Features command with the Feature Identifier field set to 10h. A value of 0h indicates that the controller does not report this field or the host controlled thermal management feature (refer to section 8.4.5) is not supported.
327:326	O	**Maximum Thermal Management Temperature (MXTMT):** This field indicates the maximum temperature, in degrees Kelvin, that the host may request in the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field of the Set Features command with the Feature Identifier set to 10h. A value of 0h indicates that the controller does not report this field or the host controlled thermal management feature is not supported.

<table>
<tr>
<td>331:328</td>
<td>O</td>
<td>
Sanitize Capabilities (SANICAP): This field indicates attributes for sanitize operations. If the Sanitize command is supported, then this field shall be non-zero. If the Sanitize command is not supported, then this field shall be cleared to 0h. Refer to section 8.15.
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:30</td><td>
No-Deallocate Modifies Media After Sanitize (NODMMAS): This field indicates if media is additionally modified by the NVMe controller after a sanitize operation successfully completes that had been started by a Sanitize command with the No-Deallocate After Sanitize bit set to ‘1’.

The work required for the associated additional media modification is included both in the estimated time for each sanitize operation and in the Sanitize Progress field (refer to Figure 242).
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>Additional media modification after sanitize operation completes successfully is not defined. Only controllers compliant with versions 1.3 and earlier of the specification or that have bits 2:0 of the SANICAP field cleared to 0h shall be allowed to return this value.</td></tr>
<tr><td>01b</td><td>Media is not additionally modified by the NVMe controller after sanitize operation completes successfully.</td></tr>
<tr><td>10b</td><td>Media is additionally modified by the NVMe controller after sanitize operation completes successfully. The Sanitize Operation Completed event does not occur until the additional media modification associated with this field has completed.</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table>
If bits 2:0 of the SANICAP field are cleared to 000b, then the controller shall clear this field to 00b.
</td></tr>
<tr><td>29</td><td>
No-Deallocate Inhibited (NDI): If set to ‘1’ and the No-Deallocate Response Mode bit is set to ‘1’, then the controller deallocates after the sanitize operation even if the No-Deallocate After Sanitize bit is set to ‘1’ in a Sanitize command.

If:
a) this bit is set to ‘1’;
b) the No-Deallocate After Sanitize bit is set to ‘1’ in a Sanitize command, and:
1) the No-Deallocate Response Mode bit (refer to Figure 318) is cleared to ‘0’; and
2) the Sanitize Config Feature (refer to section 5.21.1.23) is not supported,

then the controller aborts the Sanitize command with a status of Invalid Field in Command.

If the No-Deallocate After Sanitize bit is cleared to ‘0’ in a Sanitize command, then the value of this bit has no effect on the processing of that Sanitize command.

If bits 2:0 of the SANICAP field are cleared to 0h, then the controller shall clear this bit to ‘0’.
</td></tr>
</table>
</td>
</tr>
</table>

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
		28:03 Reserved 02 **Overwrite Support (OWS):** If set to '1', then the controller supports the Overwrite sanitize operation. If cleared to '0', then the controller does not support the Overwrite sanitize operation. 01 **Block Erase Support (BES**): If set to '1', then the controller supports the Block Erase sanitize operation. If cleared to '0', then the controller does not support the Block Erase sanitize operation. 00 **Crypto Erase Support (CES):** If set to '1', then the controller supports the Crypto Erase sanitize operation. If cleared to '0', then the controller does not support the Crypto Erase sanitize operation.
335:332	O	**Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS):** This field indicates the minimum usable size of a Host Memory Buffer Descriptor Entry in 4 KiB units. If this field is cleared to 0h, then the controller does not indicate any limitations on the Host Memory Buffer Descriptor Entry size.
337:336	O	**Host Memory Maximum Descriptors Entries (HMMAXD**): This field indicates the number of usable Host Memory Buffer Descriptor Entries. If this field is cleared to 0h, then the controller does not indicate a maximum number of Host Memory Buffer Descriptor Entries.
339:338	O	**NVM Set Identifier Maximum (NSETIDMAX):** This field defines the maximum value of a valid NVM Set Identifier for any controller in the NVM subsystem. The number of NVM Sets supported by the NVM subsystem is less than or equal to NSETIDMAX.
341:340	O	**Endurance Group Identifier Maximum (ENDGIDMAX):** This field defines the maximum value of a valid Endurance Group Identifier for any controller in the NVM subsystem. The number of Endurance Groups supported by the NVM subsystem is less than or equal to ENDGIDMAX.
342	O	**ANA Transition Time (ANATT):** This field indicates the maximum amount of time, in seconds, for a transition between ANA states or the maximum amount of time, in seconds, that the controller reports the ANA change state. If the controller supports Asymmetric Namespace Access Reporting (refer to the CMIC field), then this field shall be set to a non-zero value. If the controller does not support Asymmetric Namespace Access Reporting, then this field shall be cleared to 0h. Refer to section 8.21.4.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
343	O	**Asymmetric Namespace Access Capabilities (ANACAP):** This field indicates the capabilities associated with Asymmetric Namespace Access Reporting (refer to section 8.20). Bit 7 if set to '1', then the controller supports a non-zero value in the ANAGRPID field of the Namespace Management command. If cleared to '0', then the controller does not support a non-zero value in the ANAGRPID field of the Namespace Management command. If the Namespace Management command is not supported, then this bit shall be cleared to '0'. Bit 6 if set to '1', then the ANAGRPID field in the Identify Namespace data structure (refer to Figure 249) does not change while the namespace is attached to any controller. If cleared to '0', then the ANAGRPID field may change while the namespace is attached to any controller. Refer to section 8.20.2. Bit 5 is reserved. Bit 4 if set to '1', then the controller is able to report ANA Change state (refer to section 8.20.3.5). If cleared to '0', then the controller does not report ANA Change state. Bit 3 if set to '1', then the controller is able to report ANA Persistent Loss state (refer to section 8.20.3.4). If cleared to '0', then the controller does not report ANA Persistent Loss state. Bit 2 if set to '1', then the controller is able to report ANA Inaccessible state (refer to section 8.20.3.3). If cleared to '0', then the controller does not report ANA Inaccessible state. Bit 1 if set to '1', then the controller is able to report ANA Non-Optimized state (refer to section 8.20.3.2). If cleared to '0', then the controller does not report ANA Non-Optimized state. Bit 0 if set to '1', then the controller is able to report ANA Optimized state (refer to section 8.20.3.1). If the controller supports Asymmetric Namespace Access Reporting, then this bit is set to '1'.
347:344	O	**ANA Group Identifier Maximum (ANAGRPMAX):** This field indicates the maximum value of a valid ANA Group Identifier for any controller in the NVM subsystem. If the controller supports Asymmetric Namespace Access Reporting (refer to the CMIC field), then this field shall be set to a non-zero value. If the controller does not support Asymmetric Namespace Access Reporting, then this field shall be cleared to 0h.
351:348	O	**Number of ANA Group Identifiers (NANAGRPID):** This field indicates the number of ANA groups supported by the controller. If the controller supports Asymmetric Namespace Access Reporting (refer to the CMIC field), then this field shall be set to a non-zero value that is less than or equal to the ANAGRPMAX value. If the controller does not support Asymmetric Namespace Access Reporting, then this field shall be cleared to 0h.
355:352	O	**Persistent Event Log Size (PELS):** This field indicates the maximum reportable size for the Persistent Event Log (Refer to section 5.14.1.13) in 64 KiB units. If the Persistent Event Log is not supported, then this field is reserved.
511:356		Reserved

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
NVM Command Set Attributes		
512	M	**Submission Queue Entry Size (SQES):** This field defines the required and maximum Submission Queue entry size when using the NVM Command Set. Bits 7:4 define the maximum Submission Queue entry size when using the NVM Command Set. This value is greater than or equal to the required SQ entry size (i.e., bits 3:0 in this field). The value is in bytes and is reported as a power of two (2^*n*). The recommended value is 6, corresponding to a standard NVM Command Set SQ entry size of 64 bytes. Controllers that implement proprietary extensions may support a larger value. Bits 3:0 define the required (i.e., minimum) Submission Queue Entry size when using the NVM Command Set. This is the minimum entry size that may be used. The value is in bytes and is reported as a power of two (2^*n*). The required value shall be 6, corresponding to 64.
513	M	**Completion Queue Entry Size (CQES):** This field defines the required and maximum Completion Queue entry size when using the NVM Command Set. Bits 7:4 define the maximum Completion Queue entry size when using the NVM Command Set. This value is greater than or equal to the required CQ entry size (i.e., bits 3:0 in this field). The value is in bytes and is reported as a power of two (2^*n*). The recommended value is 4, corresponding to a standard NVM Command Set CQ entry size of 16 bytes. Controllers that implement proprietary extensions may support a larger value. Bits 3:0 define the required (i.e., minimum) Completion Queue entry size when using the NVM Command Set. This is the minimum entry size that may be used. The value is in bytes and is reported as a power of two (2^*n*). The required value shall be 4, corresponding to 16.
515:514	M	**Maximum Outstanding Commands (MAXCMD):** Indicates the maximum number of commands that the controller processes at one time for a particular queue (which may be larger than the size of the corresponding Submission Queue). The host may use this value to size Completion Queues and optimize the number of commands submitted at one time to a particular I/O Queue. This field is mandatory for NVMe over Fabrics implementations and optional for NVMe over PCIe implementations. If the field is not used, it shall be cleared to 0h.
519:516	M	**Number of Namespaces (NN):** This field indicates the maximum value of a valid NSID for the NVM subsystem. If the MNAN field is cleared to 0h, then this field also indicates the maximum number of namespaces supported by the NVM subsystem.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
521:520	M	**Optional NVM Command Support (ONCS):** This field indicates the optional NVM commands and features supported by the controller. Refer to section 6. Bits 15:8 are reserved. Bit 7 if set to '1', then the controller supports the Verify command. If cleared to '0', then the controller does not support the Verify command. Bit 6 if set to '1', then the controller supports the Timestamp feature. If cleared to '0', then the controller does not support the Timestamp feature. Refer to section 5.21.1.14. Bit 5 if set to '1', then the controller supports reservations. If cleared to '0', then the controller does not support reservations. If the controller supports reservations then the following commands associated with reservations shall be supported: Reservation Report, Reservation Register, Reservation Acquire, and Reservation Release. Refer to section 8.8 for additional requirements. Bit 4 if set to '1', then the controller supports the Save field set to a non-zero value in the Set Features command and the Select field set to a non-zero value in the Get Features command. If cleared to '0', then the controller does not support the Save field set to a non-zero value in the Set Features command and the Select field set to a non-zero value in the Get Features command. Bit 3 if set to '1', then the controller supports the Write Zeroes command. If cleared to '0', then the controller does not support the Write Zeroes command. Bit 2 if set to '1', then the controller supports the Dataset Management command. If cleared to '0', then the controller does not support the Dataset Management command. Bit 1 if set to '1', then the controller supports the Write Uncorrectable command. If cleared to '0', then the controller does not support the Write Uncorrectable command. Bit 0 if set to '1', then the controller supports the Compare command. If cleared to '0', then the controller does not support the Compare command.
523:522	M	**Fused Operation Support (FUSES):** This field indicates the fused operations that the controller supports. Refer to section 6.2. Bits 15:1 are reserved. Bit 0 if set to '1', then the controller supports the Compare and Write fused operation. If cleared to '0', then the controller does not support the Compare and Write fused operation. Compare shall be the first command in the sequence.
524	M	**Format NVM Attributes (FNA):** This field indicates attributes for the Format NVM command. Bits 7:3 are reserved. Bit 2 indicates whether cryptographic erase is supported as part of the secure erase functionality. If set to '1', then cryptographic erase is supported. If cleared to '0', then cryptographic erase is not supported. Bit 1 indicates whether secure erase functionality applies to all namespaces in an NVM subsystem or is specific to a particular namespace. If set to '1', then any secure erase performed as part of a format operation results in a secure erase of all namespaces in the NVM subsystem. If cleared to '0', then any secure erase performed as part of a format results in a secure erase of the particular namespace specified. Bit 0 indicates whether the format operation (excluding secure erase) applies to all namespaces in an NVM subsystem or is specific to a particular namespace. If set to '1', then all namespaces in an NVM subsystem shall be configured with the same attributes and a format (excluding secure erase) of any namespace results in a format of all namespaces in an NVM subsystem. If cleared to '0', then the controller supports format on a per namespace basis.

Figure 251: Identify – Identify Controller Data Structure

<table>
<tr><th>Bytes</th><th>O/M [1]</th><th>Description</th></tr>
<tr><td>525</td><td>M</td><td>
Volatile Write Cache (VWC): This field indicates attributes related to the presence of a volatile write cache in the controller.

Bits 7:3 are reserved.

Bits 2:1 indicate Flush command behavior (refer to section 6.8) if the NSID value is set to FFFFFFFFh as follows:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>Support for the NSID field set to FFFFFFFFh is not indicated. Only controllers compliant with versions 1.3 and earlier of the specification shall be allowed to return this value.</td></tr>
<tr><td>01b</td><td>Reserved.</td></tr>
<tr><td>10b</td><td>The Flush command does not support the NSID field set to FFFFFFFFh. The controller shall fail a Flush command with the NSID set to FFFFFFFFh with a status code of Invalid Namespace or Format.</td></tr>
<tr><td>11b</td><td>The Flush command supports the NSID field set to FFFFFFFFh.</td></tr>
</table>
Bit 0 if set to ‘1’ indicates that a volatile write cache is present. If cleared to ‘0’, a volatile write cache is not present.

If a volatile write cache is present, then the host controls whether the volatile write cache is enabled with a Set Features command specifying the Volatile Write Cache feature identifier (refer to section 5.21.1.6). The Flush command (refer to section 6.8) is used to request that the contents of a volatile write cache be made non-volatile.
</td></tr>
<tr><td>527:526</td><td>M</td><td>
Atomic Write Unit Normal (AWUN): This field indicates the size of the write operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format during normal operation. This field is specified in logical blocks and is a 0's based value.

If a specific namespace guarantees a larger size than is reported in this field, then this namespace specific size is reported in the NAWUN field in the Identify Namespace data structure. Refer to section 6.4.

If a write command is submitted with size less than or equal to the AWUN value, the host is guaranteed that the write command is atomic to the NVM with respect to other read or write commands. If a write command is submitted with size greater than the AWUN value, then there is no guarantee of command atomicity. AWUN does not have any applicability to write errors caused by power failure (refer to Atomic Write Unit Power Fail).

A value of FFFFh indicates all commands are atomic as this is the largest command size. It is recommended that implementations support a minimum of 128 KiB (appropriately scaled based on LBA size).
</td></tr>
</table>

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
529:528	M	**Atomic Write Unit Power Fail (AWUPF):** This field indicates the size of the write operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format during a power fail or error condition. If a specific namespace guarantees a larger size than is reported in this field, then this namespace specific size is reported in the NAWUPF field in the Identify Namespace data structure. Refer to section 6.4. This field is specified in logical blocks and is a 0's based value. The AWUPF value shall be less than or equal to the AWUN value. If a write command is submitted with size less than or equal to the AWUPF value, the host is guaranteed that the write is atomic to the NVM with respect to other read or write commands. If a write command is submitted that is greater than this size, there is no guarantee of command atomicity. If the write size is less than or equal to the AWUPF value and the write command fails, then subsequent read commands for the associated logical blocks shall return data from the previous successful write command. If a write command is submitted with size greater than the AWUPF value, then there is no guarantee of data returned on subsequent reads of the associated logical blocks.
530	M	**NVM Vendor Specific Command Configuration (NVSCC):** This field indicates the configuration settings for NVM Vendor Specific command handling. Refer to section 8.7. Bits 7:1 are reserved. Bit 0 if set to '1' indicates that all NVM Vendor Specific Commands use the format defined in Figure 107. If cleared to '0' indicates that the format of all NVM Vendor Specific Commands are vendor specific.
531	M	**Namespace Write Protection Capabilities (NWPC):** This field indicates the optional namespace write protection capabilities supported by the controller. Refer to section 8.19. Bits 7:3 are reserved. Bit 2 if set to '1', then the controller supports the Permanent Write Protect state. If cleared to '0', then the controller does not support the Permanent Write Protect state. If this bit is set to '1', then the controller shall support the Namespace Write Protection Authentication field (refer to section 8.10). Bit 1 if set to '1', then the controller supports the Write Protect Until Power Cycle state. If cleared to '0', then the controller does not support Write Protect Until Power Cycle state. If this bit is set to '1', then the controller shall support the Namespace Write Protection Authentication field (refer to section 8.10). Bit 0 if set to '1', then the controller shall support the No Write Protect and Write Protect namespace write protection states and may support the Write Protect Until Power Cycle state and Permanent Write Protect namespace write protection states (refer to section 8.19). If cleared to '0', then the controller does not support Namespace Write Protection and bits 2:1 shall be cleared to 00b.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
533:532	O	**Atomic Compare & Write Unit (ACWU):** This field indicates the size of the write operation guaranteed to be written atomically to the NVM across all namespaces with any supported namespace format for a Compare and Write fused operation. If a specific namespace guarantees a larger size than is reported in this field, then the Atomic Compare & Write Unit size for that namespace is reported in the NACWU field in the Identify Namespace data structure. Refer to section 6.4. This field shall be supported if the Compare and Write fused command is supported. This field is specified in logical blocks and is a 0's based value. If a Compare and Write is submitted that requests a transfer size larger than this value, then the controller may abort the command with a status code of Atomic Write Unit Exceeded. If Compare and Write is not a supported fused command, then this field shall be 0h.
535:534		Reserved

Figure 251: Identify – Identify Controller Data Structure

<table>
<tr><th>Bytes</th><th>O/M [1]</th><th>Description</th></tr>
<tr><td>539:536</td><td>O</td><td>SGL Support (SGLS): This field indicates if SGLs are supported for the NVM Command Set and the particular SGL types supported. Refer to section 4.4.
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:22</td><td>Reserved</td></tr>
<tr><td>21</td><td>If set to ‘1’, then the controller supports the Transport SGL Data Block descriptor. If cleared to ‘0’, then the controller does not support the Transport SGL Data Block descriptor.</td></tr>
<tr><td>20</td><td>If set to ‘1’, then the controller supports the Address field in SGL Data Block, SGL Segment, and SGL Last Segment descriptor types specifying an offset. If cleared to ‘0’, then the Address field specifying an offset is not supported.</td></tr>
<tr><td>19</td><td>If set to ‘1’, then use of a Metadata Pointer (MPTR) that contains an address of an SGL segment containing exactly one SGL Descriptor that is qword aligned is supported. If cleared to ‘0’, then use of a MPTR containing an SGL Descriptor is not supported.</td></tr>
<tr><td>18</td><td>If set to ‘1’, then the controller supports commands that contain a data or metadata SGL of a length larger than the amount of data to be transferred. If cleared to ‘0’, then the SGL length shall be equal to the amount of data to be transferred.</td></tr>
<tr><td>17</td><td>This field specifies metadata buffer alignment requirements when CDW0.PSDT is set to 01b (refer to Figure 105). If set to ‘1’, then use of a byte aligned contiguous physical buffer of metadata (the Metadata Pointer field in Figure 106) is supported. If cleared to ‘0’, then use of a byte aligned contiguous physical buffer of metadata is not supported.</td></tr>
<tr><td>16</td><td>If set to ‘1’, then the SGL Bit Bucket descriptor is supported. If cleared to ‘0’, then the SGL Bit Bucket descriptor is not supported.</td></tr>
<tr><td>15:03</td><td>Reserved</td></tr>
<tr><td>02</td><td>If set to ‘1’, then the controller supports the Keyed SGL Data Block descriptor. If cleared to ‘0’, then the controller does not support the Keyed SGL Data Block descriptor.</td></tr>
<tr><td>01:00</td><td>This field is used to determine the SGL support for the NVM Command Set. Valid values are shown in the table below.
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>SGLs are not supported.</td></tr>
<tr><td>01b</td><td>SGLs are supported. There is no alignment nor granularity requirement for Data Blocks.</td></tr>
<tr><td>10b</td><td>SGLs are supported. There is a dword alignment and granularity requirement for Data Blocks (refer to section 4.4).</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table></td></tr>
</table></td></tr>
<tr><td>543:540</td><td>O</td><td>Maximum Number of Allowed Namespaces (MNAN): This field indicates the maximum number of namespaces supported by the NVM subsystem. If this field is cleared to 0h, then the maximum number of namespaces supported by the NVM subsystem is less than or equal to the value in the NN field. If the controller supports Asymmetric Namespace Access Reporting, then this field shall be set to a non-zero value that is less than or equal to the NN value.</td></tr>
<tr><td>767:544</td><td></td><td>Reserved</td></tr>
</table>

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
1023:768	M	**NVM Subsystem NVMe Qualified Name (SUBNQN):** This field specifies the NVM Subsystem NVMe Qualified Name as a UTF-8 null-terminated string. Refer to section 7.9 for the definition of NVMe Qualified Name. Support for this field is mandatory if the controller supports revision 1.2.1 or later as indicated in the Version register (refer to section 3.1.2).
1791:1024		Reserved
2047:1792		Refer to the NVMe over Fabrics specification.
Power State Descriptors		
2079:2048	M	**Power State 0 Descriptor (PSD0):** This field indicates the characteristics of power state 0. The format of this field is defined in Figure 252.
2111:2080	O	**Power State 1 Descriptor (PSD1):** This field indicates the characteristics of power state 1. The format of this field is defined in Figure 252.
2143:2112	O	**Power State 2 Descriptor (PSD2):** This field indicates the characteristics of power state 2. The format of this field is defined in Figure 252.
2175:2144	O	**Power State 3 Descriptor (PSD3):** This field indicates the characteristics of power state 3. The format of this field is defined in Figure 252.
2207:2176	O	**Power State 4 Descriptor (PSD4):** This field indicates the characteristics of power state 4. The format of this field is defined in Figure 252.
2239:2208	O	**Power State 5 Descriptor (PSD5):** This field indicates the characteristics of power state 5. The format of this field is defined in Figure 252.
2271:2240	O	**Power State 6 Descriptor (PSD6):** This field indicates the characteristics of power state 6. The format of this field is defined in Figure 252.
2303:2272	O	**Power State 7 Descriptor (PSD7):** This field indicates the characteristics of power state 7. The format of this field is defined in Figure 252.
2335:2304	O	**Power State 8 Descriptor (PSD8):** This field indicates the characteristics of power state 8. The format of this field is defined in Figure 252.
2367:2336	O	**Power State 9 Descriptor (PSD9):** This field indicates the characteristics of power state 9. The format of this field is defined in Figure 252.
2399:2368	O	**Power State 10 Descriptor (PSD10):** This field indicates the characteristics of power state 10. The format of this field is defined in Figure 252.
2431:2400	O	**Power State 11 Descriptor (PSD11):** This field indicates the characteristics of power state 11. The format of this field is defined in Figure 252.
2463:2432	O	**Power State 12 Descriptor (PSD12):** This field indicates the characteristics of power state 12. The format of this field is defined in Figure 252.
2495:2464	O	**Power State 13 Descriptor (PSD13):** This field indicates the characteristics of power state 13. The format of this field is defined in Figure 252.
2527:2496	O	**Power State 14 Descriptor (PSD14):** This field indicates the characteristics of power state 14. The format of this field is defined in Figure 252.
2559:2528	O	**Power State 15 Descriptor (PSD15):** This field indicates the characteristics of power state 15. The format of this field is defined in Figure 252.
2591:2560	O	**Power State 16 Descriptor (PSD16):** This field indicates the characteristics of power state 16. The format of this field is defined in Figure 252.
2623:2592	O	**Power State 17 Descriptor (PSD17):** This field indicates the characteristics of power state 17. The format of this field is defined in Figure 252.
2655:2624	O	**Power State 18 Descriptor (PSD18):** This field indicates the characteristics of power state 18. The format of this field is defined in Figure 252.
2687:2656	O	**Power State 19 Descriptor (PSD19):** This field indicates the characteristics of power state 19. The format of this field is defined in Figure 252.
2719:2688	O	**Power State 20 Descriptor (PSD20):** This field indicates the characteristics of power state 20. The format of this field is defined in Figure 252.
2751:2720	O	**Power State 21 Descriptor (PSD21):** This field indicates the characteristics of power state 21. The format of this field is defined in Figure 252.
2783:2752	O	**Power State 22 Descriptor (PSD22):** This field indicates the characteristics of power state 22. The format of this field is defined in Figure 252.

Figure 251: Identify – Identify Controller Data Structure

Bytes	O/M [1]	Description
2815:2784	O	**Power State 23 Descriptor (PSD23):** This field indicates the characteristics of power state 23. The format of this field is defined in Figure 252.
2847:2816	O	**Power State 24 Descriptor (PSD24):** This field indicates the characteristics of power state 24. The format of this field is defined in Figure 252.
2879:2848	O	**Power State 25 Descriptor (PSD25):** This field indicates the characteristics of power state 25. The format of this field is defined in Figure 252.
2911:2880	O	**Power State 26 Descriptor (PSD26):** This field indicates the characteristics of power state 26. The format of this field is defined in Figure 252.
2943:2912	O	**Power State 27 Descriptor (PSD27):** This field indicates the characteristics of power state 27. The format of this field is defined in Figure 252.
2975:2944	O	**Power State 28 Descriptor (PSD28):** This field indicates the characteristics of power state 28. The format of this field is defined in Figure 252.
3007:2976	O	**Power State 29 Descriptor (PSD29):** This field indicates the characteristics of power state 29. The format of this field is defined in Figure 252.
3039:3008	O	**Power State 30 Descriptor (PSD30):** This field indicates the characteristics of power state 30. The format of this field is defined in Figure 252.
3071:3040	O	**Power State 31 Descriptor (PSD31):** This field indicates the characteristics of power state 31. The format of this field is defined in Figure 252.
Vendor Specific		
4095:3072	O	Vendor Specific.
NOTES: 1 O/M definition: O = Optional, M = Mandatory.		

Figure 252 defines the power state descriptor that describes the attributes of each power state. For more information on how the power state descriptor fields are used, refer to section 8.4 on power management.

Figure 252: Identify – Power State Descriptor Data Structure

Bits	Description
255:184	Reserved
183:182	**Active Power Scale (APS):** This field indicates the scale for the Active Power field. If an Active Power Workload is reported for a power state, then the Active Power Scale shall also be reported for that power state. **Value** / **Definition** 00b – Not reported for this power state 01b – 0.0001 W 10b – 0.01 W 11b – Reserved
181:179	Reserved
178:176	**Active Power Workload (APW):** This field indicates the workload used to calculate maximum power for this power state. Refer to section 8.4.3 for more details on each of the defined workloads. This field shall not be “No Workload” unless ACTP is 0h.
175:160	**Active Power (ACTP):** This field indicates the largest average power consumed by the NVM subsystem over a 10 second period in this power state with the workload indicated in the Active Power Workload field. The power in Watts is equal to the value in this field multiplied by the scale indicated in the Active Power Scale field. A value of 0h indicates Active Power is not reported.
159:152	Reserved

Figure 252: Identify – Power State Descriptor Data Structure

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>151:150</td><td>Idle Power Scale (IPS): This field indicates the scale for the Idle Power field.

<table><tr><th>Value</th><th>Definition</th></tr><tr><td>00b</td><td>Not reported for this power state</td></tr><tr><td>01b</td><td>0.0001 W</td></tr><tr><td>10b</td><td>0.01 W</td></tr><tr><td>11b</td><td>Reserved</td></tr></table></td></tr>
<tr><td>149:144</td><td>Reserved</td></tr>
<tr><td>143:128</td><td>Idle Power (IDLP): This field indicates the typical power consumed by the NVM subsystem over 30 seconds in this power state when idle (i.e., there are no pending commands, register accesses, background processes, sanitize operation, nor device self-test operations). The measurement starts after the NVM subsystem has been idle for 10 seconds. The power in Watts is equal to the value in this field multiplied by the scale indicated in the Idle Power Scale field. A value of 0h indicates Idle Power is not reported. Refer to section 8.4.

Note: This value may be used by hosts to manage power versus resume latency. Platform and form factor specifications may have additional power measurement and reporting requirements that are outside the scope of this specification.</td></tr>
<tr><td>127:125</td><td>Reserved</td></tr>
<tr><td>124:120</td><td>Relative Write Latency (RWL): This field indicates the relative write latency associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means lower write latency.</td></tr>
<tr><td>119:117</td><td>Reserved</td></tr>
<tr><td>116:112</td><td>Relative Write Throughput (RWT): This field indicates the relative write throughput associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means higher write throughput.</td></tr>
<tr><td>111:109</td><td>Reserved</td></tr>
<tr><td>108:104</td><td>Relative Read Latency (RRL): This field indicates the relative read latency associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means lower read latency.</td></tr>
<tr><td>103:101</td><td>Reserved</td></tr>
<tr><td>100:96</td><td>Relative Read Throughput (RRT): This field indicates the relative read throughput associated with this power state. The value in this field shall be less than the number of supported power states (e.g., if the controller supports 16 power states, then valid values are 0 through 15). A lower value means higher read throughput.</td></tr>
<tr><td>95:64</td><td>Exit Latency (EXLAT): This field indicates the maximum exit latency in microseconds associated with exiting this power state. A value of 0h indicates Exit Latency is not reported.</td></tr>
<tr><td>63:32</td><td>Entry Latency (ENLAT): This field indicates the maximum entry latency in microseconds associated with entering this power state. A value of 0h indicates Entry Latency is not reported.</td></tr>
<tr><td>31:26</td><td>Reserved</td></tr>
<tr><td>25</td><td>Non-Operational State (NOPS): This bit indicates whether the controller processes I/O commands in this power state. If this bit is cleared to ‘0’, then the controller processes I/O commands in this power state. If this bit is set to ‘1’, then the controller does not process I/O commands in this power state. Refer to section 8.4.1.</td></tr>
<tr><td>24</td><td>Max Power Scale (MXPS): This bit indicates the scale for the Maximum Power field. If this bit is cleared to ‘0’, then the scale of the Maximum Power field is in 0.01 Watts. If this bit is set to ‘1’, then the scale of the Maximum Power field is in 0.0001 Watts.</td></tr>
<tr><td>23:16</td><td>Reserved</td></tr>
<tr><td>15:00</td><td>Maximum Power (MP): This field indicates the sustained maximum power consumed by the NVM subsystem in this power state. The power in Watts is equal to the value in this field multiplied by the scale specified in the Max Power Scale bit. A value of 0h indicates Maximum Power is not reported. Refer to section 8.4.</td></tr>
</table>

Figure 252: Identify – Power State Descriptor Data Structure

Bits	Description
	Note: This value is intended to provide an approximate guideline for hosts to manage power versus performance. Platform and form factor specifications may have additional power measurement and reporting requirements that are outside the scope of this specification.

5.15.2.3 Active Namespace ID list (CNS 02h)

A list of 1,024 namespace IDs is returned to the host containing active NSIDs in increasing order that are greater than the value specified in the Namespace Identifier (NSID) field of the command. The controller should abort the command with status code Invalid Namespace or Format if the NSID field is set to FFFFFFFEh or FFFFFFFFh. The NSID field may be cleared to 0h to retrieve a Namespace List including the namespace starting with NSID of 1h. The data structure returned is a Namespace List (refer to section 4.10).

5.15.2.4 Namespace Identification Descriptor list (CNS 03h)

A list of Namespace Identification Descriptor structures (refer to Figure 253) is returned to the host for the namespace specified in the Namespace Identifier (NSID) field if it is an active NSID. If the NSID field does not specify an active NSID, then refer to section 6.1.5 for the status code to return.

The controller may return any number of variable length Namespace Identification Descriptor structures that fit into the 4,096 byte Identify payload. All remaining bytes after the namespace identification descriptor structures should be cleared to 0h, and the host shall interpret a Namespace Identifier Descriptor Length (NIDL) value of 0h as the end of the list. The host should ignore any Namespace Identification Descriptor with a Namespace Identifier Type not supported by the host.

A controller shall not return multiple descriptors with the same Namespace Identifier Type (NIDT). A controller shall return at least one descriptor identifying the namespace.

Figure 253: Identify – Namespace Identification Descriptor

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Namespace Identifier Type (NIDT): This field indicates the data type contained in the Namespace Identifier field and the length of that type as defined in the following table.
<table>
<tr><th>Value</th><th>Length (NIDL)</th><th>Definition</th></tr>
<tr><td>0h</td><td></td><td>Reserved</td></tr>
<tr><td>1h</td><td>8h</td><td>IEEE Extended Unique Identifier: The NID field contains a copy of the EUI64 field in the Identify Namespace data structure (refer to Figure 249). If the EUI64 field of the Identify Namespace data structure is not supported, (i.e., EUI64 field is cleared to 0h), the controller shall not report a Namespace Identification Descriptor with a value of type 1h.</td></tr>
<tr><td>2h</td><td>10h</td><td>Namespace Globally Unique Identifier: The NID field contains a copy of the NGUID field in the Identify Namespace data structure (refer to Figure 249). If the NGUID field of the Identify Namespace data structure is not supported (i.e., the NGUID field is cleared to 0h), the controller shall not report a Namespace Identification Descriptor with a value of type 2h.</td></tr>
<tr><td>3h</td><td>10h</td><td>Namespace UUID: The NID field contains a 128-bit Universally Unique Identifier (UUID) as specified in RFC 4122. Refer to section 7.10.6.

If the namespace does not support an IEEE Extended Unique Identifier (i.e., EUI64 field is cleared to 0h) and does not support a Namespace Globally Unique Identifier (i.e., the NGUID field is cleared to 0h), then the namespace shall report a Namespace Identification Descriptor with a value of type 3h.</td></tr>
<tr><td>4h to FFh</td><td></td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>01</td><td>Namespace Identifier Length (NIDL): This field contains the length in bytes of the Namespace Identifier (NID) field. The total length of the Namespace Identification Descriptor in bytes is the value in this field plus four. If this field is cleared to 0h it indicates the end of the Namespace Identifier Descriptor list.</td></tr>
<tr><td>02:03</td><td>Reserved</td></tr>
<tr><td>(NIDL + 3):04</td><td>Namespace Identifier (NID): This field contains a value that is globally unique and assigned to the namespace when the namespace is created. This field remains fixed throughout the life of the namespace and is preserved across namespace and controller operations (e.g., Controller Level Reset, namespace format, etc.). The type of the value is specified by the Namespace Identifier Type (NIDT) field, and the size is specified by the Namespace Identifier Length (NIDL) field.</td></tr>
</table>

5.15.2.5 NVM Set List (CNS 04h)

Figure 254 defines an NVM Set List. The data structure is an ordered list of NVM Set Attribute Entry data structures, sorted by NVM Set Identifier, starting with the first NVM Set Identifier supported by the NVM subsystem that is equal to or greater than the NVM Set Identifier indicated in CDW11.NVMSETID. The NVM Set List describes the attributes for each NVM Set in the list based on the NVM Set Attributes Entry in Figure 254.

Figure 254: NVM Set List

Bytes	Description
00	**Number of Identifiers:** This field indicates the number of NVM Set Attributes Entries in the list. There are up to 31 entries in the list. A value of 0h indicates that there are no entries in the list.
127:01	Reserved
255:128	**Entry 0:** This field contains the first NVM Set Attributes Entry in the list, if present.
383:256	**Entry 1:** This field contains the second NVM Set Attributes Entry in the list, if present.
…	**…**

Figure 254: NVM Set List

Bytes	Description
(N*128+255): (N*128+128)	**Entry N:** This field contains the N+1 NVM Set Attributes Entry in the list, if present.

Figure 255: NVM Set Attributes Entry

Bytes	Description
01:00	**NVM Set Identifier:** This field indicates the identifier of the NVM Set in the NVM subsystem that is described by this entry.
03:02	**Endurance Group Identifier:** This field indicates the Endurance Group for this NVM Set. Refer to section 8.17.
07:04	Reserved
11:08	**Random 4 KiB Read Typical:** This field indicates the typical time to complete a 4 KiB random read in 100 nanosecond units when the NVM Set is in a Predictable Latency Mode Deterministic Window and there is 1 outstanding command per NVM Set.
15:12	**Optimal Write Size:** This field indicates the size in bytes for optimal write performance. A value of 0h indicates that no Optimal Write Size is specified. This field should be set to 0h when namespaces within an NVM Set have different LBA formats that do not allow an Optimal Write Size to be specified.
31:16	**Total NVM Set Capacity:** This field indicates the total NVM capacity in this NVM Set. The value is in bytes.
47:32	**Unallocated NVM Set Capacity:** This field indicates the unallocated NVM capacity in this NVM Set. The value is in bytes.
127:48	Reserved

5.15.2.6 Allocated Namespace ID list (CNS 10h)

A list of up to 1,024 namespace IDs is returned to the host containing allocated NSIDs in increasing order that are greater than the value specified in the Namespace Identifier (NSID) field of the Identify command.

The controller should abort the command with status code Invalid Namespace or Format if the NSID field is set to FFFFFFFEh or FFFFFFFFh. The NSID field may be cleared to 0h to retrieve a Namespace List including the namespace starting with NSID of 1h. The data structure returned is a Namespace List (refer to section 4.10).

5.15.2.7 Identify Namespace data structure for an Allocated Namespace ID (CNS 11h)

The Identify Namespace data structure (refer to Figure 249) is returned to the host for the namespace specified in the Namespace Identifier (NSID) field if it is an allocated NSID. If the specified namespace is an unallocated NSID then the controller returns a zero filled data structure.

If the specified namespace is an invalid NSID then the controller shall abort the command with a status code of Invalid Namespace or Format. If the NSID field is set to FFFFFFFFh then the controller should abort the command with a status code of Invalid Namespace or Format.

5.15.2.8 Namespace Attached Controller list (CNS 12h)

A Controller List (refer to section 4.11) of up to 2,047 controller identifiers is returned containing a controller identifier greater than or equal to the value specified in the Controller Identifier (CDW10.CNTID) field. The list contains controller identifiers that are attached to the namespace specified in the Namespace Identifier

(NSID) field. If the NSID field is set to FFFFFFFFh, then the controller should abort the command with a status code of Invalid Field in Command.

5.15.2.9 Controller list (CNS 13h)

A Controller List (refer to section 4.11) of up to 2,047 controller identifiers is returned containing a controller identifier greater than or equal to the value specified in the Controller Identifier (CDW10.CNTID) field. The list contains controller identifiers in the NVM subsystem that may or may not be attached to namespace(s).

5.15.2.10 Primary Controller Capabilities data structure (CNS 14h)

The Primary Controller Capabilities Structure (refer to Figure 256) is returned to the host for the primary controller specified.

Figure 256: Identify – Primary Controller Capabilities Structure

Bytes	Description
01:00	**Controller Identifier (CNTLID):** This field indicates the Controller Identifier of the primary controller.
03:02	**Port Identifier (PORTID):** This field indicates the Port Identifier of the NVM subsystem port associated with the primary controller. The Port Identifier for a PCI Express Port is the same as the Port Number field in Link Capabilities Register in the PCI Express Capability structure (refer to section 2.5.6).
04	**Controller Resource Types (CRT):** This field indicates the controller resources types supported. If a primary controller supports a controller resource type, then all associated secondary controllers shall support that controller resource type. Bits 7:2 are reserved. Bit 1 if set to '1', then VI Resources are supported. Bit 1 if cleared to '0', then VI Resources are not supported. Refer to section 8.5.2. Bit 0 if set to '1', then VQ Resources are supported. Bit 0 if cleared to '0', then VQ Resources are not supported. Refer to section 8.5.1.
31:05	Reserved
35:32	**VQ Resources Flexible Total (VQFRT):** This field indicates the total number of VQ Flexible Resources for the primary and its secondary controllers.
39:36	**VQ Resources Flexible Assigned (VQRFA):** This field indicates the total number of VQ Flexible Resources Assigned to the associated secondary controllers.
41:40	**VQ Resources Flexible Allocated to Primary (VQRFAP):** This field indicates the total number of VQ Flexible Resources currently allocated to the primary controller. This value may change after a Controller Level Reset other than a Controller Reset (i.e., CC.EN transitions from '1' to '0') if a new value was set using the Virtualization Management command. The default value of this field is implementation specific.
43:42	**VQ Resources Private Total (VQPRT):** This field indicates the total number of VQ Private Resources for the primary controller.
45:44	**VQ Resources Flexible Secondary Maximum (VQFRSM):** This field indicates the maximum number of VQ Flexible Resources that may be assigned to a secondary controller.
47:46	**VQ Flexible Resource Preferred Granularity (VQGRAN):** This field indicates the preferred granularity of assigning and removing VQ Flexible Resources. Assigning and removing VQ Resources in this granularity minimizes any wasted internal implementation resources.
63:48	Reserved
67:64	**VI Resources Flexible Total (VIFRT):** This field indicates the total number of VI Flexible Resources for the primary and its secondary controllers.
71:68	**VI Resources Flexible Assigned (VIRFA):** This field indicates the total number of VI Flexible Resources Assigned to the associated secondary controllers.

Figure 256: Identify – Primary Controller Capabilities Structure

Bytes	Description
73:72	**VI Resources Flexible Allocated to Primary (VIRFAP):** This field indicates the total number of VI Flexible Resources currently allocated to the primary controller. This value may change after a Controller Level Reset other than a Controller Reset (i.e., CC.EN transitions from '1' to '0') if a new value was set using the Virtualization Management command. The default value of this field is implementation specific.
75:74	**VI Resources Private Total (VIPRT):** This field indicates the total number of VI Private Resources for the primary controller.
77:76	**VI Resources Flexible Secondary Maximum (VIFRSM):** This field indicates the maximum number of VI Flexible Resources that may be assigned to a secondary controller.
79:78	**VI Flexible Resource Preferred Granularity (VIGRAN):** This field indicates the preferred granularity of assigning and removing VI Flexible Resources. Assigning and removing VI Resources in this granularity minimizes any wasted internal implementation resources.
4095:80	Reserved

5.15.2.11 Secondary Controller list (CNS 15h)

A Secondary Controller List (refer to Figure 257) is returned to the host for up to 127 secondary controllers associated with the primary controller processing this command. The list contains entries for controller identifiers greater than or equal to the value specified in the Controller Identifier (CDW10.CNTID) field.

All secondary controllers are represented, including those that are in an Offline state due to SR-IOV configuration settings (e.g., VF Enable is cleared to '0' or NumVFs specifies a value that does not enable the associated secondary controller).

Figure 257: Secondary Controller List

Bytes	Description
00	**Number of Identifiers:** This field indicates the number of Secondary Controller Entries in the list. There are up to 127 entries in the list. A value of 0h indicates there are no entries in the list.
31:01	Reserved
63:32	**SC Entry 0:** This field contains the first Secondary Controller Entry in the list, if present.
95:64	**SC Entry 1:** This field contains the second Secondary Controller Entry in the list, if present.
…	…
(N*32+63): (N*32+32)	**SC Entry N:** This field contains the N+1 Secondary Controller Entry in the list, if present.

Figure 258: Secondary Controller Entry

Bytes	Description
01:00	**Secondary Controller Identifier (SCID):** This field indicates the Controller Identifier of the secondary controller described by this entry.
03:02	**Primary Controller Identifier (PCID): T**his field indicates the Controller Identifier of the associated primary controller.
04	**Secondary Controller State (SCS):** This field indicates the state of the secondary controller. Bits 7:1 are reserved. Bit 0 if set to '1', then the controller is in the Online state. Bit 0 if cleared to '0', then the controller is in the Offline state.
07:05	Reserved

Figure 258: Secondary Controller Entry

Bytes	Description
09:08	**Virtual Function Number (VFN):** If the secondary controller is an SR-IOV VF, this field indicates its VF Number, where VF Number > 0, and VF Number is no larger than the total number of VFs indicated by the TotalVFs register (refer to Single Root I/O Virtualization and Sharing Specification) in the PF's SR-IOV Extended Capability structure. If the secondary controller is not an SR-IOV VF, then this field is cleared to 0h.
11:10	**Number of VQ Flexible Resources Assigned (NVQ):** This field indicates the number of VQ Flexible Resources currently assigned to the indicated secondary controller.
13:12	**Number of VI Flexible Resources Assigned (NVI):** This field indicates the number of VI Flexible Resources currently assigned to the indicated secondary controller.
31:14	Reserved

5.15.2.12 Namespace Granularity List (CNS 16h)

If the controller supports reporting of Namespace Granularity (refer to section 8.12.1), then a Namespace Granularity List (refer to Figure 259) is returned to the host for up to sixteen namespace granularity descriptors (refer to Figure 260).

Figure 259: Namespace Granularity List

Bytes	Description
03:00	**Namespace Granularity Attributes:** This field indicates attributes of the Namespace Granularity List. Bits 31:1 are reserved. Bit 0 **(Granularity Descriptor Mapping):** If set to '1', then each valid namespace granularity descriptor applies to the LBA format having the same index and the Number of Descriptors field shall be equal to the Number of LBA Formats field in the Identify Namespace data structure (refer to Figure 249). If cleared to '0', then NG Descriptor 0 shall apply to all LBA formats and the Number of Descriptors field shall be cleared to 0h.
04	**Number of Descriptors:** This field indicates the number of valid namespace granularity descriptors in the list. This is a 0's based value. The namespace granularity descriptors with an index greater than the value in this field shall be cleared to 0h.
31:05	Reserved
47:32	**NG Descriptor 0:** This field contains the first namespace granularity descriptor in the list. This namespace granularity descriptor applies to LBA formats as indicated by the Granularity Descriptor Mapping bit.
63:48	**NG Descriptor 1:** This field contains the second namespace granularity descriptor in the list. This namespace granularity descriptor applies to LBA Format 1.
…	…
287:272	**NG Descriptor 15:** This field contains the sixteenth namespace granularity descriptor in the list. This namespace granularity descriptor applies to LBA Format 15.

The format of the namespace granularity descriptor is defined in Figure 260.

Figure 260: Namespace Granularity Descriptor

Bytes	Description
07:00	**Namespace Size Granularity:** Indicates the preferred granularity of allocation of namespace size when a namespace is created. The value is in bytes. A value of 0h indicates that the namespace size granularity is not reported.

Figure 260: Namespace Granularity Descriptor

Bytes	Description
15:08	**Namespace Capacity Granularity:** Indicates the preferred granularity of allocation of namespace capacity when a namespace is created. The value is in bytes. A value of 0h indicates that the namespace capacity granularity is not reported.

5.15.2.13 UUID List (CNS 17h)

The format of the UUID List is defined in Figure 261. Each UUID List entry is either 0h, the NVMe Invalid UUID, or a valid UUID. Valid UUIDs are those which are non-zero and are not the NVMe Invalid UUID (refer to section 8.24).

If bit 9 (UUID List) is set to '1' in the Controller Attributes (CTRATT) field in the Identify Controller data structure (refer to Figure 251), then:

- The UUID List shall contain at least one valid UUID (refer to section 8.24);
- The UUID 1 field shall contain a non-zero value; and
- A UUID field cleared to 0h indicates the end of the UUID List.

The list may be in any order.

Figure 261: UUID List

Bytes	Description
31:00	Reserved
63:32	**UUID 1:** This field contains the first UUID List Entry in the list.
95:64	**UUID 2:** This field contains the second UUID List Entry in the list, if present, otherwise cleared to 0h.
…	**…**
4063:4032	**UUID 126:** This field contains the last non-zero UUID List Entry in the list, if present, otherwise cleared to 0h.
4095:4064	**UUID 127:** This field shall be cleared to 0h.

The format of a UUID List Entry is defined in Figure 262.

Figure 262: UUID List Entry

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>UUID Lists Entry Header:
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>7:2</td><td>Reserved</td></tr>
<tr><td>1:0</td><td>Identifier Association: This field indicates whether the UUID is associated with a vendor.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>00b</td><td>No association reported.</td></tr>
<tr><td>01b</td><td>The UUID is associated with the vendor reported in the PCI Vendor ID field of the Identify Controller data structure (refer to Figure 251).</td></tr>
<tr><td>10b</td><td>The UUID is associated with the vendor reported in the PCI Subsystem Vendor ID field of the Identify Controller data structure.</td></tr>
<tr><td>11b</td><td>Reserved</td></tr>
</table></td></tr>
</table></td></tr>
<tr><td>15:01</td><td>Reserved</td></tr>
<tr><td>31:16</td><td>UUID: This field contains a 128-bit Universally Unique Identifier (UUID) as specified in RFC 4122. Refer to section 7.10.6.</td></tr>
</table>

5.15.3 Command Completion

Upon completion of the Identify command, the controller posts a completion queue entry to the Admin Completion Queue.

5.16 Keep Alive command

The Keep Alive command (refer to section 5.21.1.15) and associated functionality is used by the host to determine that the controller is operational and used by the controller to determine that the host is operational. The host and controller are operational when each is accessible and able to issue or process commands. The controller indicates the granularity of the Keep Alive Timer in the KAS field in the Identify Controller data structure (refer to Figure 251).

If a Keep Alive Timeout has been enabled on the Admin Queue, the Keep Alive Timer is restarted when:

- A Keep Alive command (refer to section 7.12.1) is processed; or
- At the end of the Keep Alive Timeout (refer to section 7.12.2) when TBKAS is set to '1' and an Admin command or an I/O command is processed during the Keep Alive Timeout Interval.

All command specific fields are reserved.

5.16.1 Command Completion

Upon completion of the Keep Alive command, the controller shall post a completion queue entry to the Admin Completion Queue indicating the status for the command.

5.17 NVMe-MI Receive command

Refer to the NVM Express Management Interface Specification for details on the NVMe-MI Receive command.

5.18 NVMe-MI Send command

Refer to the NVM Express Management Interface Specification for details on the NVMe-MI Send command.

5.19 Namespace Attachment command

The Namespace Attachment command is used to attach and detach controllers from a namespace. The attach and detach operations are persistent across all reset events. Namespace attach and detach operations are persistent across Virtualization Management commands that set a secondary controller offline.

If the Namespace Attachment command is supported, then the Namespace Management command (refer to section 5.20) shall also be supported.

The Namespace Attachment command uses the Data Pointer and Command Dword 10 fields. All other command specific fields are reserved.

The Select field determines the data structure used as part of the command. The data structure is 4,096 bytes in size. The data structure used for Controller Attach and Controller Detach is a Controller List (refer to section 4.11). The controllers that are to be attached or detached, respectively, are described in the data structure.

Figure 263: Namespace Attachment – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field. If using PRPs, this field shall not be a pointer to a PRP List as the data buffer may not cross more than one page boundary.

Figure 264: Namespace Attachment – Command Dword 10

Bits	Description
31:04	Reserved
03:00	**Select (SEL):** This field selects the type of attachment to perform. **Value** / **Description** 0h – Controller Attach 1h – Controller Detach 2h to Fh – Reserved

5.19.1 Command Completion

When the command is completed, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.

Command specific status values associated with the Namespace Attachment command are defined in Figure 265. For failures, the byte offset of the first failing entry is reported in the Command Specific Information field of the Error Information Log Entry. The controller does not process further entries in the Controller List after an error is encountered.

Figure 265: Namespace Attachment – Command Specific Status Values

Value	Description
18h	**Namespace Already Attached:** The controller is already attached to the namespace specified.
19h	**Namespace Is Private:** The controller is not attached to the namespace. The request to attach the controller could not be completed because the namespace is private and is already attached to one controller.
1Ah	**Namespace Not Attached:** The controller is not attached to the namespace. The request to detach the controller could not be completed.
1Ch	**Controller List Invalid:** The controller list provided is invalid or the controller list contains an administrative controller.
25h	**ANA Attach Failed:** The controller is not attached to the namespace as a result of an ANA condition (e.g., attaching the controller would result in an ANA Persistent Loss state (refer to section 8.20.3.4)).

5.20 Namespace Management command

The Namespace Management command is used to manage namespaces (refer to section 8.12), including create and delete operations.

Note: The controller continues to execute commands submitted to I/O Submission Queues while this operation is in progress.

If the Namespace Management command is supported, then the Namespace Attachment command (refer to section 5.19) shall also be supported.

Host software uses the Namespace Attachment command to attach or detach a namespace to or from a controller. The create operation does not attach the namespace to a controller. As a side effect of the delete operation, the namespace is detached from all controllers as the namespace is no longer present in the system. It is recommended that host software detach all controllers from a namespace prior to deleting the namespace. If the namespace is attached to another controller (i.e., a controller other than the controller processing the operation) and that controller has Namespace Attribute Notices enabled (refer to Figure 291), when a delete operation is requested, then as part of the delete operation a Namespace Attribute Notice is issued by that controller to indicate a namespace change.

The data structure used for the create operation is defined in Figure 269 and has the same format as the Identify Namespace data structure defined in Figure 249. After successful completion of a Namespace Management command with the create operation, the namespace is formatted with the specified attributes. The fields that host software may specify in the create operation are defined in Figure 266. Fields that are reserved are cleared to 0h by host software. There is no data structure transferred for the delete operation.

Figure 266: Namespace Management – Host Software Specified Fields

Bytes	Description	Host Specified
07:00	Namespace Size (NSZE)	Yes
15:08	Namespace Capacity (NCAP)	Yes
25:16	Reserved	
26	Formatted LBA Size (FLBAS)	Yes
28:27	Reserved	
29	End-to-end Data Protection Type Settings (DPS)	Yes
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	Yes
91:31	Reserved	
95:92	ANA Group Identifier (ANAGRPID) [1]	Yes
99:96	Reserved	
101:100	NVM Set Identifier (NVMSETID) [1]	Yes
383:102	Reserved	

Notes:
1. A value of 0h specifies that the controller determines the value to use (refer to section 8.12). If the associated feature is not supported, then the field is ignored by the controller.

The Namespace Management command uses the Data Pointer and Dword 10 fields. All other command specific fields are reserved.

The Namespace Identifier (NSID) field is used as follows for create and delete operations:

- **Create:** The NSID field is reserved for this operation; host software clears this field to a value of 0h. The controller shall select an available Namespace Identifier to use for the operation; or
- **Delete:** This field specifies the previously created namespace to delete in this operation. Specifying a value of FFFFFFFFh is used to delete all namespaces in the NVM subsystem. If the value of FFFFFFFFh is specified and there are zero valid namespaces, the command completes successfully.

Figure 267: Namespace Management – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field. If using PRPs, this field shall not be a pointer to a PRP List as the data buffer may not cross more than one page boundary.

Figure 268: Namespace Management – Command Dword 10

Bits	Description
31:04	Reserved
03:00	**Select (SEL):** This field selects the type of management operation to perform. **Value** / **Description** 0h / Create 1h / Delete 2h to Fh / Reserved

Figure 269: Namespace Management – Data Structure for Create

Bytes	Description
383:00	**Identify Namespace:** The fields set by host software are specified in Figure 266. Host software shall set reserved fields to 0h.
1023:384	Reserved
4095:1024	Vendor specific

5.20.1 Command Completion

When the command is completed, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.

Namespace Management command specific status values are defined in Figure 270.

Figure 270: Namespace Management – Command Specific Status Values

Value	Description
0Ah	**Invalid Format:** The LBA Format specified is not supported. This may be due to various conditions, including: 1) specifying an invalid LBA Format number; 2) enabling protection information when there is not sufficient metadata per LBA; 3) the specified format is not available in the current configuration; or 4) invalid security state (refer to TCG Storage Interface Interactions Specification).
15h	**Namespace Insufficient Capacity:** Creating the namespace requires more unallocated capacity than is currently available (refer to Unallocated NVM Capacity field in Figure 249). The Command Specific Information field of the Error Information Log specifies the total amount of unallocated NVM capacity required to create the namespace in bytes.
16h	**Namespace Identifier Unavailable:** The number of namespaces supported has been exceeded.
1Bh	**Thin Provisioning Not Supported:** Thin provisioning is not supported by the controller.
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
24h	**ANA Group Identifier Invalid:** The specified ANA Group Identifier (ANAGRPID) is not supported in the submitted command. This may be due to various conditions, including: a) specifying an ANAGRPID that does not exist; b) the controller does not allow an ANAGRPID to be specified (i.e., bit 7 in the ANACAP field is cleared to '0'); or c) the specified ANAGRPID is not supported by the controller processing the command (e.g., the specified value exceeds ANAGRPMAX (refer to Figure 251)). If the host specified a non-zero ANAGRPID, retrying the command with the ANAGRPID field cleared to 0h may succeed.

Dword 0 of the completion queue entry contains the Namespace Identifier created. The definition of Dword 0 of the completion queue entry is in Figure 271.

Figure 271: Namespace Management – Completion Queue Entry Dword 0

Bits	Description
31:00	**Namespace Identifier (NSID):** This field specifies the namespace identifier created in a Create operation. This field is reserved for all other operations.

5.21 Set Features command

The Set Features command specifies the attributes of the Feature indicated.

The Set Features command uses the Data Pointer, Command Dword 10, and Command Dword 14. The use of Command Dword 11, Command Dword 12, Command Dword 13, and and Command Dword 15 fields is Feature specific. If Command Dword 11, Command Dword 12, Command Dword 13, or Command Dword 15 fields are not used, then the Command Dwords are reserved.

Figure 272: Set Features – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field. If using PRPs, this field shall not be a pointer to a PRP List as the data buffer may not cross more than one page boundary. If no data structure is used as part of the specified feature, then this field is not used.

Figure 273: Set Features – Command Dword 10

Bits	Description
31	**Save (SV):** This bit specifies that the controller shall save the attribute so that the attribute persists through all power states and resets. The controller indicates in bit 4 of the Optional NVM Command Support field of the Identify Controller data structure in Figure 251 whether this bit is supported. If the Feature Identifier specified in the Set Features command is not saveable by the controller and the controller receives a Set Features command with the Save bit set to one, then the command shall be aborted with a status of Feature Identifier Not Saveable.
30:08	Reserved
07:00	**Feature Identifier (FID):** This field indicates the identifier of the Feature that attributes are being specified for.

If the controller supports selection of a UUID by the Set Features command (refer to Figure 275 and section 8.24) and the controller supports selection of a UUID for the specified vendor specific feature identifier (refer to Figure 275), then Command Dword 14 is used to specify a UUID Index value (refer to Figure 274). If the controller does not support selection of a UUID by the Set Features command or the controller does not support selection of a UUID for the specified vendor specific feature identifier, then Command Dword 14 does not specify a UUID Index value.

Figure 274: Set Features – Command Dword 14

Bits	Description
31:07	Reserved
06:00	**UUID Index:** Refer to Figure 502.

5.21.1 Feature Specific Information

Figure 275 defines the Features that may be configured with a Set Features command and retrieved with a Get Features command. Figure 276 defines Features that are specific to the NVM Command Set. Refer to section 7.1 for mandatory, optional, and prohibited features for the various controller types. Some Features utilize a memory buffer to configure or return attributes for a Feature, whereas others only utilize a dword in the command or completion queue entry. If a Feature is not persistent across power cycles and resets, then the current value of that Feature shall be set to the default value of that Feature as part of a Controller Level Reset. For more information on Features, including default value definitions, saved value definitions, and current value definitions, refer to section 7.8.

There may be commands in execution when a Feature is changed. The new settings may or may not apply to commands already submitted for execution when the Feature is changed. Any commands submitted to a Submission Queue after a Set Features command is successfully completed shall utilize the new settings for the associated Feature. To ensure that a Features values apply to all subsequent commands, the host should allow commands being processed to complete prior to issuing the Set Features command.

If the controller does not support a changeable value for a Feature (e.g., the Feature is not changeable), and a Set Features command for that Feature is processed, then if that command specifies a Feature value that:

- is not the same as the existing value for that Feature, then the controller shall abort that command with a status code of Feature Not Changeable; and
- is the same as the existing value for that Feature, then the controller may:
  - complete that command successfully; or
  - abort that command with a status code of Feature Not Changeable.

Figure 275: Set Features – Feature Identifiers

Feature Identifier	Current Setting Persists Across Power Cycle and Reset [2]	Uses Memory Buffer for Attributes	Feature Name
00h	Reserved		
01h	No	No	Arbitration
02h	No	No	Power Management
03h	Yes	Yes	LBA Range Type
04h	No	No	Temperature Threshold
05h	No	No	Error Recovery
06h	No	No	Volatile Write Cache
07h	No	No	Number of Queues
08h	No	No	Interrupt Coalescing
09h	No	No	Interrupt Vector Configuration
0Ah	No	No	Write Atomicity Normal
0Bh	No	No	Asynchronous Event Configuration
0Ch	No	Yes	Autonomous Power State Transition
0Dh	No [3]	No [4]	Host Memory Buffer
0Eh	No	Yes	Timestamp
0Fh	No	No	Keep Alive Timer
10h	Yes	No	Host Controlled Thermal Management
11h	No	No	Non-Operational Power State Config
12h	Yes	No	Read Recovery Level Config
13h	No	Yes	Predictable Latency Mode Config
14h	No	No	Predictable Latency Mode Window
15h	No	No	LBA Status Information Report Interval
16h	No	Yes	Host Behavior Support
17h	Yes	No	Sanitize Config
18h	No	No	Endurance Group Event Configuration
19h to 77h	Reserved		

Figure 275: Set Features – Feature Identifiers

Feature Identifier	Current Setting Persists Across Power Cycle and Reset [2]	Uses Memory Buffer for Attributes	Feature Name
78h to 7Fh	Refer to the NVMe Management Interface Specification for definition.		
80h to BFh			Command Set Specific (Reserved)
C0h to FFh			Vendor Specific[1, 5]

NOTES:
1. The behavior of a controller in response to an inactive namespace ID to a vendor specific Feature Identifier is vendor specific.
2. This column is only valid if the feature is not saveable (refer to section 7.8). If the feature is saveable, then this column is not used.
3. The controller does not save settings for the Host Memory Buffer feature across power states and reset events, however, host software may restore the previous values. Refer to section 8.9.
4. The feature does not use a memory buffer for Set Features commands and does use a memory buffer for Get Features commands. Refer to section 8.9.
5. Selection of a UUID may be supported. Refer to section 8.24.

Figure 276: Set Features, NVM Command Set Specific – Feature Identifiers

Feature Identifier	Current Setting Persists Across Power Cycle and Reset [1]	Uses Memory Buffer for Attributes	Feature Name
80h	Yes	No	Software Progress Marker
81h	No	Yes	Host Identifier
82h	No	No	Reservation Notification Mask
83h	Yes	No	Reservation Persistence
84h	No	No	Namespace Write Protection Config
85h to BFh			Reserved

NOTES:
1. This column is only valid if the feature is not saveable (refer to section 7.8). If the feature is saveable, then this column is not used.

5.21.1.1 Arbitration (Feature Identifier 01h)

This Feature controls command arbitration. Refer to section 4.13 for command arbitration details. The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 277 are returned in Dword 0 of the completion queue entry for that command.

Figure 277: Arbitration & Command Processing – Command Dword 11

Bits	Description
31:24	**High Priority Weight (HPW):** This field defines the number of commands that may be executed from the high priority service class in each arbitration round. This is a 0's based value.
23:16	**Medium Priority Weight (MPW):** This field defines the number of commands that may be executed from the medium priority service class in each arbitration round. This is a 0's based value.
15:08	**Low Priority Weight (LPW):** This field defines the number of commands that may be executed from the low priority service class in each arbitration round. This is a 0's based value.
07:03	Reserved

Figure 277: Arbitration & Command Processing – Command Dword 11

Bits	Description
02:00	**Arbitration Burst (AB):** Indicates the maximum number of commands that the controller may launch at one time from a particular Submission Queue. The value is expressed as a power of two (e.g., 000b indicates one, 011b indicates eight). A value of 111b indicates no limit.

5.21.1.2 Power Management (Feature Identifier 02h)

This Feature allows the host to configure the power state. The attributes are specified in Command Dword 11 (refer to Figure 278).

Upon successful completion of a Set Features command for this feature, the controller shall be in the Power State specified. For a transition to a non-operational power state, the device may exceed the power indicated for that non-operational power state as defined in section 8.4.1 (e.g., while completing this command). If enabled, autonomous power state transitions continue to occur from the new state.

If a Get Features command is submitted for this Feature, the attributes described in Figure 279 are returned in Dword 0 of the completion queue entry for that command.

Figure 278: Power Management – Command Dword 11

Bits	Description
31:08	Reserved
07:05	**Workload Hint (WH):** This field indicates the type of workload expected. This hint may be used by the NVM subsystem to optimize performance. Refer to section 8.4.3 for more details.
04:00	**Power State (PS):** This field indicates the new power state into which the controller is requested to transition. This power state shall be one supported by the controller as indicated in the Number of Power States Supported (NPSS) field in the Identify Controller data structure. If the power state specified is not supported, the controller shall abort the command and should return an error of Invalid Field in Command.

Figure 279: Power Management – Completion Queue Entry Dword 0

Bits	Description
31:08	Reserved
07:05	**Workload Hint (WH):** This field indicates the type of workload. Refer to section 8.4.3 for more details.
04:00	**Power State (PS):** This field indicates the current power state of the controller, or the power state into which the controller is transitioning.

5.21.1.3 LBA Range Type (Feature Identifier 03h), (Optional)

This feature indicates the type and attributes of LBA ranges that are part of the specified namespace. If multiple Set Features commands for this feature are processed, then only information from the most recent successful command is retained (i.e., subsequent commands replace information provided by previous commands).

A Set Features command with the Feature Identifier set to 03h and the NSID field set to FFFFFFFFh shall be aborted with a status of Invalid Field in Command.

The LBA Range Type feature uses Command Dword 11 and specifies the type and attribute information in the data structure indicated in Figure 282. The data structure is 4,096 bytes in size and shall be physically contiguous.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 281 are returned in Dword 0 of the completion queue entry and the LBA Range Type data structure specified in Figure 282 is returned in the data buffer for that command.

Figure 280: LBA Range Type – Command Dword 11

Bits	Description
31:06	Reserved
05:00	**Number of LBA Ranges (NUM):** This field specifies the number of LBA ranges specified in this command. This is a 0's based value. This field is used for the Set Features command only and is ignored for the Get Features command for this Feature.

Figure 281: LBA Range Type – Completion Queue Entry Dword 0

Bits	Description
31:06	Reserved
05:00	**Number of LBA Ranges (NUM):** This field indicates the number of valid LBA ranges returned in the data buffer for the command (refer to Figure 282). This is a 0's based value.

Each entry in the LBA Range Type data structure is defined in Figure 282. The LBA Range feature is a set of 64 byte entries; the number of entries is indicated as a command parameter, the maximum number of entries is 64. The controller is not required to perform validation checks on any of the fields in this data structure. The LBA ranges should not overlap and may be listed in any order (e.g., ordering by LBA is not required). If the controller checks for LBA range overlap and the controller detects an LBA range overlap, then the controller should return an error of Overlapping Range.

For a Get Features command, the controller may clear to zero all unused entries in the LBA Range Type data structure. For a Set Features command, the controller shall ignore all unused entries in the LBA Range Type data structure.

If the size of the namespace or the LBA format of the namespace changes, then the specified LBA ranges may not represent the expected locations in the NVM. After such a change, the host should ensure the intended LBAs are specified.

The default value for this feature should clear the Number of LBA Ranges field to 0h (i.e., one LBA Range is present) and initialize the LBA Range Type data structure to contain a single entry with the:

- Type field cleared to 0h;
- Attributes field set to 1h;
- Starting LBA field cleared to 0h;
- Number of Logical Blocks field set to indicate the number of LBAs in the namespace; and
- GUID field cleared to 0h, or set to a globally unique identifier.

Figure 282: LBA Range Type – Data Structure Entry

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>00</td><td>Type (Type): Specifies the Type of the LBA range. The Types are listed below.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0h</td><td>General Purpose</td></tr>
<tr><td>1h</td><td>Filesystem</td></tr>
<tr><td>2h</td><td>RAID</td></tr>
<tr><td>3h</td><td>Cache</td></tr>
<tr><td>4h</td><td>Page / swap file</td></tr>
<tr><td>5h to 7Fh</td><td>Reserved</td></tr>
<tr><td>80h to FFh</td><td>Vendor Specific</td></tr>
</table></td></tr>
</table>

Figure 282: LBA Range Type – Data Structure Entry

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>01</td><td>Attributes: Specifies attributes of the LBA range. Each bit defines an attribute.
<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>0</td><td>If set to ‘1’, the LBA range may be overwritten. If cleared to ‘0’, the area should not be overwritten.</td></tr>
<tr><td>1</td><td>If set to ‘1’, the LBA range should be hidden from the OS / EFI / BIOS. If cleared to ‘0’, the area should be visible to the OS / EFI / BIOS.</td></tr>
<tr><td>2 to 7</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>15:02</td><td>Reserved</td></tr>
<tr><td>23:16</td><td>Starting LBA (SLBA): This field specifies the 64-bit logical block address of the first logical block that is part of this LBA range.</td></tr>
<tr><td>31:24</td><td>Number of Logical Blocks (NLB): This field specifies the number of logical blocks that are part of this LBA range. This is a 0’s based value (e.g., the value 0h specifies one block).</td></tr>
<tr><td>47:32</td><td>Unique Identifier (GUID): This field contains a global unique identifier, for use by the host, that uniquely specifies the type of this LBA range. Well known Types may be defined and published on the NVM Express website.</td></tr>
<tr><td>63:48</td><td>Reserved</td></tr>
</table>

5.21.1.4 Temperature Threshold (Feature Identifier 04h)

A controller may report up to nine temperature values in the SMART / Health Information log (i.e., the Composite Temperature and Temperature Sensor 1 through Temperature Sensor 8; refer to Figure 198). Associated with each implemented temperature sensor is an over temperature threshold and an under temperature threshold. When a temperature is greater than or equal to its corresponding over temperature threshold or less than or equal to its corresponding under temperature threshold, then bit one of the Critical Warning field in the SMART / Health Information Log (refer to section 5.14.1.2) is set to one. This may trigger an asynchronous event.

The over temperature threshold feature shall be implemented for Composite Temperature. The under temperature threshold Feature shall be implemented for Composite Temperature if a non-zero Warning Composite Temperature Threshold (WCTEMP) field value is reported in the Identify Controller data structure (refer to Figure 251). The over temperature threshold and under temperature threshold features shall be implemented for all implemented temperature sensors (i.e., all Temperature Sensor fields that report a non-zero value).

The default value of the over temperature threshold feature for Composite Temperature is the value in the Warning Composite Temperature Threshold (WCTEMP) field in the Identify Controller data structure if WCTEMP is non-zero; otherwise, the default value is implementation specific. The default value of the under temperature threshold feature for Composite Temperature is implementation specific. The default value of the over temperature threshold for all implemented temperature sensors is FFFFh. The default value of the under temperature threshold for all implemented temperature sensors is 0h.

If a Get Features command is submitted for this feature, the temperature threshold selected by Command Dword 11 is returned in Dword 0 of the completion queue entry for that command.

Figure 283: Temperature Threshold – Command Dword 11

Bits	Description
31:22	Reserved

Figure 283: Temperature Threshold – Command Dword 11

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>21:20</td><td>Threshold Type Select (THSEL): This field selects the threshold type that is modified by a Set Features command and whose threshold value is returned by a Get Features command.

<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>00b</td><td>Over Temperature Threshold</td></tr>
<tr><td>01b</td><td>Under Temperature Threshold</td></tr>
<tr><td>10b to 11b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>19:16</td><td>Threshold Temperature Select (TMPSEL): This field selects the temperature whose threshold is modified by a Set Features command and whose threshold value is returned by a Get Features command.

<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0h</td><td>Composite Temperature</td></tr>
<tr><td>1h</td><td>Temperature Sensor 1</td></tr>
<tr><td>2h</td><td>Temperature Sensor 2</td></tr>
<tr><td>3h</td><td>Temperature Sensor 3</td></tr>
<tr><td>4h</td><td>Temperature Sensor 4</td></tr>
<tr><td>5h</td><td>Temperature Sensor 5</td></tr>
<tr><td>6h</td><td>Temperature Sensor 6</td></tr>
<tr><td>7h</td><td>Temperature Sensor 7</td></tr>
<tr><td>8h</td><td>Temperature Sensor 8</td></tr>
<tr><td>9h to Eh</td><td>Reserved</td></tr>
<tr><td>Fh</td><td>All implemented temperature sensors in a Set Features command. Reserved in a Get Features command.</td></tr>
</table></td></tr>
<tr><td>15:00</td><td>Temperature Threshold (TMPTH): Indicates the threshold value for the temperature sensor and threshold type specified.</td></tr>
</table>

5.21.1.5 Error Recovery (Feature Identifier 05h)

This Feature controls the error recovery attributes for the specified namespace. The attributes are indicated in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes described in Figure 284 are returned in Dword 0 of the completion queue entry for that command.

Figure 284: Error Recovery – Command Dword 11

Bits	Description
31:17	Reserved
16	**Deallocated or Unwritten Logical Block Error Enable (DULBE):** If set to '1', then the Deallocated or Unwritten Logical Block error is enabled for the namespace specified in the NSID field. If cleared to '0', then the Deallocated or Unwritten Logical Block error is disabled for the namespace specified in the NSID field. Host software shall only enable this error if the DAE bit in the NSFEAT field is set to ‘1’ in the Identify Namespace data structure. The default value for this bit shall be ‘0’. Refer to section 6.7.1.1.
15:00	**Time Limited Error Recovery (TLER):** Indicates a limited retry timeout value in 100 millisecond units. This limit applies to I/O commands that support the Limited Retry bit and that are sent to the namespace for which this Feature has been set. The timeout starts when error recovery actions have started while processing the command. A value of 0h indicates that there is no timeout. Note: This mechanism is primarily intended for use by host software that may have alternate means of recovering the data.

5.21.1.6 Volatile Write Cache (Feature Identifier 06h), (Optional)

This Feature controls the volatile write cache, if present, on the controller. If a volatile write cache is present (refer to the VWC field in Figure 251), then this feature shall be supported. The attributes are specified in Command Dword 11.

Note: If the controller is able to guarantee that data present in a write cache is written to non-volatile media on loss of power, then that write cache is considered non-volatile and this feature does not apply to that write cache.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 285 are returned in Dword 0 of the completion queue entry for that command.

If a volatile write cache is not present, then a Set Features command specifying the Volatile Write Cache feature identifier shall abort with Invalid Field in Command status, and a Get Features command specifying the Volatile Write Cache feature identifier should abort with Invalid Field in Command status.

Figure 285: Volatile Write Cache – Command Dword 11

Bits	Description
31:01	Reserved
00	**Volatile Write Cache Enable (WCE):** If set to '1', then the volatile write cache is enabled. If cleared to '0', then the volatile write cache is disabled.

5.21.1.7 Number of Queues (Feature Identifier 07h)

This Feature indicates the number of queues that the host requests for the controller processing the command. This feature shall only be issued during initialization prior to creation of any I/O Submission and/or Completion Queues. If a Set Features command is issued for this feature after creation of any I/O Submission and/or I/O Completion Queues, then the Set Features command shall abort with status code of Command Sequence Error. The controller shall not change the value allocated between resets. For a Set Features command, the attributes are specified in Command Dword 11 (refer to Figure 286). For a Get Features command, Dword 11 is ignored.

If a Set Features or Get Features command is submitted for this Feature, the attributes specified in Figure 287 are returned in Dword 0 of the completion queue entry for that command.

Figure 286: Number of Queues – Command Dword 11

Bits	Description
31:16	**Number of I/O Completion Queues Requested (NCQR):** Indicates the number of I/O Completion Queues requested by software. This number does not include the Admin Completion Queue. A minimum of one queue shall be requested, reflecting that the minimum support is for one I/O Completion Queue. This is a 0's based value. The maximum value that may be specified is 65,534 (i.e., 65,535 I/O Completion Queues). If the value specified is 65,535, the controller should return an error of Invalid Field in Command.
15:00	**Number of I/O Submission Queues Requested (NSQR):** Indicates the number of I/O Submission Queues requested by software. This number does not include the Admin Submission Queue. A minimum of one queue shall be requested, reflecting that the minimum support is for one I/O Submission Queue. This is a 0's based value. The maximum value that may be specified is 65,534 (i.e., 65,535 I/O Submission Queues). If the value specified is 65,535, the controller should return an error of Invalid Field in Command.

Note: The value allocated may be smaller or larger than the number of queues requested, often in virtualized implementations. The controller may not have as many queues to allocate as are requested. Alternatively, the controller may have an allocation unit of queues (e.g., power of two) and may supply more queues to host software to satisfy its allocation unit.

Figure 287: Number of Queues – Completion Queue Entry Dword 0

Bits	Description
31:16	**Number of I/O Completion Queues Allocated (NCQA):** Indicates the number of I/O Completion Queues allocated by the controller. A minimum of one queue shall be allocated, reflecting that the minimum support is for one I/O Completion Queue. The value may not match the number requested by host software. This is a 0's based value.
15:00	**Number of I/O Submission Queues Allocated (NSQA):** Indicates the number of I/O Submission Queues allocated by the controller. A minimum of one queue shall be allocated, reflecting that the minimum support is for one I/O Submission Queue. The value may not match the number requested by host software. This is a 0's based value.

5.21.1.8 Interrupt Coalescing (Feature Identifier 08h)

This Feature configures interrupt coalescing settings. The controller should signal an interrupt when either the Aggregation Time or the Aggregation Threshold conditions are met. If either the Aggregation Time or the Aggregation Threshold fields are cleared to 0h, then an interrupt may be generated (i.e., interrupt coalescing is implicitly disabled). This Feature applies only to the I/O Queues. It is recommended that interrupts for commands that complete in error are not coalesced. The settings are specified in Command Dword 11.

If the controller detects that interrupts are already being processed for this vector, then the controller may delay additional interrupts. Specifically, if the Completion Queue Head Doorbell register is being updated that is associated with a particular interrupt vector, then the controller has a positive indication that completion queue entries are already being processed. In this case, the aggregation time and/or the aggregation threshold may be reset/restarted upon the associated register write. This may result in interrupts being delayed indefinitely in certain workloads where the aggregation time or aggregation threshold is non-zero.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 288 are returned in Dword 0 of the completion queue entry for that command.

This Feature is valid when the controller is configured for Pin Based, MSI, Multiple MSI or MSI-X interrupts. There is no requirement for the controller to persist these settings if interrupt modes are changed. It is recommended that the host re-issue this Feature after changing interrupt modes.

Figure 288: Interrupt Coalescing – Command Dword 11

Bits	Description
31:16	Reserved
15:08	**Aggregation Time (TIME):** Specifies the recommended maximum time in 100 microsecond increments that a controller may delay an interrupt due to interrupt coalescing. A value of 0h corresponds to no delay. The controller may apply this time per interrupt vector or across all interrupt vectors. The reset value of this setting is 0h.
07:00	**Aggregation Threshold (THR):** Specifies the recommended minimum number of completion queue entries to aggregate per interrupt vector before signaling an interrupt to the host. This is a 0's based value. The reset value of this setting is 0h.

5.21.1.9 Interrupt Vector Configuration (Feature Identifier 09h)

This Feature configures settings specific to a particular interrupt vector. The settings are specified in Command Dword 11.

By default, coalescing settings are enabled for each interrupt vector. Interrupt coalescing is not supported for the Admin Completion Queue.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 289 are returned in Dword 0 of the completion queue entry for that command for the Interrupt Vector specified in Command Dword 11.

Prior to issuing a Set Features command that specifies this Feature, the host shall configure the specified Interrupt Vector with an I/O Completion Queue (refer to section 5.3). If the specified Interrupt Vector is invalid, or not associated with an existing I/O Completion Queue (refer to Figure 153), then the controller should return an error of Invalid Field in Command.

Figure 289: Interrupt Vector Configuration – Command Dword 11

Bits	Description
31:17	Reserved
16	**Coalescing Disable (CD):** If set to '1', then any interrupt coalescing settings shall not be applied for this interrupt vector. If cleared to '0', then interrupt coalescing settings apply for this interrupt vector.
15:00	**Interrupt Vector (IV):** This field specifies the interrupt vector for which the configuration settings are applied.

5.21.1.10 Write Atomicity Normal (Feature Identifier 0Ah)

This Feature controls the operation of the AWUN and NAWUN parameters (refer to section 6.4). The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 290 are returned in Dword 0 of the completion queue entry for that command.

Figure 290: Write Atomicity Normal – Command Dword 11

Bits	Description
31:01	Reserved
00	**Disable Normal (DN):** If set to '1', then the host specifies that AWUN and NAWUN are not required and that the controller shall only honor AWUPF and NAWUPF. If cleared to '0', then AWUN, NAWUN, AWUPF, and NAWUPF shall be honored by the controller.

5.21.1.11 Asynchronous Event Configuration (Feature Identifier 0Bh)

This Feature controls the events that trigger an asynchronous event notification to the host. This Feature may be used to disable reporting events in the case of a persistent condition (refer to section 5.2). If the condition for an event is true when the corresponding notice is enabled, then an event is sent to the host. The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 291 are returned in Dword 0 of the completion queue entry for that command.

Figure 291: Asynchronous Event Configuration – Command Dword 11

Bits	Description
31:28	Refer to the NVMe over Fabrics specification.
27:15	Reserved

Figure 291: Asynchronous Event Configuration – Command Dword 11

Bits	Description
14	**Endurance Group Event Aggregate Log Change Notices:** This bit determines whether an asynchronous event notification is sent to the host when an event entry for an Endurance Group (refer to section 8.17) has been added to the Endurance Group Event Aggregate log (refer to section 5.14.1.15). If this bit is set to '1', then the Endurance Group Event Aggregate Log Change event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the Endurance Group Event Aggregate Log Change event to the host. If Endurance Groups are not supported and this bit is set to '1', then the Set Features command shall be aborted with a status of Invalid Field in Command.
13	**LBA Status Information Notices:** This bit determines whether an asynchronous event notification is sent to the host for an LBA Status Information Alert event (refer to Figure 149). If this bit is set to '1', then the LBA Status Information Alert event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the LBA Status Information Alert event to the host.
12	**Predictable Latency Event Aggregate Log Change Notices:** This bit determines whether an asynchronous event notification is sent to the host when an event pending entry for an NVM Set (refer to section 5.14.1.11) has been added to the Predictable Latency Event Aggregate Log. If this bit is set to '1', then the Predictable Latency Event Aggregate Log Change event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the Predictable Latency Event Aggregate Log Change event to the host.
11	**Asymmetric Namespace Access Change Notices:** This bit determines whether an asynchronous event notification is sent to the host when an asymmetric namespace access change occurs (i.e., the contents of the Asymmetric Namespace Access log page (refer to section 5.14.1.12) change). If this bit is set to '1', then the Asymmetric Namespace Access Change Notices event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the Asymmetric Namespace Access Change Notices event to the host.
10	**Telemetry Log Notices:** This bit determines whether an asynchronous event notification is sent to the host when the Telemetry Controller-Initiated Data Available field transitions from 0h to 1h in the Telemetry Controller-Initiated log page. If this bit is set to '1', then the Telemetry Log Changed event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the Telemetry Log Changed event to the host.
09	**Firmware Activation Notices:** This bit determines whether an asynchronous event notification is sent to the host for a Firmware Activation Starting event (refer to Figure 149). If this bit is set to '1', then the Firmware Activation Starting event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the Firmware Activation Starting event to the host.
08	**Namespace Attribute Notices:** This bit determines whether an asynchronous event notification is sent to the host for a Namespace Attribute change (refer to Figure 149). If this bit is set to '1', then the Namespace Attribute Changed event is sent to the host when this condition occurs. If this bit is cleared to '0', then the controller shall not send the Namespace Attribute Changed event to the host.
07:00	**SMART / Health Critical Warnings:** This field determines whether an asynchronous event notification is sent to the host for the corresponding Critical Warning specified in the SMART / Health Information log (refer to Figure 198). If a bit is set to '1', then an asynchronous event notification is sent when the corresponding critical warning bit is set to '1' in the SMART / Health Information log. If a bit is cleared to '0', then an asynchronous event notification is not sent when the corresponding critical warning bit is set to '1' in the SMART / Health Information log.

5.21.1.12 Autonomous Power State Transition (Feature Identifier 0Ch), (Optional)

This feature configures the settings for autonomous power state transitions, refer to section 8.4.2.

The Autonomous Power State Transition uses Command Dword 11 and specifies the attribute information in the data structure indicated in Figure 292 and the Autonomous Power State Transition data structure consisting of 32 of the entries defined in Figure 293.

If a Get Features command is issued for this Feature, the attributes specified in Figure 292 are returned in Dword 0 of the completion queue entry and the Autonomous Power State Transition data structure, whose entry structure is defined in Figure 293, is returned in the data buffer for that command.

Figure 292: Autonomous Power State Transition – Command Dword 11

Bits	Description
31:01	Reserved
00	**Autonomous Power State Transition Enable (APSTE):** This bit specifies whether autonomous power state transition is enabled. If this bit is set to '1', then autonomous power state transitions are enabled. If this bit is cleared to '0', then autonomous power state transitions are disabled. This bit is cleared to '0' by default.

Each entry in the Autonomous Power State Transition data structure is defined in Figure 293. Each entry is 64 bits in size. There is an entry for each of the allowable 32 power states. For power states that are not supported, the unused Autonomous Power State Transition data structure entries shall be cleared to all zeroes. The entries begin with power state 0 and then increase sequentially (i.e., power state 0 is described in bytes 7:0, power state 1 is described in bytes 15:8, etc.). The data structure is 256 bytes in size and shall be physically contiguous.

Figure 293: Autonomous Power State Transition – Data Structure Entry

Bits	Description
63:32	Reserved
31:08	**Idle Time Prior to Transition (ITPT):** This field specifies the amount of idle time that occurs in this power state prior to transitioning to the Idle Transition Power State. The time is specified in milliseconds. A value of 0h disables the autonomous power state transition feature for this power state.
07:03	**Idle Transition Power State (ITPS):** This field specifies the power state to which the controller autonomously transitions, after there is a continuous period of idle time in the current power state that exceeds the time specified in the Idle Time Prior to Transition (ITPT) field. If the ITPT field is set to a non-zero value, then the state specified in this field shall be a non-operational state as described in Figure 252. This field should not specify a power state with higher reported idle power than the current power state. If the ITPT field is cleared to 0h, then this field should be cleared to 0h.
02:00	Reserved

The Autonomous Power State Transition feature may interact with the Non-Operational Power State Config feature (refer to section 5.21.1.17). Figure 294 shows these interactions.

Figure 294: Interactions between APSTE and NOPPME

APSTE[1]	NOPPME[2]	Non-operational power state entry	Background operations during non-operational power states
1	1	Entered by host request[3] or by ITPT idle timer[4]	Allowed
0	1	Entered by host request[3]	Allowed
1	0	Entered by host request[3] or by ITPT idle timer[4]	Not allowed

Figure 294: Interactions between APSTE and NOPPME

APSTE[1]	NOPPME[2]	Non-operational power state entry	Background operations during non-operational power states
0	0	Entered by host request[3]	Not allowed

NOTES:
1. Defined in Figure 292.
2. Defined in Figure 308.
3. Refer to section 5.21.1.1.
4. Refer to Figure 293.

5.21.1.13 Host Memory Buffer (Feature Identifier 0Dh), (Optional)

This Feature controls the Host Memory Buffer. The attributes are specified in Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15.

The Host Memory Buffer feature provides a mechanism for the host to allocate a portion of host memory for the exclusive use of the controller. After a successful completion of a Set Features command enabling the host memory buffer, the host shall not write to:

a) The Host Memory Descriptor List (refer to Figure 300); and
b) the associated host memory region (i.e., the memory regions described by the Host Memory Descriptor List),

until the host memory buffer has been disabled.

If the host memory buffer is enabled, then a Set Features command to enable the host memory buffer (i.e., the EHM bit (refer to Figure 295) set to ‘1’) shall abort with a status code of Command Sequence Error.

If the host memory buffer is not enabled, then a Set Features command to disable the host memory buffer (i.e., the EHM bit (refer to Figure 295) cleared to ‘0’) shall succeed without taking any action.

After a successful completion of a Set Features command that disables the host memory buffer, the controller shall not access any data in the host memory buffer until the host memory buffer has been enabled. The controller should retrieve any necessary data from the host memory buffer in use before posting the completion queue entry for the Set Features command that disables the host memory buffer. Posting of the completion queue entry for the Set Features command that disables the host memory buffer acknowledges that it is safe for the host software to modify the host memory buffer contents. Refer to section 8.9.

Figure 295: Host Memory Buffer – Command Dword 11

Bits	Description
31:02	Reserved
01	**Memory Return (MR):** If set to ‘1’, then the host is returning memory previously allocated to the controller for use as the host memory buffer (HMB). That memory may have been in use for the HMB prior to a reset or entering the Runtime D3 state (e.g., prior to the HMB being disabled). A returned host memory buffer shall have the exact same size, descriptor list address, descriptor list contents, and host memory buffer contents as last seen by the controller before the host memory buffer was disabled (i.e., a Set Features command with the EHM bit cleared to '0' was processed). If cleared to ‘0’, then the host is allocating host memory resources with undefined content.
00	**Enable Host Memory (EHM):** If set to ‘1’, then the host memory buffer shall be enabled and the controller may use the host memory buffer. If cleared to ‘0’, then the host memory buffer shall be disabled, and the controller shall not use the host memory buffer. If a Set Features command is processed with this bit cleared to ‘0’, then the controller shall ignore Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15.

Figure 296: Host Memory Buffer – Command Dword 12

Bits	Description
31:00	**Host Memory Buffer Size (HSIZE):** This field specifies the size of the host memory buffer allocated in memory page size (CC.MPS) units.

Figure 297: Host Memory Buffer– Command Dword 13

Bits	Description
31:00	**Host Memory Descriptor List Lower Address (HMDLLA):** This field specifies the lower 32 bits of the physical location of the Host Memory Descriptor List (refer to Figure 300) for the Host Memory Buffer. This address shall be 16 byte aligned, indicated by bits 3:0 being cleared to 0h. NOTE: The controller shall operate as if bits 3:0 are cleared to 0h. However, the controller is not required to check that bits 3:0 are cleared to 0h.

Figure 298: Host Memory Buffer – Command Dword 14

Bits	Description
31:00	**Host Memory Descriptor List Upper Address (HMDLUA):** This field specifies the upper 32 bits of the physical location of the Host Memory Descriptor List for the Host Memory Buffer.

The Host Memory Descriptor List Address (HMDLLA/HMDLUA) specifies the address of a physically contiguous data structure in host memory that describes the address and length pairs of the Host Memory Buffer. The number of address and length pairs is specified in the Host Memory Descriptor List Entry Count in Figure 299. The Host Memory Descriptor List is described in Figure 300.

Figure 299: Host Memory Buffer – Command Dword 15

Bits	Description
31:00	**Host Memory Descriptor List Entry Count (HMDLEC):** This field specifies the number of entries provided in the Host Memory Descriptor List.

Figure 300: Host Memory Buffer – Host Memory Descriptor List

Bytes	Description
15:0	Host Memory Buffer Descriptor (refer to Figure 301) Entry 0
31:16	Host Memory Buffer Descriptor Entry 1
47:32	Host Memory Buffer Descriptor Entry 2
63:48	Host Memory Buffer Descriptor Entry 3
…	
16*n+15:16*n	Host Memory Buffer Descriptor Entry n (where n = HMDLEC - 1 (refer to Figure 299))

Each Host Memory Buffer Descriptor Entry shall describe a host memory address in memory page size units and the number of contiguous memory page size units associated with the host address.

Figure 301: Host Memory Buffer – Host Memory Buffer Descriptor Entry

Bits	Description
127:96	Reserved
95:64	**Buffer Size (BSIZE):** Indicates the number of contiguous memory page size (CC.MPS) units for this descriptor.

Figure 301: Host Memory Buffer – Host Memory Buffer Descriptor Entry

Bits	Description
63:00	**Buffer Address (BADD):** Indicates the host memory address for this descriptor aligned to the memory page size (CC.MPS). The lower bits (*n*:0) of this field indicate the offset within the memory page is 0h (e.g., if the memory page size is 4 KiB, then bits 11:00 shall be 0h; if the memory page size is 8 KiB, then bits 12:00 shall be 0h).

If a Get Features command is issued for this Feature, the attributes specified in Figure 302 are returned in Dword 0 of the completion queue entry and the Host Memory Buffer Attributes data structure, whose structure is defined in Figure 303, is returned in the data buffer for that command.

Figure 302: Host Memory Buffer – Completion Queue Entry Dword 0

Bits	Description
31:01	Reserved
00	**Enable Host Memory (EHM):** If set to '1', then the host memory buffer is enabled and the controller may use the host memory buffer. If cleared to '0', then the host memory buffer is disabled, and the controller is not using the host memory buffer.

Figure 303: Host Memory Buffer – Attributes Data Structure

Bytes	Description
3:0	**Host Memory Buffer Size (HSIZE):** This field indicates the size of the host memory buffer allocated in memory page size units.
7:4	**Host Memory Descriptor List Address Lower (HMDLAL):** This field indicates the lower 32 bits of the physical location of the Host Memory Descriptor List (refer to Figure 300) for the host memory buffer. This address shall be 16 byte aligned. The lower 4 bits shall be cleared to '0'.
11:8	**Host Memory Descriptor List Address Upper (HMDLAU):** This field indicates the upper 32 bits of the physical location of the Host Memory Descriptor List (refer to Figure 300) for the host memory buffer.
15:12	**Host Memory Descriptor List Entry Count (HMDLEC):** This field indicates the number of valid Host Memory Descriptor Entries (refer to Figure 301) in the Host Memory Descriptor List (refer to Figure 300).
4095:16	Reserved

5.21.1.14 Timestamp (Feature Identifier 0Eh), (Optional)

The Timestamp feature enables the host to set a timestamp value in the controller. A controller indicates support for the Timestamp feature through the Optional NVM Command Support (ONCS) field in the Identify Controller data structure. The Timestamp value (refer to Figure 304) in a Set Features command sets a timestamp value in the controller. After the current value for this feature is set, the controller updates that value as time passes. A Get Features command that requests the current value reports the timestamp value in the controller at the time the Get Features command is processed (e.g., the value set with a Set Features command for the current value plus the elapsed time since being set).

Note: If the Timestamp feature is saveable (refer to Figure 188) and the host saves a value, then the timestamp value restored after a subsequent power on or reset event is the value that was saved (refer to section 7.8). As a result, the timestamp may appear to move backwards in time.

The accuracy of Timestamp values after initialization may be affected by vendor specific factors, such as whether the controller continuously counts after the timestamp is initialized, or whether the controller stops counting during certain intervals (e.g., non-operational power states). If the controller stops counting during such intervals, then the Synch bit in the Timestamp – Data Structure for Get Features (refer to Figure 305) shall be set to '1'.

If the controller maintains (i.e., continues to update) the timestamp value across any type of Controller Level Reset (e.g., across a Controller Reset), then the controller shall also preserve the Timestamp Origin field (refer to Figure 305) across that type of Controller Level Reset.

If the controller does not maintain the timestamp across the most recent Controller Level Reset, then the Timestamp field is cleared to 0h due to that Controller Level Reset.

Timestamp values should not be used for security applications. Other application use of the Timestamp is outside the scope of this specification.

If a Set Features command is issued for this Feature, the data structure specified in Figure 304 is transferred in the data buffer for that command, specifying the Timestamp value.

Figure 304: Timestamp – Data Structure for Set Features

Bytes	Description
05:00	**Timestamp:** Number of milliseconds that have elapsed since midnight, 01-Jan-1970, UTC.
07:06	Reserved

If a Get Features command is issued for this Feature, the data structure specified in Figure 305 is returned in the data buffer for that command.

Figure 305: Timestamp – Data Structure for Get Features

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>05:00</td><td>Timestamp:
If the Timestamp Origin field cleared to 000b, then this field is set to the time in milliseconds since the last Controller Level Reset.

If the Timestamp Origin field is set to 001b, then this field is set to the last Timestamp value set by the host, plus the time in milliseconds since the Timestamp was set. If the sum of the Timestamp value set by the host and the elapsed time exceeds 2^48, the value returned should be reduced modulo 2^48.

If the Synch bit is set to ‘1’, then the Timestamp value may be reduced by vendor specific time intervals not counted by the controller.</td></tr>
<tr><td>06</td><td>
<table>
<tr><th>Bits</th><th>Attribute</th><th>Definition</th></tr>
<tr><td>07:04</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>03:01</td><td>Timestamp Origin</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>The Timestamp field was initialized to 0h by a Controller Level Reset.</td></tr>
<tr><td>001b</td><td>The Timestamp field was initialized with a Timestamp value using a Set Features command.</td></tr>
<tr><td>010b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
<tr><td>00</td><td>Synch</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0</td><td>The controller counted time in milliseconds continuously since the Timestamp value was initialized.</td></tr>
<tr><td>1</td><td>The controller may have stopped counting during vendor specific intervals after the Timestamp value was initialized (e.g., non-operational power states).</td></tr>
</table>
</td></tr>
</table>
</td></tr>
<tr><td>07</td><td>Reserved</td></tr>
</table>

5.21.1.15 Keep Alive Timer (Feature Identifier 0Fh)

This Feature controls the Keep Alive Timer. Refer to section 7.12 for Keep Alive details. The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 306 are returned in Dword 0 of the completion queue entry for that command.

Figure 306: Keep Alive Timer – Command Dword 11

Bits	Description
31:00	**Keep Alive Timeout (KATO):** This field specifies the timeout value for the Keep Alive feature in milliseconds. The controller rounds up the value specified to the granularity indicated in the KAS field in the Identify Controller data structure. If cleared to 0h, then the Keep Alive Timer is disabled. The default value for this field is 0h for PCIe and fabrics that do not require use of the Keep Alive feature. For fabrics that require use of the Keep Alive feature, the default value for this field is 1D4C0h (i.e., 120,000 milliseconds or 2 minutes) rounded up to that granularity.

5.21.1.16 Host Controlled Thermal Management (Feature Identifier 10h), (Optional)

This feature configures the settings for the host controlled thermal management feature, refer to section 8.4.5. The host controlled thermal management feature uses Command Dword 11 with the attributes shown in Figure 307.

If a Get Features command is submitted for this feature, then the attributes shown in Figure 307 are returned in Dword 0 of the completion queue entry for that command.

This feature is not namespace specific.

Figure 307: HCTM – Command Dword 11

Bits	Description
31:16	**Thermal Management Temperature 1 (TMT1):** This field specifies the temperature, in Kelvins, when the controller begins to transition to lower power active power states or performs vendor specific thermal management actions while minimizing the impact on performance (e.g., light throttling) in order to attempt to reduce the Composite Temperature. A value cleared to 0h, specifies that this part of the feature shall be disabled. The range of values that are supported by the controller are indicated in the Minimum Thermal Management Temperature field and Maximum Thermal Management Temperature field in the Identify Controller data structure in Figure 251. If the host attempts to set this field to a value less than the value contained in the Minimum Thermal Management Temperature field or greater than the value contained in the Maximum Thermal Management Temperature field in the Identify Controller data structure in Figure 251, then the command shall abort with a status code of Invalid Field in Command. If the host attempts to set this field to a value greater than or equal to the value contained in the Thermal Management Temperature 2 field, if non-zero, then the command shall abort with a status code of Invalid Field in Command.

Figure 307: HCTM – Command Dword 11

Bits	Description
15:00	**Thermal Management Temperature 2 (TMT2):** This field specifies the temperature, in Kelvins, when the controller begins to transition to lower power active power states or perform vendor specific thermal management actions regardless of the impact on performance (e.g., heavy throttling) in order to attempt to reduce the Composite Temperature. A value cleared to 0h, specifies that this part of the feature shall be disabled. The range of values that are supported by the controller are indicated in the Minimum Thermal Management Temperature field and Maximum Thermal Management Temperature field in the Identify Controller data structure in Figure 251. If the host attempts to set this field to a value less than the value contained in the Minimum Thermal Management Temperature field or greater than the value contained in the Maximum Thermal Management Temperature field in the Identify Controller data structure in Figure 251, then the command shall abort with a status code of Invalid Field in Command. If the host attempts to set this field to a non-zero value less than or equal to the value contained in the Thermal Management Temperature 1 field, then the command shall abort with a status code of Invalid Field in Command.

5.21.1.17 Non-Operational Power State Config (Feature Identifier 11h), (Optional)

This Feature configures non-operational power state settings for the controller. The settings are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the values in Figure 308 are returned in Dword 0 of the completion queue entry for that command.

Figure 308: Non-Operational Power State Config – Command Dword 11

Bits	Description
31:01	Reserved
00	**Non-Operational Power State Permissive Mode Enable (NOPPME):** If NOPPME is set to ‘1’, then the controller may temporarily exceed the power limits of any non-operational power state, up to the limits of the last operational power state, to run controller initiated background operations in that state (i.e., Non-Operational Power State Permissive Mode is enabled). If NOPPME is cleared to ‘0’, then the controller shall not exceed the limits of any non-operational state while running controller initiated background operations in that state (i.e., Non-Operational Power State Permissive Mode is disabled). If Non-Operational Power State Permissive Mode is disabled, then: a) thermal management that requires power (e.g., cooling fans) may be disabled; and b) performance after resuming from the non-operational power state may be degraded until background activity that was not allowed while in that non-operational power state has completed. If the host attempts to set this bit to ‘1’ and the controller does not support Non-Operational Power State Permissive Mode as indicated in the Controller Attributes (CTRATT) field of the Identify Controller data structure, then the controller shall abort the command with a status of Invalid Field in Command.

The Non-Operational Power State Config feature may interact with the Autonomous Power State Transition feature (refer to section 5.21.1.12). Figure 294 shows these interactions.

5.21.1.18 Read Recovery Level Config (Feature Identifier 12h)

This Feature is used to configure the Read Recovery Level (refer to section 8.16). The attributes are specified in Command Dword 11 and Command Dword 12. Modifying the Read Recovery Level has no effect on the data contained in any associated namespace.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 310 are returned in Dword 0 of the completion queue entry for that command.

Figure 309: Read Recovery Level Config – Command Dword 11

Bits	Description
31:16	Reserved
15:00	**NVM Set Identifier (NVMSETID):** This field specifies the NVM Set to be modified. If NVM Sets are not supported, then this field is ignored and the command applies to all namespaces in the NVM subsystem.

Figure 310: Read Recovery Level Config – Command Dword 12

Bits	Description
31:04	Reserved
03:00	**Read Recovery Level (RRL):** This field sets the Read Recovery Level for the NVM Set specified.

5.21.1.19 Predictable Latency Mode Config (Feature Identifier 13h)

This Feature configures an NVM Set to use Predictable Latency Mode, including warning event thresholds. Predictable Latency Mode and events are disabled by default. The attributes are specified in Command Dword 11, Command Dword 12, and the Deterministic Threshold Configuration data structure.

The NVM Set has transitioned to Predictable Latency Mode when the controller completes a Set Features command successfully with the Predictable Latency Enable bit in Command Dword 12 set to '1'. A transition to the Predictable Latency Mode may be delayed (i.e., the Set Features command completion is delayed) if the NVM subsystem needs to perform background operations on the NVM in order to operate in Predictable Latency Mode. Upon successful completion of this command, the controller shall be in the Non-Deterministic Window.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 312 are returned in Dword 0 of the completion queue entry for that command and the Deterministic Threshold Configuration data structure is returned.

Figure 311: Predictable Latency Mode Config – Command Dword 11

Bits	Description
31:16	Reserved
15:00	**NVM Set Identifier:** This field specifies the NVM Set to be modified.

Figure 312: Predictable Latency Mode Config – Command Dword 12

Bits	Description
31:01	Reserved
00	**Predictable Latency Enable:** If this bit is set to '1', then Predictable Latency Mode (refer to section 8.18) is enabled for the NVM Set specified. If this bit is cleared to '0', then Predictable Latency Mode is disabled for the NVM Set specified.

Predictable Latency Events (refer to section 5.14.1.11) are configured as described in Figure 313.

Figure 313: Predictable Latency Mode – Deterministic Threshold Configuration Data Structure

Bytes	Description
01:00	**Enable Event:** This field specifies whether an entry shall be added to the Predictable Latency Event Aggregate Log Page for the associated event. If a bit is set to '1', then an entry shall be added if the specified event occurs. If a bit is cleared to '0', then an entry shall not be added if the specified event occurs. Bits: 00 – DTWIN Reads Warning 01 – DTWIN Writes Warning 02 – DTWIN Time Warning 03 to 13 – Reserved 14 – Autonomous transition from DTWIN to NDWIN due to typical or maximum value exceeded. 15 – Autonomous transition from DTWIN to NDWIN due to Deterministic Excursion.
31:02	Reserved
39:32	**DTWIN Reads Threshold:** If the value of DTWIN Reads Estimate falls below this value and the DTWIN Reads Warning is enabled, then the 'DTWIN Reads Warning' event is set in the Predictable Latency Per NVM Set Log Page for the affected NVM Set.
47:40	**DTWIN Writes Threshold:** If the value of DTWIN Writes Estimate falls below this value and the DTWIN Writes Warning is enabled, then the 'DTWIN Writes Warning' event is set in the Predictable Latency Per NVM Set Log Page for the affected NVM Set.
55:48	**DTWIN Time Threshold:** If the value of DTWIN Time Estimate falls below this value and the DTWIN Time Warning is enabled, then the 'DTWIN Time Warning' event is set in the Predictable Latency Per NVM Set Log Page for the affected NVM Set.
511:56	Reserved

5.21.1.20 Predictable Latency Mode Window (Feature Identifier 14h)

This Feature is used to set the window for the specified NVM Set and its associated namespaces if the NVM Set is configured in Predictable Latency Mode (refer to section 8.18). The attributes are specified in Command Dword 11 and Command Dword 12. If Predictable Latency Mode is not enabled, then the controller shall return an error of Invalid Field in Command.

The transition to the window selected is complete when the Set Features command completes successfully. A transition to the Deterministic Window may be delayed (i.e., the Set Features command completion is delayed) if the minimum time has not been spent in the Non-Deterministic Window.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 315 are returned in Dword 0 of the completion queue entry for that command. If Predictable Latency Mode is not enabled, then the controller shall return an error of Invalid Field in Command.

Figure 314: Predictable Latency Mode Window – Command Dword 11

Bits	Description
31:16	Reserved
15:00	**NVM Set Identifier:** This field specifies the NVM Set to be modified.

Figure 315: Predictable Latency Mode Window – Command Dword 12

Bits	Description
31:03	Reserved

Figure 315: Predictable Latency Mode Window – Command Dword 12

Bits	Description
02:00	**Window Select:** This field selects or indicates the window used by all namespaces in the NVM Set. **Value** / **Definition** 000b – Reserved 001b – Deterministic Window (DTWIN) 010b – Non-Deterministic Window (NDWIN) 011b to 111b – Reserved

5.21.1.21 LBA Status Information Attributes (Feature Identifier 15h)

The LBA Status Information Poll Interval (LSIPI) (refer to Figure 316) is the minimum interval that the host should wait between subsequent reads of the LBA Status Information log page with the Retain Asynchronous Event bit cleared to '0'. The LBA Status Information Poll Interval (LSIPI) is not changeable by the host.

The LBA Status Information Report Interval (LSIRI) (refer to Figure 316) is the minimum amount of time that a controller shall delay before sending an LBA Status Information Alert asynchronous event, if LBA Status Information Notices are enabled. The default value of the LSIRI is equal to LSIPI.

The host may read the LBA Status Information log page as part of LBA Status Information Alert asynchronous event processing or the host may use a polled method without enabling LBA Status Information Notices.

The controller reports the value of the LBA Status Information Attributes in Dword 0 of the completion queue entry when the host issues either a Set Features or Get Features command for this feature. The host configures the LBA Status Information Report Interval by issuing a Set Features command for this feature and specifying the value of the LBA Status Information Report Interval in Command Dword 11 (refer to Figure 316).

The host should not specify a value for the LBA Status Information Report Interval (LSIRI) which is less than the LBA Status Information Poll Interval (LSIPI) value reported by the controller. If the host specifies a value the controller does not support, the controller shall return the closest value supported by the controller in Dword 0 of the completion queue entry for the Set Features command. The accuracy of the interval measurement on the part of the controller is implementation specific.

The controller shall not send an LBA Status Information asynchronous event unless:

a) there are Tracked LBAs and:
    a) the LBA Status Information Report Interval condition has been exceeded and the LBA Status Generation Counter has been incremented since the last LBA Status Information Alert asynchronous event occurred; or
    b) an implementation specific aggregate threshold, if any exists, of Tracked LBAs has been exceeded;

    or

b) a component (e.g., die or channel) failure has occurred that may result in the controller aborting commands with Unrecovered Read Error status.

When the host issues a Get Log Page command for Log Identifier 0Eh with the Retain Asynchronous Event bit cleared to '0', the LBA Status Information Alert asynchronous event is cleared, if one was outstanding, and the LBA Status Information Report Interval is restarted by the controller.

LBAs added to the Tracked LBA List or component failures that generate potential LBAs for an Untracked LBA list may be coalesced into a single LBA Status Information Alert asynchronous event notification.

Figure 316: LBA Status Information Attributes – Command Dword 11

Bits	Description
31:16	**LBA Status Information Poll Interval (LSIPI):** The minimum amount of time in 100 millisecond increments that the host should wait between subsequent reads of the LBA Status Information log page with the Retain Asynchronous Event bit cleared to '0'.
15:00	**LBA Status Information Report Interval (LSIRI):** If LBA Status Information Notices are enabled, the value in this field is the minimum amount of time in 100 millisecond increments that a controller shall delay before sending an LBA Status Information Alert asynchronous event.

5.21.1.22 Host Behavior Support (Feature Identifier 16h)

This Feature enables use of controller functionality that is associated with and depends upon specific host behavior that may or may not be supported by all hosts. A controller does not use such functionality unless the host has indicated that the host supports the specific host behavior upon which the functionality depends. The host indicates that support to the controller by setting a field in this Feature. That host action enables controller use of the associated functionality with that host. A controller shall not use functionality with a host that has not indicated support for the associated specific host behavior upon which that controller functionality depends. The attributes in Figure 317 are transferred in the data buffer.

For example, the Command Interrupted status code is associated with and depends upon the specific host behavior that the host is expected to retry commands that are aborted with that status code. That command retry behavior may or may not be supported by all hosts (e.g., hosts based on versions of NVMe 1.3 and earlier are unlikely to retry commands aborted with the Command Interrupted status code as that status code was introduced after NVMe 1.3). A host that supports that command retry behavior indicates its support to the controller by setting a field to 1h in the Host Behavior Support Feature. Setting that field to 1h enables controller use of the Command Interrupted status code, with the result that this status code is used only with hosts that have indicated support for the associated command retry behavior.

This Feature is not saveable (refer to Figure 188). The default value of this Feature shall be all bytes cleared to 0h.

After a successful completion of a Set Features command for this Feature, the controller may use controller-to-host functionality that depends on specific host behavior as indicated by the attributes. If multiple Set Features commands for this Feature are processed by the controller, only information from the most recent successful command is retained (i.e., subsequent commands replace information provided by previous commands).

If a Get Features command is submitted for this Feature, the attributes specified in Figure 317 are returned in the data buffer for that command.

Figure 317: Host Behavior Support – Data Structure

Bytes	Description
00	**Advanced Command Retry Enable (ACRE):** If set to 1h, then the Command Interrupted status code is enabled (refer to Figure 128) and command retry delays are enabled. The controller may use the Command Interrupted status code and may indicate a command retry delay by setting the Command Retry Delay (CRD) field to a non-zero value in the Status field of a Completion Queue Entry, refer to Figure 126. A host that sets this field to 1h indicates host support for the command retry behaviors that are specified for both the Command Interrupted status code and non-zero values in the CRD field. If cleared to 0h, then both the Command Interrupted status code and command retry delays are disabled. The controller shall not use the Command Interrupted status code, and shall clear the CRD field to 0h in all CQEs. All values other than 0h and 1h are reserved.
511:01	Reserved

5.21.1.23 Sanitize Config (Feature Identifier 17h), (Optional)

This Feature controls behavior of the Sanitize command and sanitize operations. The scope of this Feature is the NVM subsystem.

The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 318 are returned in Dword 0 of the completion queue entry for that command.

If this Feature is not saveable (refer to Figure 188), then the default value of the NODRM attribute shall be cleared to '0' (i.e., No-Deallocate Error Response Mode).

If the capabilities of the Sanitize Config Feature Identifier are both changeable and saveable (refer to section 7.8), then the host is able to configure this Feature when initially provisioning a device.

Figure 318: Sanitize Config – Command Dword 11

Bits	Description
31:01	Reserved
00	**No-Deallocate Response Mode (NODRM):** If the No-Deallocate Inhibited bit in the Sanitize Capabilities field of the Identify Controller data structure (refer to Figure 251) is set to '1', then the NODRM bit defines the response of the controller to a Sanitize command processed with the No-Deallocate After Sanitize bit (refer to Figure 334) set to '1'. If the NODRM bit is set to '1' (i.e., No-Deallocate Warning Response Mode), then the controller shall process such Sanitize commands, and if the resulting sanitize operation is completed successfully, then bits 2:0 of the Sanitize Status field in the Sanitize Status log page shall be set to 100b (refer to Figure 242). If the NODRM bit is cleared to '0' (i.e., No-Deallocate Error Response Mode), then the controller shall abort such Sanitize commands with a status of Invalid Field in Command. If the No-Deallocate Inhibited bit in the Sanitize Capabilities field of the Identify Controller data structure (refer to Figure 251) is cleared to '0', then this bit has no effect.

5.21.1.24 Endurance Group Event Configuration (Feature Identifier 18h), (Optional)

This Feature controls the events that trigger adding an Endurance Group Event Aggregate Log Change Notices event to the Endurance Group Event Aggregate log. This Feature may be used to disable reporting events in the case of a persistent condition (refer to section 5.2). If the condition for an event is true when the corresponding notice is enabled, then an event is sent to the host. The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the Endurance Group Critical Warnings field in Command Dword 11 is not used and the attributes specified in Figure 319 are returned in Dword 0 of the completion queue entry for that command.

Figure 319: Asynchronous Event Configuration – Command Dword 11

Bits	Description
31:24	Reserved
23:16	**Endurance Group Critical Warnings:** This field determines whether an event entry for an Endurance Group (refer to section 8.17) is added to the Endurance Group Event Aggregate log page (refer to section 5.14.1.15) for the corresponding Critical Warning specified in the Endurance Group Information log (refer to Figure 208). If a bit is set to '1', then an entry is added when the corresponding critical warning bit is set to '1' in the Endurance Group Information log. If a bit is cleared to '0', then an entry is not added when the corresponding critical warning bit is set to '1' in the Endurance Group Information log page.

Figure 319: Asynchronous Event Configuration – Command Dword 11

Bits	Description
15:00	**Endurance Group Identifier (ENDGID):** This field indicates the Endurance Group for which asynchronous events are being configured. If this field is cleared to 0h, then the Endurance Group Critical Warnings field is not used.

If a bit is set to '1' in the Endurance Group Critical Warnings field which corresponds to a reserved bit in the Critical Warning field of the Endurance Group Information log page (refer to Figure 208), then the Set Features command shall be aborted with a status of Invalid Field in Command.

If the Endurance Group Identifier specifies an Endurance Group that does not exist, then the Set Features or Get Features command shall be aborted with a status of Invalid Field in Command.

5.21.1.25 Software Progress Marker (Feature Identifier 80h), (Optional) – NVM Command Set Specific

This Feature is a software progress marker. The software progress marker is persistent across power states. For additional details, refer to section 7.6.1.1. This information may be used to indicate to an OS software driver whether there have been issues with the OS successfully loading. The attributes are specified in Command Dword 11.

If a Get Features command is submitted for this Feature, the attributes specified in Figure 320 are returned in Dword 0 of the completion queue entry for that command.

Figure 320: Software Progress Marker – Command Dword 11

Bits	Description
31:08	Reserved
07:00	**Pre-boot Software Load Count (PBSLC):** Indicates the load count of pre-boot software. After successfully loading and initializing the controller, pre-boot software should set this field to one more than the previous value of the Pre-boot Software Load Count. If the previous value is 255, then the value should not be updated by pre-boot software (i.e., the value does not wrap to 0). OS driver software should set this field to 0h after the OS has successfully been initialized.

5.21.1.26 Host Identifier (Feature Identifier 81h), (Optional[1])

This feature allows the host to register a Host Identifier with the controller. The Host Identifier is used by the controller to determine whether other controllers in the NVM subsystem are associated with the same host. The Host Identifier may be used to designate host elements that access an NVM subsystem independently of each other or for reservations.

The Host Identifier is contained in the data structure indicated in Figure 322. The attributes are specified in Command Dword 11. If a Get Features command is issued for this Feature, the data structure specified in Figure 322 is returned in the data buffer for that command.

The requirements and use of the Host Identifier feature is dependent on whether the NVMe over PCIe implementation or NVMe over Fabrics implementation are supported. Refer to section 5.21.1.26.1 and section 5.21.1.26.2.

[1] Mandatory if reservations are supported by the controller as indicated in the ONCS field in the Identify Controller data structure.

Figure 321: Host Identifier – Command Dword 11

Bits	Description
31:01	Reserved
00	**Enable Extended Host Identifier (EXHID):** If set to '1', then the host is requesting the use of an extended 128-bit Host Identifier. If cleared to '0', then the host is requesting the use of a 64-bit Host Identifier. NVMe over Fabrics implementations shall use an extended 128-bit Host Identifier. If the controller does not support a 128-bit Host Identifier as indicated in the Controller Attributes field in the Identify Controller data structure and the host sets this bit to '1', then a status value of Invalid Field in Command shall be returned. If the controller does not support a 64-bit Host Identifier (e.g., the device is an NVMe over Fabrics device) and the host clears this bit to '0', then a status value of Invalid Field in Command shall be returned. If the NVM subsystem supports a 64-bit Host Identifier, supports a 128-bit Host Identifier and detects that another controller in the NVM subsystem is already using a non-zero Host Identifier of a different size than the size requested in this command, then a status of Host Identifier Inconsistent Format shall be returned.

Figure 322: Host Identifier – Data Structure Entry

Bytes	Description
15:00	**Host Identifier (HOSTID):** This field specifies a 64-bit or 128-bit identifier that uniquely identifies the host associated with the controller within the NVM subsystem. The host provides an 8 byte or 16 byte data structure depending on the value specified in the Enable Extended Host Identifier bit. The value of the Host Identifier used by a host, the method used to select this value, and the method used to ensure uniqueness are outside the scope of this specification. Controllers in an NVM subsystem that have the same Host Identifier are assumed to be associated with the same host and have the same reservation and registration rights. A Host Identifier value of 0h indicates that the host is not associated with any other controller in the NVM subsystem.

5.21.1.26.1NVMe over PCIe Implementations

The Host Identifier is an optional feature in NVMe over PCIe implementations. The controller may support a 64-bit Host Identifier and/or an extended 128-bit Host Identifier. It is recommended that implementations support the extended 128-bit Host Identifier as indicated in the Controller Attributes field in the Identify Controller data structure. The Host Identifier may be modified at any time using a Set Features command causing the controller to be logically remapped from the original host associated with the old Host Identifier to a new host associated with the new Host Identifier.

A Host Identifier value of 0h is a valid value that indicates that the host associated with the controller is not associated with any other controller in the NVM subsystem. Specifically, two controllers in an NVM subsystem that both have a Host Identifier of 0h indicates that the controllers are associated with different hosts. Using a Host Identifier value of 0h is a valid configuration for the reservations feature. However, reservations and registrations associated with a Host Identifier of 0h do not persist across a Controller Level Reset since a host that uses a Host Identifier of 0h is treated as a different host after a Controller Level Reset.

5.21.1.26.2NVMe over Fabrics Implementations

The Host Identifier is a mandatory feature in NVMe over Fabrics implementations. The Host Identifier shall be an extended 128-bit Host Identifier. The Host Identifier shall be set to a non-zero value in the Fabrics Connect command. The Host Identifier shall not be modified. A Set Features command specifying the Host

Identifier Feature shall be aborted with a status of Command Sequence Error. A Get Features command specifying the Host Identifier Feature shall return the value set in the Fabrics Connect command.

5.21.1.27 Reservation Notification Mask (Feature Identifier 82h), (Optional[2])

This Feature controls the masking of reservation notifications on a per namespace basis. A Reservation Notification log page is created whenever a reservation notification occurs on a namespace and the corresponding reservation notification type is not masked on that namespace by this Feature. If reservations are supported by the controller, then this Feature shall be supported. The attributes are specified in Command Dword 11.

A Set Features command that uses a namespace ID other than FFFFFFFFh modifies the reservation notification mask for the corresponding namespace only. A Set Features command that uses a namespace ID of FFFFFFFFh modifies the reservation notification mask of all namespaces that are attached to the controller and that support reservations. A Get Features command that uses a namespace ID other than FFFFFFFFh returns the reservation notification mask for the corresponding namespace. A Get Features command that uses a namespace ID of FFFFFFFFh should be aborted with status Invalid Field in Command. If a Set Features command or a Get Features command attempts to access the Reservation Notification Mask on a namespace that does not support reservations or is invalid, then that command is aborted with status Invalid Field in Command.

If a Get Features command successfully completes for this Feature, the attributes specified in Figure 323 are returned in Dword 0 of the completion queue entry for that command.

Figure 323: Reservation Notification Configuration – Command Dword 11

Bits	Description
31:04	Reserved
03	**Mask Reservation Preempted Notification (RESPRE):** If set to '1', then mask the reporting of reservation preempted notification by the controller. If cleared to '0', then the notification is not masked and a Reservation Notification log page is created whenever notification occurs.
02	**Mask Reservation Released Notification (RESREL):** If set to '1', then mask the reporting of reservation released notification by the controller. If cleared to '0', then the notification is not masked and a Reservation Notification log page is created whenever the notification occurs.
01	**Mask Registration Preempted Notification (REGPRE):** If set to '1', then mask the reporting of registration preempted notification by the controller. If cleared to '0', then the notification is not masked and a Reservation Notification log page is created whenever the notification occurs.
00	Reserved

5.21.1.28 Reservation Persistence (Feature Identifier 83h), (Optional[3])

Each namespace that supports reservations has a Persist Through Power Loss (PTPL) state that may be modified using either a Set Features command or a Reservation Register command (refer to section 6.11). The Reservation Persistence feature attributes are specified in Command Dword 11.

The PTPL state is contained in the Reservation Persistence Feature that is namespace specific. A Set Features command that uses the namespace ID FFFFFFFFh modifies the PTPL state associated with all namespaces that are attached to the controller and that support PTPL (i.e., support reservations). A Set Features command that uses a valid namespace ID other than FFFFFFFFh and corresponds to a namespace that supports reservations, modifies the PTPL state for that namespace. A Get Features

[2] Mandatory if reservations are supported by the namespace as indicated by a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure.
[3] Mandatory if reservations are supported by the namespace as indicated by a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure.

command that uses a namespace ID of FFFFFFFFh should be aborted with status Invalid Field in Command. A Get Features command that uses a valid namespace ID other than FFFFFFFFh and corresponds to a namespace that supports PTPL, returns the PTPL state for that namespace. If a Set Features command or a Get Features command using a namespace ID other than FFFFFFFFh attempts to access the PTPL state for a namespace that does not support this Feature Identifier, then the command is aborted with status Invalid Field in Command.

This Feature should not be saveable (refer to Figure 188). If this Feature is saveable, then the host should set the current value and the saved value to the same value.

If a Get Features command successfully completes for this Feature Identifier, the attributes specified in Figure 324 are returned in Dword 0 of the completion queue entry for that command

Figure 324: Reservation Persistence Configuration – Command Dword 11

Bits	Description
31:01	Reserved
00	**Persist Through Power Loss (PTPL):** If set to '1', then reservations and registrants persist across a power loss. If cleared to '0', then reservations are released and registrants are cleared on a power loss.

5.21.1.29 Namespace Write Protection Config (Feature Identifier 84h)

This Feature is used by the host to configure the namespace write protection state or to determine the write protection state of a namespace. Refer to section 8.19 for definition and behaviors of the namespace write protection states. The settings are specified in Command Dword 11.

This Feature is not saveable (refer to Figure 188). There is no default value for this Feature; the value of the Feature after a power cycle or a Controller Level Reset is determined by the write protection state of the namespace prior to the power cycle or Controller Level Reset, except for the Write Protect Until Power Cycle write protection state (refer to section 8.19).

If a Get Features command is submitted for this Feature, the attributes specified in Figure 325 are returned in Dword 0 of the completion queue entry for that command.

Figure 325: Write Protection – Command Dword 11

Bits	Description
31:03	Reserved
02:00	**Write Protection State:** This field specifies the write protection state of the specified namespace. **Value** / **Definition** 000b – No Write Protect 001b – Write Protect 010b – Write Protect Until Power Cycle 011b – Permanent Write Protect 100b to 111b – Reserved

If a Set Features command attempts to change the namespace write protection state of a namespace that is in the Write Protect Until Power Cycle state or the Permanent Write Protect state, then the command shall abort with a status code of Feature Not Changeable.

If a Set Features command attempts to change the namespace write protection state of a namespace to the Write Protect Until Power Cycle state and bit 0 of the of the Write Protection Authentication Control field is cleared to '0', then the command shall abort with a status code of Feature Not Changeable.

If a Set Features command changes the namespace to a write protected state, then the controller shall commit all volatile write cache data and metadata associated with the specified namespace to non-volatile media as part of transitioning to the write protected state.

5.21.2 Command Completion

Upon completion of the Set Features command, the controller posts a completion queue entry to the Admin Completion Queue. If a status of Successful Completion is returned, the completion queue entry shall not be posted until the controller has completed setting attributes associated with the Feature. Set Features command specific status values are defined in Figure 326.

Figure 326: Set Features – Command Specific Status Values

Value	Description
0Dh	**Feature Identifier Not Saveable:** The Feature Identifier specified does not support a saveable value.
0Eh	**Feature Not Changeable:** The Feature Identifier specified does not support a changeable value.
0Fh	**Feature Not Namespace Specific:** The Feature Identifier specified is not namespace specific. The Feature Identifier settings apply across all namespaces.
14h	**Overlapping Range:** This error is indicated if the LBA Range Type data structure has overlapping ranges.

5.22 Virtualization Management command

The Virtualization Management command is supported by primary controllers that support the Virtualization Enhancements capability. This command is used for several functions:

- Modifying Flexible Resource allocation for the primary controller;
- Assigning Flexible Resources for secondary controllers; and
- Setting the Online and Offline state for secondary controllers.

Refer to section 8.5 for more on the Virtualization Enhancements capability and the Virtualization Management command.

The Virtualization Management command uses the Command Dword 10 and Command Dword 11 fields. All other command specific fields are reserved.

If the action requested specifies a range of controller resources that:

a) does not exist;
b) is a Private Resource (e.g., VQ resources are requested when VQ resources are not supported, VI resources are requested when VI resources are not supported); or
c) is currently in use (e.g., the number of Controller Resources (NR) is greater than the number of remaining available flexible resources),

then an error of Invalid Resource Identifier is returned.

Figure 327: Virtualization Management – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:16</td><td>Controller Identifier (CNTLID): This field indicates the controller for which controller resources are to be modified.</td></tr>
<tr><td>15:11</td><td>Reserved</td></tr>
<tr><td>10:08</td><td>Resource Type (RT): This field indicates the type of controller resource to be modified.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>000b</td><td>VQ Resources</td></tr>
<tr><td>001b</td><td>VI Resources</td></tr>
<tr><td>010b to 111b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>07:04</td><td>Reserved</td></tr>
</table>

Figure 327: Virtualization Management – Command Dword 10

Bits	Description
03:00	**Action (ACT):** This field indicates the operation for the command to perform as described below. **Value** / **Description** 0h: Reserved 1h: **Primary Controller Flexible Allocation:** Set the number of Flexible Resources allocated to this primary controller following the next Controller Level Reset other than a Controller Reset (i.e., CC.EN transitions from '1' to '0'). If the Controller Identifier field does not correspond to this primary controller, then an error of Invalid Controller Identifier is returned. This value is persistent across power cycles and resets. 2h to 6h: Reserved 7h: **Secondary Controller Offline:** Place the secondary controller in the Offline state and remove all Flexible Resources. If the Controller Identifier field does not correspond to a secondary controller associated with this primary controller, then an error of Invalid Controller Identifier is returned. 8h: **Secondary Controller Assign:** Assign the number of controller resources specified in Number of Controller Resources to the secondary controller. If the Controller Identifier field does not correspond to a secondary controller associated with this primary controller, then an error of Invalid Controller Identifier is returned. If the secondary controller is not in the Offline state, then an error of Invalid Secondary Controller State is returned. 9h: **Secondary Controller Online:** Place the secondary controller in the Online state. If the Controller Identifier field does not correspond to a secondary controller associated with this primary controller, then an error of Invalid Controller Identifier is returned. If the secondary controller is not configured appropriately (refer to section 8.5) or the primary controller is not enabled, then an error of Invalid Secondary Controller State is returned. Ah to Fh: Reserved

Figure 328: Virtualization Management – Command Dword 11

Bits	Description
31:16	Reserved
15:00	**Number of Controller Resources (NR):** This field indicates a number of controller resources to allocate or assign.

5.22.1 Command Completion

Command specific status values associated with the Virtualization management command are defined in Figure 329.

Figure 329: Virtualization Management – Command Specific Status Values

Value	Description
1Fh	**Invalid Controller Identifier:** An invalid Controller Identifier was specified.
20h	**Invalid Secondary Controller State:** The action requested for the secondary controller is invalid based on the current state of the secondary controller and its primary controller.
21h	**Invalid Number of Controller Resources:** The specified number of Flexible Resources is invalid (e.g., the Number of Controller Resources (NR) is greater than VQ Resources Flexible Total (VQFRT) (refer to Figure 256), the Number of Controller Resources (NR) is greater than VQ Resources Flexible Secondary Maximum (VQFRSM) (refer to Figure 256)).
22h	**Invalid Resource Identifier:** At least one of the specified resource identifiers was invalid (e.g., the Number of Controller Resources (NR) is greater than the number of remaining available flexible resources).

Dword 0 of the completion queue entry contains information about the controller resources that were modified as part of the Primary Controller Flexible Allocation and Secondary Controller Assign actions. Dword 0 of the completion queue entry is defined in Figure 330.

Figure 330: Virtualization Management – Completion Queue Entry Dword 0

Bits	Description
31:16	Reserved
15:00	**Number of Controller Resources Modified (NRM):** This field indicates the number of controller resources that were allocated or assigned. The value may be smaller or larger than the number requested.

5.23 Format NVM command – NVM Command Set Specific

The Format NVM command is used to low level format the NVM media. This command is used by the host to change the LBA data size and/or metadata size. A low level format may destroy all data and metadata associated with all namespaces or only the specific namespace associated with the command (refer to the Format NVM Attributes field in the Identify Controller data structure). After the Format NVM command successfully completes, the controller shall not return any user data that was previously contained in an affected namespace.

As part of the Format NVM command, the host requests a format operation and may request a secure erase of the contents of the NVM (refer to the SES field in Figure 332). There are two types of secure erase. The User Data Erase erases all user content present in the NVM subsystem. The Cryptographic Erase erases all user content present in the NVM subsystem by deleting the encryption key with which the user data was previously encrypted.

The scope of the format operation and the scope of the format with secure erase depend on the attributes that the controller supports for the Format NVM command and the Namespace Identifier specified in the command as described in Figure 331. The type of secure erase, if applicable, is based on the setting of the Secure Erase Settings field in Command Dword 10 as defined in Figure 332.

Figure 331: Format NVM – Operation Scope

FNA Bit [1]	NSID	Format Operation
0	FFFFFFFFh	All namespaces attached to the controller. Other namespaces are not affected.
0	Any allocated value (refer to section 6.1.3)	Particular namespace specified. Other namespaces are not affected.
1	Any allocated value (refer to section 6.1.3) or FFFFFFFFh	All allocated namespaces in the NVM subsystem

NOTES:
1. For a Format NVM command with Secure Erase, this column refers to bit 1 in the FNA field in the Identify Controller data structure (refer to Figure 251) and bit 0 in the FNA field is ignored. For a Format NVM command without Secure Erase, this column refers to bit 0 in the FNA field, and bit 1 in the FNA field is ignored.

The Format NVM command may be aborted with a status code defined in this specification under circumstances defined by a security specification (e.g., invalid security state as specified in TCG Storage Interface Interactions Specification). If there are I/O commands being processed for a namespace, then a Format NVM command that is submitted affecting that namespace may be aborted; if aborted, then a status code of Command Sequence Error should be returned. If a Format NVM command is in progress, then an

I/O command that is submitted for any namespace affected by that Format NVM command may be aborted; if aborted, then a status code of Format in Progress should be returned.

For a Format NVM command with the NSID field set to FFFFFFFFh that specifies secure erase:

a) if bit 1 is set to '1' in the FNA field (refer to Figure 251) and there are no namespaces in the NVM subsystem, then that Format NVM command shall complete without error; and
b) if bit 1 is cleared to '0' in the FNA field and there are no attached namespaces, then that Format NVM command shall complete without error.

For a Format NVM command with an NSID field set to FFFFFFFFh that does not specify a secure erase:

a) if bit 0 is set to '1' in the FNA field and there are no namespaces in the NVM subsystem, then that Format NVM command shall complete without error; and
b) if bit 0 is cleared to '0' in the FNA field and there are no attached namespaces, then that Format NVM command shall complete without error.

After successful completion of a Format NVM command, the settings specified in the Format NVM command (e.g., PI, MSET, LBAF) are reported as part of the Identify Namespace data structure. If the Format NVM command results in a change of the logical block size for the namespace, then the resulting namespace size (i.e., NSZE) (refer to Figure 249) and the namespace capacity (i.e., NCAP) (refer to Figure 249) may differ from the values indicated prior to the processing of the Format NVM command.

The Format NVM command uses the Command Dword 10 field. All other command specific fields are reserved.

Figure 332: Format NVM – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:12</td><td>Reserved</td></tr>
<tr><td>11:09</td><td>Secure Erase Settings (SES): This field specifies whether a secure erase should be performed as part of the format and the type of the secure erase operation. The erase applies to all user data, regardless of location (e.g., within an exposed LBA, within a cache, within deallocated logical blocks, etc.).

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>No secure erase operation requested</td></tr>
<tr><td>001b</td><td>User Data Erase: All user data shall be erased, contents of the user data after the erase is indeterminate (e.g., the user data may be zero filled, one filled, etc.). If a User Data Erase is requested and all affected user data is encrypted, then the controller is allowed to use a cryptographic erase to perform the requested User Data Erase.</td></tr>
<tr><td>010b</td><td>Cryptographic Erase: All user data shall be erased cryptographically. This is accomplished by deleting the encryption key.</td></tr>
<tr><td>011b to 111b</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>08</td><td>Protection Information Location (PIL): If set to '1' and protection information is enabled, then protection information is transferred as the first eight bytes of metadata. If cleared to '0' and protection information is enabled, then protection information is transferred as the last eight bytes of metadata. This setting is reported in the End-to-end Data Protection Type Settings (DPS) field of the Identify Namespace data structure and is constrained by the End-to-end Data Protection Capabilities (DPC) field of the Identify Namespace data structure.</td></tr>
</table>

Figure 332: Format NVM – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>07:05</td><td>Protection Information (PI): This field specifies whether end-to-end data protection is enabled and the type of protection information. The values for this field have the following meanings:

<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>000b</td><td>Protection information is not enabled</td></tr>
<tr><td>001b</td><td>Protection information is enabled, Type 1</td></tr>
<tr><td>010b</td><td>Protection information is enabled, Type 2</td></tr>
<tr><td>011b</td><td>Protection information is enabled, Type 3</td></tr>
<tr><td>100b to 111b</td><td>Reserved</td></tr>
</table>

When end-to-end data protected is enabled, the host shall specify the appropriate protection information in the Read, Verify, Write, or Compare commands.</td></tr>
<tr><td>04</td><td>Metadata Settings (MSET): This bit is set to ‘1’ if the metadata is transferred as part of an extended data LBA. This bit is cleared to ‘0’ if the metadata is transferred as part of a separate buffer. The metadata may include protection information, based on the Protection Information (PI) field. If the Metadata Size for the LBA Format selected is 0h, then this bit is not applicable.</td></tr>
<tr><td>03:00</td><td>LBA Format (LBAF): This field specifies the LBA format to apply to the NVM media. This corresponds to the LBA formats indicated in the Identify command, refer to Figure 249 and Figure 250. Only supported LBA formats shall be selected.</td></tr>
</table>

5.23.1 Command Completion

A completion queue entry is posted to the Admin Completion Queue when the NVM media format is complete. Format NVM command specific status values are defined in Figure 333.

Figure 333: Format NVM – Command Specific Status Values

Value	Description
0Ah	**Invalid Format:** The format specified is invalid. This may be due to various conditions, including: a) specifying an invalid LBA Format number; b) enabling protection information when there is not sufficient metadata per LBA; c) the specified format is not available in the current configuration; or d) invalid security state (refer to TCG Storage Interface Interactions Specification), etc.
0Ch	**Command Sequence Error:** The command was aborted due to a protocol violation in a multi-command sequence.
15h	**Operation Denied:** The command was denied due to lack of access rights. Refer to the appropriate security specification.
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
86h	**Access Denied:** Access to the namespace and/or LBA range is denied due to lack of access rights. Refer to the appropriate security specification (e.g., TCG Storage Interface Interactions specification).

5.24 Sanitize command – NVM Command Set Specific

The Sanitize command is used to start a sanitize operation or to recover from a previously failed sanitize operation. The sanitize operation types that may be supported are Block Erase, Crypto Erase, and Overwrite. All sanitize operations are processed in the background (i.e., completion of the Sanitize command does not indicate completion of the sanitize operation). Refer to section 8.15 for details on the sanitize operation.

When a sanitize operation starts on any controller, all controllers in the NVM subsystem:

- Shall clear any outstanding Sanitize Operation Completed asynchronous event or Sanitize Operation Completed With Unexpected Deallocation asynchronous event;
- Shall update the Sanitize Status log (refer to section 5.14.1.16.2);
- Shall abort any command (submitted or in progress) not allowed during a sanitize operation with a status of Sanitize In Progress (refer to section 8.15.1);
- Shall abort device self-test operations in progress;
- Suspends autonomous power state management activities as described in section 8.4.2; and
- Shall release stream identifiers for any open streams.

If a sanitize operation is not in progress and the most recent sanitize operation did not fail, then a Sanitize command with a Sanitize Action set to 001b (i.e., Exit Failure Mode) shall complete with a status of Successful Completion and perform no other action.

While a sanitize operation is in progress, all controllers in the NVM subsystem shall abort any command not allowed during a sanitize operation with a status of Sanitize In Progress (refer to section 8.15.1) and the Persistent Memory Region shall behave as described in section 8.15.1.

After a sanitize operation fails, all controllers in the NVM subsystem shall abort any command not allowed during a sanitize operation with a status of Sanitize Failed (refer to section 8.15.1) and the Persistent Memory Region shall behave as described in section 8.15.1 until a subsequent sanitize operation is started or successful recovery from the failed sanitize operation occurs.

If the most recent failed sanitize operation was started in unrestricted completion mode (i.e., the AUSE bit was set to ‘1’ in the Sanitize command), failure recovery requires the host to issue a subsequent Sanitize command in restricted or unrestricted completion mode or to issue a subsequent Sanitize command with the Exit Failure Mode action.

If the most recent failed sanitize operation was started in restricted completion mode (i.e., the AUSE bit was cleared to ‘0’ in the Sanitize command), failure recovery requires the host to issue a subsequent Sanitize command in restricted completion mode. In the case of a sanitize operation failure in restricted completion mode, before starting another sanitize operation:

- any subsequent Sanitize command issued with the Exit Failure Mode action shall be aborted with a status of Sanitize Failed; and
- any Sanitize command issued in unrestricted completion mode shall be aborted with a status of Sanitize Failed.

The Sanitize Capabilities field in the Identify Controller data structure indicates:

a) the sanitize operation types supported;
b) whether setting No-Deallocate After Sanitize bit (i.e., Sanitize command Dword 10 bit 9) causes media to be modified after a successful sanitize operation completes; and
c) whether the controller inhibits the functionality of the No-Deallocation After Sanitize bit in the Sanitize command.

If an unsupported sanitize operation type is selected by a Sanitize command, then the controller shall abort the command with a status of Invalid Field in Command.

If any Persistent Memory Region is enabled in an NVM subsystem, then the controller shall abort any Sanitize command with a status of Sanitize Prohibited While Persistent Memory Region is Enabled. A sanitize operation is prohibited while the Persistent Memory Region is enabled.

If a firmware activation with reset is pending, then the controller shall abort any Sanitize command.

If the Firmware Commit command that established the pending firmware activation with reset condition returned a status code of:

a) Firmware Activation Requires Controller Level Reset;
b) Firmware Activation Requires Conventional Reset; or
c) Firmware Activation Requires NVM Subsystem Reset.

then the controller should abort the Sanitize command with that same status code.

If the Firmware Commit command that established the pending firmware activation with reset condition completed successfully or returned a status code other than:

a) Firmware Activation Requires Controller Level Reset;
b) Firmware Activation Requires Conventional Reset; or
c) Firmware Activation Requires NVM Subsystem Reset,

then the controller should abort the Sanitize command with a status code of Firmware Activation Requires Controller Level Reset.

Activation of new firmware is prohibited during a sanitize operation (refer to section 8.15.1).

Support for Sanitize commands in a Controller Memory Buffer (i.e., submitted to an Admin Submission Queue in a Controller Memory Buffer or specifying an Admin Completion Queue in a Controller Memory Buffer) is implementation specific. If an implementation does not support Sanitize commands in a Controller Memory Buffer and a controller's Admin Submission Queue or Admin Completion Queue is in the Controller Memory Buffer, then the controller shall abort all Sanitize commands with a status of Command Not Supported for Queue in CMB.

All sanitize operations (i.e., Block Erase, Crypto Erase, and Overwrite) are performed in the background (i.e., Sanitize command completion does not indicate sanitize operation completion). If a sanitize operation is started, then the controller shall complete the Sanitize command with a status of Successful Completion. If the controller completes a Sanitize command with any status other than Successful Completion, then the controller:

- shall not start the sanitize operation for that command;
- shall not modify the Sanitize Status log page; and
- shall not alter any user data.

The Sanitize command uses Command Dword 10 and Command Dword 11. All other command specific fields are reserved.

Figure 334: Sanitize – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:10</td><td>Reserved</td></tr>
<tr><td>09</td><td>No-Deallocate After Sanitize: If set to ‘1’ and the No-Deallocate Inhibited bit (refer to Figure 251) is cleared to ‘0’, then the controller shall not deallocate any logical blocks as a result of successfully completing the sanitize operation. If:

a) cleared to ‘0’; or
b) set to ‘1’ and the No-Deallocate Inhibited bit is set to ‘1’,

then the controller should deallocate logical blocks as a result of successfully completing the sanitize operation. This bit shall be ignored if the Sanitize Action field is set to 001b (i.e., Exit Failure Mode).</td></tr>
<tr><td>08</td><td>Overwrite Invert Pattern Between Passes (OIPBP): If set to ‘1’, then the Overwrite Pattern shall be inverted between passes. If cleared to ‘0’, then the overwrite pattern shall not be inverted between passes. This bit shall be ignored unless the Sanitize Action field is set to 011b (i.e., Overwrite).</td></tr>
<tr><td>07:04</td><td>Overwrite Pass Count (OWPASS): This field specifies the number of overwrite passes (i.e., how many times the media is to be overwritten) using the data from the Overwrite Pattern field of this command. A value of 0h specifies 16 overwrite passes. This field shall be ignored unless the Sanitize Action field is set to 011b (i.e., Overwrite).</td></tr>
<tr><td>03</td><td>Allow Unrestricted Sanitize Exit (AUSE): If set to ‘1’, then the sanitize operation is performed in unrestricted completion mode. If cleared to ‘0’, then the sanitize operation is performed in restricted completion mode. This bit shall be ignored if the Sanitize Action field is set to 001b (i.e., Exit Failure Mode).</td></tr>
<tr><td>02:00</td><td>Sanitize Action (SANACT): This field specifies the sanitize action to perform.

<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>000b</td><td>Reserved</td></tr>
<tr><td>001b</td><td>Exit Failure Mode</td></tr>
<tr><td>010b</td><td>Start a Block Erase sanitize operation</td></tr>
<tr><td>011b</td><td>Start an Overwrite sanitize operation</td></tr>
<tr><td>100b</td><td>Start a Crypto Erase sanitize operation</td></tr>
<tr><td>101b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

Figure 335: Sanitize – Command Dword 11

Bits	Description
31:00	**Overwrite Pattern (OVRPAT):** This field is ignored unless the Sanitize Action field in Command Dword 10 is set to 011b (i.e., Overwrite). This field specifies a 32-bit pattern that is used for the Overwrite sanitize operation. Refer to section 8.15.

5.24.1 Command Completion

When the command is complete, the controller shall post a completion queue entry to the Admin Completion Queue indicating the status for the command. All sanitize operations are performed in the background (i.e., completion of the Sanitize command does not indicate completion of the sanitize operation). If a sanitize operation is started, then the Sanitize Status log page shall be updated before posting the completion queue entry for the command that started that sanitize operation.

Sanitize command specific status values are defined in Figure 336.

Figure 336: Sanitize – Command Specific Status Values

Value	Description
0Bh	**Firmware Activation Requires Conventional Reset:** The sanitize operation could not be started because a firmware activation is pending and a Conventional Reset is required.
10h	**Firmware Activation Requires NVM Subsystem Reset:** The sanitize operation could not be started because a firmware activation is pending and an NVM Subsystem Reset is required.
11h	**Firmware Activation Requires Controller Level Reset:** The sanitize operation could not be started because a firmware activation is pending and a Controller Level Reset is required.
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
23h	**Sanitize Prohibited While Persistent Memory Region is Enabled:** A sanitize operation is prohibited while the Persistent Memory Region is enabled.

5.25 Security Receive command – NVM Command Set Specific

The Security Receive command transfers the status and data result of one or more Security Send commands that were previously submitted to the controller.

The association between a Security Receive command and previous Security Send commands is dependent on the Security Protocol. The format of the data to be transferred is dependent on the Security Protocol. Refer to SPC-4 for Security Protocol details.

Each Security Receive command returns the appropriate data corresponding to a Security Send command as defined by the rules of the Security Protocol. The Security Receive command data may not be retained if there is a loss of communication between the controller and host, or if a Controller Level Reset occurs.

The fields used are Data Pointer, Command Dword 10, and Command Dword 11 fields. All other command specific fields are reserved.

Figure 337: Security Receive – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field.

Figure 338: Security Receive – Command Dword 10

Bits	Description
31:24	**Security Protocol (SECP):** This field specifies the security protocol as defined in SPC-4. The controller shall abort the command with status of Invalid Field in Command if an unsupported value of the Security Protocol is specified.
23:16	**SP Specific 1 (SPSP1):** The value of this field contains bits 15:08 of the Security Protocol Specific field as defined in SPC-4.
15:08	**SP Specific 0 (SPSP0):** The value of this field contains bits 07:00 of the Security Protocol Specific field as defined in SPC-4.
07:00	**NVMe Security Specific Field (NSSF):** Refer to Figure 340 for definition of this field for Security Protocol EAh. For all other Security Protocols this field is reserved.

Figure 339: Security Receive – Command Dword 11

Bits	Description
31:00	**Allocation Length (AL):** The value of this field is specific to the Security Protocol In command with the INC_512 field cleared to 0h as defined in SPC-4.

5.25.1 Command Completion

If the command is completed, then the controller shall post a completion queue entry to the Admin Completion Queue indicating the status for the command.

5.25.2 Security Protocol 00h

A Security Receive command with the Security Protocol field cleared to 00h shall return information about the security protocols supported by the controller. This command is used in the security discovery process and is not associated with a Security Send command. Refer to SPC-4 for the details of Security Protocol 00h and the SP Specific field.

5.25.3 Security Protocol EAh

Security Protocol EAh is assigned for NVMe interface use (refer to ACS-4). This protocol may be used in Security Receive and Security Send commands. The specific usage type is defined by the Security Protocol Specific Field defined in Figure 340.

Figure 340: Security Protocol EAh – Security Protocol Specific Field Values

SP Specific (SPSP) Value	Description	NVMe Security Specific Field (NSSF) Definition
0001h	Replay Protected Memory Block	RPMB Target
0002h to FFFFh	Reserved	Reserved

5.26 Security Send command – NVM Command Set Specific

The Security Send command is used to transfer security protocol data to the controller. The data structure transferred to the controller as part of this command contains security protocol specific commands to be performed by the controller. The data structure transferred may also contain data or parameters associated with the security protocol commands. Status and data that is to be returned to the host for the security protocol commands submitted by a Security Send command are retrieved with the Security Receive command defined in section 5.25.

The association between a Security Send command and subsequent Security Receive command is Security Protocol field dependent as defined in SPC-4.

The fields used are Data Pointer, Command Dword 10, and Command Dword 11 fields. All other command specific fields are reserved.

Figure 341: Security Send – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field.

Figure 342: Security Send – Command Dword 10

Bits	Description
31:24	**Security Protocol (SECP):** This field specifies the security protocol as defined in SPC-4. The controller shall abort the command with status Invalid Field in Command if a reserved value of the Security Protocol is specified.
23:16	**SP Specific 1 (SPSP1):** The value of this field contains bits 15:08 of the Security Protocol Specific field as defined in SPC-4.

Figure 342: Security Send – Command Dword 10

Bits	Description
15:08	**SP Specific 0 (SPSP0):** The value of this field contains bits 07:00 of the Security Protocol Specific field as defined in SPC-4.
07:00	**NVMe Security Specific Field (NSSF):** Refer to Figure 340 for definition of this field for Security Protocol EAh. For all other Security Protocols this field is reserved.

Figure 343: Security Send – Command Dword 11

Bits	Description
31:00	**Transfer Length (TL):** The value of this field is specific to the Security Protocol Out command with the INC_512 field cleared to 0h as defined in SPC-4.

5.26.1 Command Completion

If the command is completed, then the controller shall post a completion queue entry to the Admin Completion Queue indicating the status for the command.

5.27 Get LBA Status command – NVM Command Set Specific

The Get LBA Status command requests information about Potentially Unrecoverable LBAs (refer to section 8.22). If the Get LBA Status command completes successfully, then the LBA Status Descriptor List, defined in Figure 348, is returned in the data buffer for that command.

The Get LBA Status command uses the Data Pointer, Command Dword 10, Command Dword 11, Command Dword 12, and Command Dword 13 fields. All other command specific fields are reserved.

The Maximum Number of Dwords (MNDW) field contains the maximum number of dwords to return. Upon successful command completion, the actual amount of data returned by the controller is indicated by the Number of LBA Status Descriptors (NLSD) field in the LBA Status Descriptor List.

A controller identifies Potentially Unrecoverable LBAs using the following two report types:

a) **Tracked LBAs:** a list of Potentially Unrecoverable LBAs associated with physical storage. These may be discovered through a background scan where the controller examines the media in the background or discovered through other means. The Tracked LBA list is able to be returned without significant delay; or
b) **Untracked LBAs:** a list of Potentially Unrecoverable LBAs generated by a scan originated by a Get LBA Status command with the ATYPE field set to 10h. The controller scans internal data structures related to LBAs to determine which LBAs are Potentially Unrecoverable LBAs. The controller may use this scan to determine which LBAs in which namespaces are affected by a component (e.g., die or channel) failure. Significant delays may be incurred during the processing of a Get LBA Status command with the ATYPE field set to 10h. After discovery of Untracked LBAs, they may or may not be added to the list of Tracked LBAs.

In response to a Get LBA Status command, the controller shall return LBA Status Descriptors that describe LBAs written by a Write Uncorrectable command in addition to any other LBAs that may return an Unrecovered Read Error status discovered through other mechanisms. The list of Tracked LBAs and the list of Untracked LBAs may include LBA Status Descriptor Entries that describe LBAs written by a Write Uncorrectable command. If an LBA Status Descriptor Entry describes LBAs written by a Write Uncorrectable command, then bit 1 in the Status field of that entry should be set to ‘1’.

Figure 344: Get LBA Status – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the start of the data buffer. Refer to Figure 106 for the definition of this field.

Figure 345: Get LBA Status – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field indicates the 64-bit address of the first logical block addressed by this command. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63:32.

Figure 346: Get LBA Status – Command Dword 12

Bits	Description
31:00	**Maximum Number of Dwords (MNDW):** This field specifies the maximum number of dwords to return. This is a 0's based value.

Figure 347: Get LBA Status – Command Dword 13

Bits	Description
31:24	**Action Type (ATYPE):** This field specifies the mechanism the controller uses in determining the LBA Status Descriptors to return as defined in Figure 349. Value / Description: 10h – Perform a scan and return Untracked LBAs and Tracked LBAs in the specified range 11h – Return Tracked LBAs in the specified range All others – Reserved
23:16	Reserved
15:00	**Range Length (RL):** This field specifies the length of the range of contiguous LBAs, beginning at Starting LBA (SLBA), that the action specified in the Action Type (ATYPE) field shall be performed on. A value of 0h in this field specifies the length of a range beginning at Starting LBA and ending at Namespace Size (NSZE) minus 1 (refer to Figure 249).

If the value in the Action Type (ATYPE) field is 10h, then:

a) the controller shall return Untracked LBAs and Tracked LBAs in the range specified in the Get LBA Status command for the namespace specified in the Namespace Identifier (CDW1.NSID);
b) the controller shall remove all LBAs in the range specified in the Get LBA Status command, which prior to processing the Get LBA Status command were successfully re-written, from relevant internal data structures (e.g., internal Tracked LBA list);
c) the controller shall ensure that any such successfully re-written logical blocks are not reported in any LBA Status Descriptor entries returned by the Get LBA Status command unless, after having been removed from relevant internal data structures and prior to processing the Get LBA Status command, were newly detected as being Potentially Unrecoverable LBAs; and
d) the list of Untracked LBAs returned by the Get LBA Status command may be discarded by the controller or added to the Tracked LBA list once the command has completed.

If the value in the Action Type (ATYPE) field is 11h, then the controller shall:

a) return Tracked LBAs in the range specified in the Get LBA Status command for the namespace specified in the Namespace Identifier (CDW1.NSID) field;

b) remove all LBAs in the range specified in the Get LBA Status command, which prior to processing the Get LBA Status command were successfully re-written, from relevant internal data structures (e.g., internal Tracked LBA list);
c) ensure that any such successfully re-written logical blocks are not reported in any LBA Status Descriptor entries returned by the Get LBA Status command unless, after having been removed from relevant internal data structures and prior to processing the Get LBA Status command, were newly detected as being Potentially Unrecoverable LBAs; and
d) not perform a foreground scan to generate and return Untracked LBAs.

Figure 348: LBA Status Descriptor List

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>03:00</td><td>Number of LBA Status Descriptors (NLSD): This field indicates the number of LBA Status Descriptor entries returned by the controller in this data structure. An LBA Status Descriptor List which indicates that no LBA Status Descriptor entries have been returned (i.e., NLSD is cleared to ‘0’) is a valid LBA Status Descriptor List.</td></tr>
<tr><td>04</td><td>Completion Condition (CMPC): If the command completes successfully, then this field indicates the condition that caused completion of the Get LBA Status command. If there are no more LBA Status Descriptor Entries to transfer in the specified range, the controller shall return Completion Condition 2h.
<table>
<tr><th>Code</th><th>Definition</th></tr>
<tr><td>0h</td><td>No indication of the completion condition.</td></tr>
<tr><td>1h</td><td>The command completed due to transferring the amount of data specified in the MNDW field. There may be more LBA Status Descriptor Entries to transfer in the specified range.</td></tr>
<tr><td>2h</td><td>The command completed due to having performed the action specified in the Action Type field over the number of logical blocks specified in the Range Length field. There are no more LBA Status Descriptor Entries to transfer in the specified range.</td></tr>
<tr><td>All others</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>07:05</td><td>Reserved</td></tr>
<tr><td>23:08</td><td>LBA Status Descriptor Entry 0: This field contains the first LBA Status Descriptor Entry in the list, if present.</td></tr>
<tr><td>39:24</td><td>LBA Status Descriptor Entry 1: This field contains the second LBA Status Descriptor Entry in the list, if present.</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>(N*16+23): (N*16+8)</td><td>LBA Status Descriptor Entry N: This field contains the N+1 LBA Status Descriptor Entry in the list, if present.</td></tr>
</table>

Figure 349: LBA Status Descriptor Entry

Bytes	Description
07:00	**Descriptor Starting LBA (DSLBA):** This field specifies the 64-bit address of the first logical block of the LBA range for which this LBA Status Descriptor reports LBA status.
11:08	**Number of Logical Blocks (NLB):** This field contains the number of contiguous logical blocks reported in this LBA Status Descriptor. The controller should return the largest aggregated possible value in this field. This is a 0’s based value.
12	Reserved

Figure 349: LBA Status Descriptor Entry

<table>
<tr><th>Bytes</th><th>Description</th></tr>
<tr><td>13</td><td>Status: This field contains additional status about this LBA range.

<table>
<tr><th>Bits</th><th>Definition</th></tr>
<tr><td>7:2</td><td>Reserved</td></tr>
<tr><td>1</td><td>If set to ‘1’, this LBA range describes LBAs written with a Write Uncorrectable command.

If cleared to ‘0’, this LBA range may or may not describe LBAs written with a Write Uncorrectable command.</td></tr>
<tr><td>0</td><td>If set to ‘1’, a read, verify, or compare command to each LBA reported in this LBA Status Descriptor may result in a command completion with Unrecovered Read Error status.

If cleared to ‘0’, the controller has not detected that a read, verify, or compare command to each LBA reported in this LBA Status Descriptor may result in a command completion with Unrecovered Read Error status.</td></tr>
</table></td></tr>
<tr><td>15:14</td><td>Reserved</td></tr>
</table>

The Descriptor Starting LBA (DSLBA) field in the first LBA Status Descriptor entry returned in the LBA Status Descriptor List shall contain the lowest numbered LBA that is greater than or equal to the value specified in the Starting LBA field in the Get LBA Status command.

For subsequent LBA Status Descriptor entries, the contents of the Descriptor Starting LBA field shall contain the value of the lowest numbered LBA meeting the requirements for the specified Action Type value that is greater than the sum of the values in:

a) the Descriptor Starting LBA field in the previous LBA Status Descriptor entry; and
b) the Number of Logical Blocks field in the previous LBA Status Descriptor entry.

5.27.1 Command Completion

When the command is completed, the controller posts a completion queue entry to the Admin Completion Queue indicating the status for the command.

6 NVM Command Set

An NVM subsystem is comprised of some number of controllers, where each controller may access some number of namespaces, where each namespace is comprised of some number of logical blocks. A logical block is the smallest unit of data that may be read or written from the controller. The logical block data size, reported in bytes, is always a power of two. Logical block sizes may be 512 bytes, 1 KiB, 2 KiB, 4 KiB, 8 KiB, etc. Supported logical block sizes are reported in the Identify Namespace data structure.

The NVM Command Set includes the commands listed in Figure 350. Refer to section 7.1 for mandatory, optional, and prohibited commands for the various controller types. The following subsections describe the definition for each of these commands. Commands shall only be submitted by the host when the controller is ready as indicated in the Controller Status register (CSTS.RDY) and after appropriate I/O Submission Queue(s) and I/O Completion Queue(s) have been created.

The Submission Queue Entry (SQE) structure and the fields that are common to all NVM commands are defined in section 4.2. The Completion Queue Entry (CQE) structure and the fields that are common to all NVM commands are defined in section 4.6. The command specific fields in the SQE and CQE structures (i.e., SQE Command Dwords 10-15 and CQE Dword 0) for the NVM Command Set are defined in this section.

In the case of Compare, Read, Verify, Write, and Write Zeroes commands, the host may indicate whether a time limit should be applied to error recovery for the operation by setting the Limited Retry (LR) bit in the command. The time limit is specified in the Error Recovery feature, specified in section 5.21.1.5. If the host does not specify a time limit should be applied, then the controller should apply all error recovery means to complete the operation.

Figure 350: Opcodes for NVM Commands

Opcode by Field			**Combined Opcode [1]**	**Command [2]**	**Reference Section**
(07)	**(06:02)**	**(01:00)**			
Standard Command	**Function**	**Data Transfer [3]**			
0b	000 00b	00b	00h	Flush [4]	6.8
0b	000 00b	01b	01h	Write	6.15
0b	000 00b	10b	02h	Read	6.9
0b	000 01b	00b	04h	Write Uncorrectable	6.16
0b	000 01b	01b	05h	Compare	6.6
0b	000 10b	00b	08h	Write Zeroes	6.17
0b	000 10b	01b	09h	Dataset Management	6.7
0b	000 11b	00b	0Ch	Verify	6.14
0b	000 11b	01b	0Dh	Reservation Register	6.11
0b	000 11b	10b	0Eh	Reservation Report	6.13
0b	001 00b	01b	11h	Reservation Acquire	6.10
0b	001 01b	01b	15h	Reservation Release	6.12
Vendor Specific					
1b	n/a	NOTE 3	80h to FFh	Vendor specific	

NOTES:
1. Opcodes not listed are reserved.
2. All NVM commands use the Namespace Identifier (NSID) field. The value FFFFFFFFh is not supported in this field unless footnote 4 in this figure indicates that a specific command does support that value.
3. Indicates the data transfer direction of the command. All options to the command shall transfer data as specified or transfer no data. All commands, including vendor specific commands, shall follow this convention: 00b = no data transfer; 01b = host to controller; 10b = controller to host; 11b = bidirectional.
4. This command may support the use of the Namespace Identifier (NSID) field set to FFFFFFFFh.

6.1 Namespaces

6.1.1 Namespace Overview

A namespace is a collection of logical blocks whose logical block addresses range from 0 to the size of the namespace – 1. A namespace ID (NSID) is an identifier used by a controller to provide access to a namespace.

6.1.2 Valid and Invalid NSIDs

Valid NSIDs are the range of possible NSIDs that may be used to refer to namespaces that exist in the NVM subsystem. Any NSID is valid, except if that NSID is 0h or greater than the Number of Namespaces field reported in the Identify Controller data structure (refer to Figure 251). NSID FFFFFFFFh is a broadcast value that is used to specify all namespaces. An invalid NSID is any value that is not a valid NSID and is also not the broadcast value.

Valid NSIDs are:

a) allocated or unallocated in the NVM subsystem; and
b) active or inactive for a specific controller.

6.1.3 Allocated and Unallocated NSID Types

In the NVM subsystem, a valid NSID is:

a) an allocated NSID; or
b) an unallocated NSID.

Allocated NSIDs refer to namespaces that exist in the NVM subsystem. Unallocated NSIDs do not refer to any namespaces that exist in the NVM subsystem.

6.1.4 Active and Inactive NSID Types

For a specific controller, an allocated NSID is:

a) an active NSID; or
b) an inactive NSID.

Active NSIDs for a controller refer to namespaces that are attached to that controller. Allocated NSIDs that are inactive for a controller refer to namespaces that are not attached to that controller.

Unallocated NSIDs are inactive NSIDs for all controllers in the NVM subsystem.

An allocated NSID may be an active NSID for some controllers and an inactive NSID for other controllers in the same NVM subsystem if the namespace that the NSID refers to is attached to some controllers, but not all controllers, in the NVM subsystem.

Refer to section 8.12 for actions associated with a namespace being detached or deleted.

6.1.5 NSID and Namespace Relationships

Unless otherwise noted, specifying an inactive NSID in a command that uses the Namespace Identifier (NSID) field shall cause the controller to abort the command with status Invalid Field in Command. Specifying an invalid NSID in a command that uses the NSID field shall cause the controller to abort the command with status Invalid Namespace or Format.

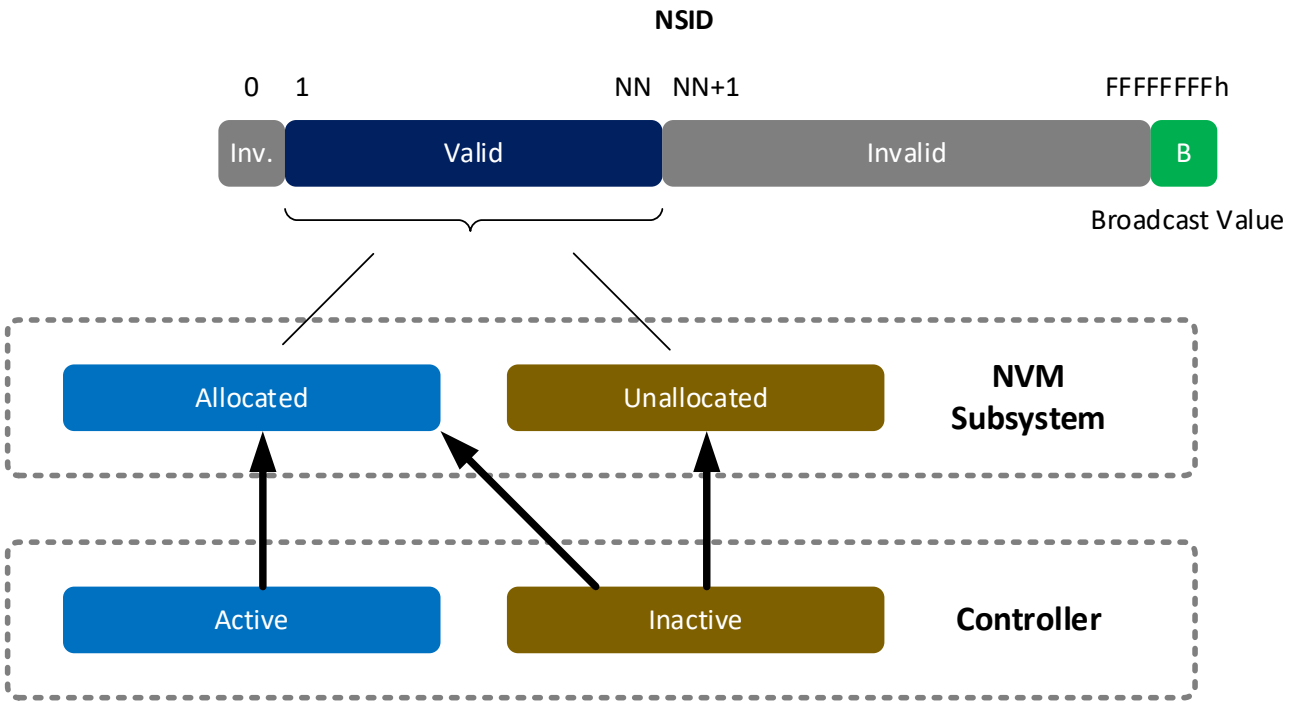
The following table summarizes the valid NSID types and Figure 351 visually shows the NSID types and how they relate.

Figure 351: NSID Types and Relationship to Namespace

Valid NSID Type	NSID relationship to namespace	Reference
Unallocated	Does not refer to any namespace that exists in the NVM subsystem	6.1.3
Allocated	Refers to a namespace that exists in the NVM subsystem	6.1.3
Inactive	Does not refer to a namespace that is attached to the controller[1]	6.1.4
Active	Refers to a namespace that is attached to the controller	6.1.4

NOTES:
1. If allocated, refers to a namespace that is not attached to the controller. If unallocated, does not refer to any namespace.

Figure 352: NSID Types



6.1.6 NSID and Namespace Usage

If Namespace Management (refer to section 8.12), ANA Reporting (refer to section 8.20), or NVM Sets (refer to section 4.9) are supported, then NSIDs shall be unique within the NVM subsystem (e.g., NSID of 3 shall refer to the same physical namespace regardless of the accessing controller). If the Namespace Management, ANA Reporting, and NVM Sets are not supported, then NSIDs:

a) for shared namespaces shall be unique; and
b) for private namespaces are not required to be unique.

The Identify command (refer to section 5.15) may be used to determine the active NSIDs for a controller and the allocated NSIDs in the NVM subsystem.

If the MNAN field (refer to Figure 251) is cleared to 0h, then the maximum number of allocated NSIDs is the same as the value reported in the NN field (refer to Figure 251). If the MNAN field is non-zero, then the maximum number of allocated NSIDs may be less than the number of namespaces (e.g., an NVM

subsystem may support a maximum valid NSID value (i.e., the NN field) set to 1,000,000 but support a maximum of 10 allocated NSID values).

To determine the active NSIDs for a particular controller, the host may follow either of the following methods:

1. Issue an Identify command with the CNS field cleared to 0h for each valid NSID (based on the Number of Namespaces value (i.e., MNAM field or NN field) in the Identify Controller data structure). If a non-zero data structure is returned for a particular NSID, then that is an active NSID; or
2. Issue an Identify command with a CNS field set to 2h to retrieve a list of up to 1,024 active NSIDs. If there are more than 1,024 active NSIDs, continue to issue Identify commands with a CNS field set to 2h until all active NSIDs are retrieved.

To determine the allocated NSIDs in the NVM subsystem, the host may issue an Identify command with the CNS field set to 10h to retrieve a list of up to 1,024 allocated NSIDs. If there are more than 1,024 allocated NSIDs, continue to issue Identify commands with a CNS field set to 10h until all allocated NSIDs are retrieved.

Namespace IDs may change across power off conditions. However, it is recommended that namespace identifiers remain static across power off conditions in order to avoid issues with EFI or OSes. To determine if the same namespace has been encountered, the host may use the:

a) UUID field in the Namespace Identification Descriptor (refer to Figure 253), if present;
b) NGUID field in the Identify Namespace data (refer to Figure 249) or in the Namespace Identification Descriptor, if present; or
c) EUI64 field in the Identify Namespace data or in the Namespace Identification Descriptor, if present.

UIDREUSE bit in the NSFEAT field (refer to Figure 249) indicates NGUID and EUI64 reuse characteristics.

A namespace may or may not have a relationship to a Submission Queue; this relationship is determined by the host software implementation. The controller shall support access to any active namespace from any I/O Submission Queue.

6.1.7 Namespace Size, Capacity and Utilization

The Identify Namespace data structure (refer to Figure 249) contains related fields reporting the Namespace Size, Capacity and Utilization:

- The Namespace Size (NSZE) field defines the total size of the namespace in logical blocks (LBA 0 through n-1).
- The Namespace Capacity (NCAP) field defines the maximum number of logical blocks that may be allocated at any point in time.
- The Namespace Utilization (NUSE) field defines the number of logical blocks currently allocated in the namespace.

The following relationship holds: Namespace Size >= Namespace Capacity >= Namespace Utilization.

When the THINP bit in the NSFEAT field is set to ‘1’, the controller:

- may report a value in the Namespace Capacity field that is smaller than the value in the Namespace Size field; and
- shall track the number of allocated blocks in the Namespace Utilization field.

When the THINP bit in the NSFEAT field is cleared to ‘0’, the controller:

- shall report a value in the Namespace Capacity field that is equal to the Namespace Size; and
- may report a value in the Namespace Utilization field that is always equal to the value in the Namespace Capacity field.

A logical block shall be marked as allocated when it is written with:

- a Write command;

- a Write Uncorrectable command; or
- a Write Zeroes command that does not deallocate the logical block (refer to section 6.7.1.1).

A logical block may be marked as allocated as the result of:

- a Write command not addressing the logical block; or
- a Write Zeroes command not addressing the logical block (refer to section 6.7.1.1).

A logical block may be marked deallocated as the result of:

- a Dataset Management command (refer to section 6.7.1.1); or
- a Write Zeroes command addressing the logical block (refer to section 6.7.1.1); or
- a Sanitize operation.

If the controller supports Asymmetric Namespace Access Reporting (i.e., bit 3 set to '1' in the CMIC field in the Identify Controller data structure (refer to Figure 251)), then the NUSE field (refer to Figure 249) and the NVMCAP field (refer to Figure 249) are cleared to 0h if the relationship between the controller and the namespace is in the ANA Inaccessible state (refer to section 8.20.3.3) or the ANA Persistent Loss state (refer to section 8.20.3.4). The Namespace Attribute Changed event is not generated for changes to these fields that result from ANA state changes as described in Figure 150. The host uses the Asymmetric Namespace Access Change Notices as an indication of these changes.

6.2 Fused Operations

The command sequences that may be used in a fused operation for the NVM Command Set are defined in Figure 353. Refer to section 4.12 for details on fused operations.

Figure 353: Supported Fused Operations

Command 1	Command 2	Fused Operation
Compare	Write	Compare and Write

6.2.1 Compare and Write

The Compare and Write fused operation compares the contents of the logical block(s) specified in the Compare command to the data stored at the indicated LBA range. If the compare is successful, then the LBA range is updated with the data provided in the Write command. If the Compare operation is not successful, then the Write operation is aborted with a status of Command Aborted due to Failed Fused Command and the contents in the LBA range are not modified. If the Write operation is not successful, the Compare operation completion status is unaffected.

Note: To ensure the Compare and Write is an atomic operation in a multi-host environment, host software should ensure that the size of a Compare and Write fused operation is no larger than the ACWU/NACWU (refer to section 6.4) and that Atomic Boundaries are respected (refer to section 6.4.3). Controllers may abort a Compare and Write fused operation that is larger than ACWU/NACWU or that crosses an Atomic Boundary with an error of Atomic Write Unit Exceeded.

6.3 Command Ordering Requirements

For all commands which are not part of a fused operation (refer to section 4.12), or for which the write size is greater than AWUN, each command is processed as an independent entity without reference to other commands submitted to the same I/O Submission Queue or to commands submitted to other I/O Submission Queues. Specifically, the controller is not responsible for checking the LBA of a Read or Write command to ensure any type of ordering between commands. For example, if a Read is submitted for LBA *x* and there is a Write also submitted for LBA *x*, there is no guarantee of the order of completion for those commands (the Read may finish first or the Write may finish first). If there are ordering requirements

between these commands, host software or the associated application is required to enforce that ordering above the level of the controller.

The ordering requirements for fused operations are described in section 4.12.

6.4 Atomic Operations

Figure 354 is an overview of the parameters that define the controller's support for atomic operations. These parameters may affect command behavior and execution order based on write size (on a per controller or a per namespace basis).

Figure 354: Atomicity Parameters

	Parameter Name	Value[1]
Controller Atomic Parameters (refer to the Identify Controller data structure in Figure 251)	Atomic Write Unit Normal (AWUN)	
	Atomic Write Unit Power Fail (AWUPF)	≤ AWUN
	Atomic Compare and Write Unit (ACWU)	
Namespace Atomic Parameters (refer to the Identify Namespace data structure in Figure 249)	Namespace Atomic Write Unit Normal (NAWUN)	≥ AWUN
	Namespace Atomic Write Unit Power Fail (NAWUPF)	≥ AWUPF ≤ NAWUN
	Namespace Atomic Compare and Write Unit (NACWU)	≥ ACWU
Namespace Atomic Boundary Parameters (refer to the Identify Namespace data structure in Figure 249)	Namespace Atomic Boundary Size Normal (NABSN)	≥ NAWUN
	Namespace Atomic Boundary Offset (NABO)	≤ NABSN ≤ NABSPF
	Namespace Atomic Boundary Size Power Fail (NABSPF)	≥ NAWUPF

NOTES:
1. When the parameter is supported, the value shall meet the listed condition(s).

The NVM subsystem reports in the Identify Controller data structure the size in logical blocks of the write operation guaranteed to be written atomically under various conditions, including normal operation, power fail, and in a Compare & Write fused operation. The values reported in the Identify Controller data structure are valid across all namespaces with any supported namespace format, forming a baseline value that is guaranteed not to change.

An NVM subsystem may report per namespace values for these fields that are specific to the namespace format and are indicated in the Identify Namespace data structure (refer to Figure 249). If an NVM subsystem reports a per namespace value, then that value shall be greater than or equal to the corresponding baseline value indicated in the Identify Controller data structure (refer to Figure 251).

The values are reported in the fields (Namespace) Atomic Write Unit Normal, (Namespace) Atomic Write Unit Power Fail, and (Namespace) Atomic Compare & Write Unit in the Identify Controller data structure or the Identify Namespace data structure depending on whether the values are the baseline or namespace specific.

A controller may support Atomic Boundaries that shall not be crossed by an atomic operation. The Namespace Atomic Boundary Parameters (NABSN, NABO, and NABSPF) define these boundaries for a namespace. A namespace supports Atomic Boundaries if NABSN or NABSPF is set to a non-zero value. A namespace that does not support Atomic Boundaries shall clear the NABSN and NABSPF fields to 0h. Namespace Atomicity Parameter and Namespace Atomic Boundary Parameter values may be format specific and may change if the namespace format is modified.

In the case of a shared namespace, operations performed by an individual controller are atomic to the shared namespace at the write atomicity level reported in the corresponding Identify Controller or Identify Namespace data structures of the controller to which the command was submitted.

6.4.1 AWUN/NAWUN

AWUN/NAWUN control the atomicity of command execution in relation to other commands. They impose inter-command serialization of writing of blocks of data to the NVM and prevent blocks of data ending up on the NVM containing partial data from one new command and partial data from one or more other new commands.

If a write command is submitted with size less than or equal to the AWUN/NAWUN value and the write command does not cross an atomic boundary (refer to section 6.4.3), then the host is guaranteed that the write command is atomic to the NVM with respect to other read or write commands. If a write command is submitted with size greater than the AWUN/NAWUN value or crosses an atomic boundary, then there is no guarantee of command atomicity. AWUN/NAWUN does not have any applicability to write errors caused by power failure or other error conditions (refer to Atomic Write Unit Power Fail).

The host may indicate that AWUN and NAWUN are not necessary by configuring the Write Atomicity Normal feature (refer to section 5.21.1.10), which may result in higher performance in some implementations.

6.4.1.1 AWUN/NAWUN Example (Informative)

In this example, AWUN/NAWUN has a value of 2K (equivalent to four 512 byte logical blocks) and the namespace atomic boundary sizes (NABSN and NABSPF) are 0h. The host issues two write commands, each with a length of 2K (i.e., four logical blocks). Command A writes LBAs 0-3 and command B writes LBAs 1-4.

Since the size of both command A and command B is less than or equal to the value of AWUN/NAWUN, the controller serializes these two write commands so that the resulting data in LBAs 0-4 reflects command A followed by command B, or command B followed by command A, but not an intermediate state where some of the logical blocks are written with data from command A and others are written with data from command B. Figure 355 shows valid results of the data in LBAs 0-4 and examples of invalid results (of which there are more possible combinations).

Figure 355: AWUN/NAWUN Example Results

	LBA 0	1	2	3	4	5	6	7
Valid Result	A	A	A	A	B			
Valid Result	A	B	B	B	B			
Invalid Result	A	A	B	B	B			
Invalid Result	A	B	A	A	B			

If the size of write commands A and B is larger than the AWUN/NAWUN value, then there is no guarantee of ordering. After execution of command A and command B, there may be an arbitrary mix of data from command A and command B in the LBA range specified.

6.4.2 AWUPF/NAWUPF

AWUPF and NAWUPF indicate the behavior of the controller if a power fail or other error condition interrupts a write operation causing a torn write. A torn write is a write operation where only some of the logical blocks that are supposed to be written contiguously are actually stored on the NVM, leaving the target logical blocks in an indeterminate state in which some logical blocks contain original data and some logical blocks contain new data from the write operation.

If a write command is submitted with size less than or equal to the AWUPF/NAWUPF value and the write command does not cross an atomic boundary (refer to section 6.4.3), the controller guarantees that if the

command fails due to a power failure or other error condition, then subsequent read commands for the logical blocks associated with the write command shall return one of the following:

- All old data (i.e., original data on the NVM in the LBA range addressed by the interrupted write); or
- All new data (i.e., all data to be written to the NVM by the interrupted write).

If a write command is submitted with size greater than the AWUPF/NAWUPF value or crosses an atomic boundary, then there is no guarantee of the data returned on subsequent reads of the associated logical blocks.

6.4.2.1 AWUPF/NAWUPF Example (Informative)

In this example, AWUPF/NAWUPF has a value of 1K (equivalent to two 512 byte logical blocks), AWUN/NAWUN has a value of 2K (equivalent to four 512 byte logical blocks) and the namespace atomic boundary sizes (NABSN and NABSPF) are 0h. Command A writes LBAs 0 to 1. Figure 356 shows the initial state of the NVM.

Figure 356: AWUPF/NAWUPF Example Initial State of NVM

	LBA 0	1	2	3	4	5	6	7
	C	B	B	B	B			

Command A begins executing but is interrupted by a power failure during the writing of the logical block at LBA 1. Figure 357 describes valid and invalid results.

Figure 357: AWUPF/NAWUPF Example Final State of NVM

	LBA 0	1	2	3	4	5	6	7
Valid Result	A	A	B	B	B			
Valid Result	C	B	B	B	B			
Invalid Result	A	B	B	B	B			
Invalid Result	C	A	B	B	B			
Invalid Result	D	D	B	B	B			

If the size of write command A is larger than the AWUPF/NAWUPF value, then there is no guarantee of the state of the data contained in the specified LBA range after the power fail or error condition.

After a write command has completed, reads for that location which are subsequently submitted shall return the data from that write command and not an older version of the data from previous write commands with the following exception;

If all of the following conditions are met:

a) the controller supports a volatile write cache;
b) the volatile write cache is enabled;
c) the FUA bit for the write is not set;
d) no flush commands, associated with the same namespace as the write, successfully completed before shutdown; and
e) a controller shutdown occurs without completing the normal or abrupt shutdown procedure outlined in section 7.6.2,

then subsequent reads for locations written to the volatile write cache that were not written to non-volatile storage may return older data.

6.4.3 Atomic Boundaries

Atomic Boundaries control how the atomicity guarantees defined in section 6.4 are enforced by the controller, with the added constraint of the alignment of the LBA range specified in the command. Atomic Boundaries are defined on a per namespace basis only. The namespace supports Atomic Boundaries if NABSN or NABSPF are set to non-zero values.

To ensure backwards compatibility, the values reported for AWUN, AWUPF, and ACWU shall be set such that they are supported even if a write crosses an atomic boundary. If a controller does not guarantee atomicity across atomic boundaries, the controller shall set AWUN, AWUPF, and ACWU to 0h (1 LBA).

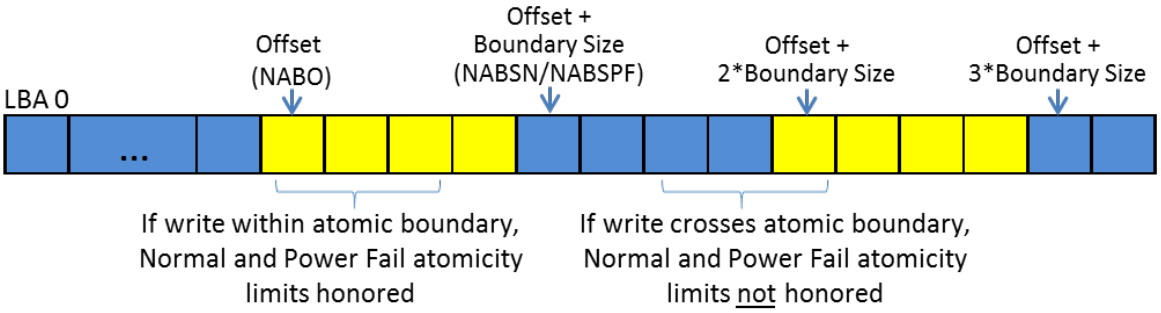
The boundary size shall be greater than or equal to the corresponding atomic write size (i.e., NABSN/NABSPF shall be greater than or equal to NAWUN/NAWUPF, respectively). NABO shall be less than or equal to NABSN and NABSPF.

For Boundary Offset (NABO) and Boundary Size (NABSN or NABSPF), the LBA range in a command is within a Namespace Atomic Boundary if none of the logical block addresses in the range cross: Boundary Offset + (y * Boundary Size); for any integer y ≥ 0.

If a write command crosses the atomic boundary specified by the NABSN value, then the atomicity based on the NAWUN parameters is not guaranteed. If a write command crosses the atomic boundary specified by the NABSPF value, then the atomicity based on the NAWUPF parameters is not guaranteed.

Figure 358 shows an example of the behavior of Atomic Boundaries. Writes to an individual blue or yellow section do not cross an atomic boundary.

Figure 358: Atomic Boundaries Example



6.5 End-to-end Protection Information

The commands that include data transfer may utilize end-to-end data protection. Within these commands, the protection information action and protection information check field is specified as defined in Figure 359.

Figure 359: Protection Information Field Definition

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>03</td><td>Protection Information Action (PRACT): The protection information action bit indicates the action to take for the protection information. If the namespace is not formatted to use end-to-end protection information, then this bit is ignored. Refer to section 8.3.
<table>
<tr><th>PRACT Value</th><th>Metadata Size</th><th>Description</th></tr>
<tr><td>1b</td><td>8 Bytes</td><td>The protection information is stripped (read) or inserted (write).</td></tr>
<tr><td>1b</td><td>> 8 Bytes</td><td>The protection information is passed (read) or replaces the first or last 8 bytes of the metadata (write).</td></tr>
<tr><td>0b</td><td>any</td><td>The protection information is passed (read and write).</td></tr>
</table></td></tr>
<tr><td>02:00</td><td>Protection Information Check (PRCHK): The protection information check field specifies the fields that shall be checked as part of end-to-end data protection processing. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.
<table>
<tr><th>Bit</th><th>Definition</th></tr>
<tr><td>02</td><td>If set to ‘1’ enables protection information checking of the Guard field. If cleared to ‘0’, the Guard field is not checked.</td></tr>
<tr><td>01</td><td>If set to ‘1’ enables protection information checking of the Application Tag field. If cleared to ‘0’, the Application Tag field is not checked.</td></tr>
<tr><td>00</td><td>If set to ‘1’ enables protection information checking of the Logical Block Reference Tag field. If cleared to ‘0’, the Logical Block Reference Tag field is not checked.</td></tr>
</table></td></tr>
</table>

6.6 Compare command

The Compare command reads the logical blocks specified by the command from the medium and compares the data read to a comparison data buffer transferred as part of the command. If the data read from the controller and the comparison data buffer are equivalent with no miscompares, then the command completes successfully. If there is any miscompare, the command completes with an error of Compare Failure.

If metadata is provided, then a comparison is also performed for the metadata, excluding protection information. The command may specify protection information to be checked as described in section 8.3.1.4.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 14, and Command Dword 15 fields. If the command uses PRPs for the data transfer, then the Metadata Pointer, PRP Entry 1, and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the Metadata SGL Segment Pointer and SGL Entry 1 fields are used. All other command specific fields are reserved.

Figure 360: Compare – Metadata Pointer

Bits	Description
63:00	**Metadata Pointer (MPTR):** This field contains the Metadata Pointer, if applicable. Refer to Figure 106 for the definition of this field.

Figure 361: Compare – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the data to use for the compare. Refer to Figure 106 for the definition of this field.

Figure 362: Compare – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field specifies the 64-bit address of the first logical block to compare against as part of the operation. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63:32.

Figure 363: Compare – Command Dword 12

Bits	Description
31	**Limited Retry (LR):** If set to '1', the controller should apply limited retry efforts. If cleared to '0', the controller should apply all available error recovery means to retrieve the data for comparison.
30	**Force Unit Access (FUA):** If set to '1', then for data and metadata, if any, associated with logical blocks specified by the Compare command, the controller shall: 1) commit that data and metadata, if any, to non-volatile media; and 2) read the data and metadata, if any, from non-volatile media. If cleared to '0', then this bit has no effect.
29:26	**Protection Information Field (PRINFO):** Specifies the protection information action and check field, as defined in Figure 359. The Protection Information Action (PRACT) bit shall be cleared to '0'. If the Protection Information Check (PRCHK) field is non-zero, a check is performed on the logical block read from NVM (refer to section 8.3.1.4).
25:16	Reserved
15:00	**Number of Logical Blocks (NLB):** This field specifies the number of logical blocks to be compared. This is a 0's based value.

Figure 364: Compare – Command Dword 14

Bits	Description
31:00	**Expected Initial Logical Block Reference Tag (EILBRT):** This field specifies the Initial Logical Block Reference Tag expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

Figure 365: Compare – Command Dword 15

Bits	Description
31:16	**Expected Logical Block Application Tag Mask (ELBATM):** This field specifies the Application Tag Mask expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.
15:00	**Expected Logical Block Application Tag (ELBAT):** This field specifies the Application Tag expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

6.6.1 Command Completion

If the command is completed, then the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command. If there are any miscompares between the data

read from the NVM media and the data buffer provided, then the command fails with a status code of Compare Failure.

Compare command specific status values are defined in Figure 366.

Figure 366: Compare – Command Specific Status Values

Value	Description
81h	**Invalid Protection Information:** The Protection Information Field (PRINFO) (refer to Figure 363) settings specified in the command are invalid for the Protection Information with which the namespace was formatted (refer to the PI field in Figure 332 and the DPS field in Figure 249) or the EILBRT field is invalid (refer to section 8.3.1.5).

6.7 Dataset Management command

The Dataset Management command is used by the host to indicate attributes for ranges of logical blocks. This includes attributes like frequency that data is read or written, access size, and other information that may be used to optimize performance and reliability. This command is advisory; a compliant controller may choose to take no action based on information provided.

The command uses Command Dword 10, and Command Dword 11 fields. If the command uses PRPs for the data transfer, then the PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Figure 367: Dataset Management – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the data to use for the command. Refer to Figure 106 for the definition of this field.

Figure 368: Dataset Management – Command Dword 10

Bits	Description
31:08	Reserved
07:00	**Number of Ranges (NR):** Indicates the number of 16 byte range sets that are specified in the command. This is a 0's based value.

Figure 369: Dataset Management – Command Dword 11

Bit	Description
31:03	Reserved
02	**Attribute – Deallocate (AD):** If set to '1', then the NVM subsystem may deallocate all provided ranges. The data returned for logical blocks that were deallocated is specified in section 6.7.1.1. The data and metadata for logical blocks that are not deallocated by the NVM subsystem are not changed as the result of a Dataset Management command.
01	**Attribute – Integral Dataset for Write (IDW):** If set to '1', then the dataset should be optimized for write access as an integral unit. The host expects to perform operations on all ranges provided as an integral unit for writes, indicating that if a portion of the dataset is written it is expected that all of the ranges in the dataset are going to be written.
00	**Attribute – Integral Dataset for Read (IDR):** If set to '1', then the dataset should be optimized for read access as an integral unit. The host expects to perform operations on all ranges provided as an integral unit for reads, indicating that if a portion of the dataset is read it is expected that all of the ranges in the dataset are going to be read.

If the Dataset Management command is supported, all combinations of attributes specified in Figure 369 may be set.

The data that the Dataset Management command provides is a list of ranges with context attributes. Each range consists of a starting LBA, a length of logical blocks that the range consists of and the context attributes to be applied to that range. The length in logical blocks field is a 1-based value. The definition of the Dataset Management command Range field is specified in Figure 370. The maximum case of 256 ranges is shown.

Figure 370: Dataset Management – Range Definition

Range	Bytes	Field
Range 0	03:00	Context Attributes
	07:04	Length in logical blocks
	15:08	Starting LBA
Range 1	19:16	Context Attributes
	23:20	Length in logical blocks
	31:24	Starting LBA
…		
Range 255	4083:4080	Context Attributes
	4087:4084	Length in logical blocks
	4095:4088	Starting LBA

6.7.1 Context Attributes

The context attributes specified for each range provides information about how the range is intended to be used by host software. The use of this information is optional and the controller is not required to perform any specific action.

Note: The controller is required to maintain the integrity of data on the NVM media regardless of whether the attributes provided by host software are accurate.

Figure 371: Dataset Management – Context Attributes

Attribute	Bits	Description
Command Access Size	31:24	Number of logical blocks expected to be transferred in a single Read or Write command from this dataset. A value of 0h indicates no Command Access Size is provided.
Reserved	23:11	Reserved
WP: Write Prepare	10	If set to ‘1’, then the provided range is expected to be written in the near future.
SW: Sequential Write Range	09	If set to ‘1’, then the dataset should be optimized for sequential write access. The host expects to perform operations on the dataset as a single object for writes.
SR: Sequential Read Range	08	If set to ‘1’, then the dataset should be optimized for sequential read access. The host expects to perform operations on the dataset as a single object for reads.
Reserved	07:06	Reserved
AL: Access Latency	05:04	**Value** / **Definition** 00b – None. No latency information provided. 01b – Idle. Longer latency acceptable. 10b – Normal. Typical latency. 11b – Low. Smallest possible latency.

Figure 371: Dataset Management – Context Attributes

<table>
<tr><th>Attribute</th><th>Bits</th><th>Description</th></tr>
<tr><td>AF: Access Frequency</td><td>03:00</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>No frequency information provided.</td></tr>
<tr><td>1h</td><td>Typical number of reads and writes expected for this LBA range.</td></tr>
<tr><td>2h</td><td>Infrequent writes and infrequent reads to the LBA range indicated.</td></tr>
<tr><td>3h</td><td>Infrequent writes and frequent reads to the LBA range indicated.</td></tr>
<tr><td>4h</td><td>Frequent writes and infrequent reads to the LBA range indicated.</td></tr>
<tr><td>5h</td><td>Frequent writes and frequent reads to the LBA range indicated.</td></tr>
<tr><td>6h to Fh</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

6.7.1.1 Deallocate

A logical block that has never been written to, or which has been deallocated using the Dataset Management command, the Write Zeroes command or the Sanitize command is called a deallocated or unwritten logical block.

Using the Error Recovery feature (refer to section 5.21.1.5), host software may select the behavior of the controller when reading deallocated or unwritten blocks. The controller shall abort Read, Verify, or Compare commands that include deallocated or unwritten blocks with a status of Deallocated or Unwritten Logical Block if that error has been enabled using the DULBE bit in the Error Recovery feature. If the Deallocated or Unwritten Logical error is not enabled, the values read from a deallocated or unwritten block and its metadata (excluding protection information) shall be:

- all bytes cleared to 0h if bits 2:0 in the DLFEAT field are set to 001b;
- all bytes set to FFh if bits 2:0 in the DLFEAT field are set to 010b; or
- either all bytes cleared to 0h or all bytes set to FFh if bits 2:0 in the DLFEAT field are set to 000b.

The value read from a deallocated logical block shall be deterministic; specifically, the value returned by subsequent reads of that logical block shall be the same until a write operation occurs to that logical block. A deallocated or unwritten block is no longer deallocated or unwritten when the logical block is written. Read operations and Verify operations do not affect the deallocation status of a logical block.

The values read from a deallocated or unwritten logical block's protection information field shall:

- have the Guard field value set to FFFFh or set to the CRC for the value read from the deallocated logical block and its metadata (excluding protection information) (e.g., cleared to 0h if the value read is all bytes cleared to 0h); and
- have the Application Tag field value set to FFFFh and the Reference Tag field value set to FFFFFFFFh (indicating the protection information shall not be checked).

Using the Error Recovery feature (refer to section 5.21.1.5), host software may enable an error to be returned if a deallocated or unwritten logical block is read. If this error is supported for the namespace and enabled, then a Read, Verify, or Compare command that includes a deallocated or unwritten logical block shall abort with the Unwritten or Deallocated Logical Block status code. Note: Legacy software may not handle an error for this case.

Note: The operation of the Deallocate function is similar to the ATA DATA SET MANAGEMENT with Trim feature described in ACS-4 and SCSI UNMAP command described in SBC-3.

6.7.2 Command Completion

When the command is completed, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

Dataset Management command specific status values are defined in Figure 372.

Figure 372: Dataset Management – Command Specific Status Values

Value	Description
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
80h	**Conflicting Attributes:** The attributes specified in the command are conflicting.
82h	**Attempted Write to Read Only Range:** The controller may optionally report this status if a Deallocate is attempted for a read only range. The controller shall not return this status value if the read-only condition on the media is a result of a change in the write protection state of a namespace (refer to section 8.19).

6.8 Flush command

The Flush command is used to request that the contents of volatile write cache be made non-volatile.

If a volatile write cache is enabled (refer to section 5.21.1.6), then the Flush command shall commit data and metadata associated with the specified namespace(s) to non-volatile media. The flush applies to all commands for the specified namespace(s) completed by the controller prior to the submission of the Flush command. The controller may also flush additional data and/or metadata from any namespace.

If bits 2:1 are set to 11b in the VWC field (refer to Figure 251) and the specified NSID is FFFFFFFFh, then the Flush command applies to all namespaces attached to the controller processing the Flush command. If bits 2:1 are set to 10b in the VWC field and the specified NSID is FFFFFFFFh, then the controller fails the command with status code Invalid Namespace or Format. If bits 2:1 are cleared to 00b in the VWC field, then the controller behavior if the specified NSID is FFFFFFFFh is not indicated. Controllers compliant with versions 1.4 and later of this specification shall not set bits 2:1 in the VWC field to the value of 00b.

If a volatile write cache is not present or not enabled, then Flush commands:

- shall complete successfully and have no effect if a sanitize operation is not in progress; and
- may complete successfully and have no effect if a sanitize operation is in progress.

All command specific fields are reserved.

6.8.1 Command Completion

Upon completion of the Flush command, the controller posts a completion queue entry to the associated I/O Completion Queue.

6.9 Read command

The Read command reads data and metadata, if applicable, from the I/O controller for the LBAs indicated. The command may specify protection information to be checked as part of the read operation.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15 fields. If the command uses PRPs for the data transfer, then the Metadata Pointer, PRP Entry 1, and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the Metadata SGL Segment Pointer and SGL Entry 1 fields are used.

Figure 373: Read – Metadata Pointer

Bits	Description
63:00	**Metadata Pointer (MPTR):** This field contains the Metadata Pointer, if applicable. Refer to Figure 106 for the definition of this field.

Figure 374: Read – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies where data is transferred to. Refer to Figure 106 for the definition of this field.

Figure 375: Read – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field indicates the 64-bit address of the first logical block to be read as part of the operation. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63: 32.

Figure 376: Read – Command Dword 12

Bits	Description
31	**Limited Retry (LR):** If set to '1', the controller should apply limited retry efforts. If cleared to '0', the controller should apply all available error recovery means to return the data to the host.
30	**Force Unit Access (FUA):** If set to '1', then for data and metadata, if any, associated with logical blocks specified by the Read command, the controller shall: 1) commit that data and metadata, if any, to non-volatile media; and 2) return the data, and metadata, if any, that are read from non-volatile media. There is no implied ordering with other commands. If cleared to '0', then this bit has no effect.
29:26	**Protection Information Field (PRINFO):** Specifies the protection information action and check field, as defined in Figure 359.
25:16	Reserved
15:00	**Number of Logical Blocks (NLB):** This field indicates the number of logical blocks to be read. This is a 0's based value.

Figure 377: Read – Command Dword 13

Bits	Description
31:08	Reserved

Figure 377: Read – Command Dword 13

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>07:00</td><td>
Dataset Management (DSM): This field indicates attributes for the LBA(s) being read.
<table>
<tr><th>Bits</th><th>Attribute</th><th>Definition</th></tr>
<tr><td>07</td><td>Incompressible</td><td>If set to ‘1’, then data is not compressible for the logical blocks indicated. If cleared to ‘0’, then no information on compression is provided.</td></tr>
<tr><td>06</td><td>Sequential Request</td><td>If set to ‘1’, then this command is part of a sequential read that includes multiple Read commands. If cleared to ‘0’, then no information on sequential access is provided.</td></tr>
<tr><td>05:04</td><td>Access Latency</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>None. No latency information provided.</td></tr>
<tr><td>01b</td><td>Idle. Longer latency acceptable.</td></tr>
<tr><td>10b</td><td>Normal. Typical latency.</td></tr>
<tr><td>11b</td><td>Low. Smallest possible latency.</td></tr>
</table>
</td></tr>
<tr><td>03:00</td><td>Access Frequency</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>No frequency information provided.</td></tr>
<tr><td>1h</td><td>Typical number of reads and writes expected for this LBA range.</td></tr>
<tr><td>2h</td><td>Infrequent writes and infrequent reads to the LBA range indicated.</td></tr>
<tr><td>3h</td><td>Infrequent writes and frequent reads to the LBA range indicated.</td></tr>
<tr><td>4h</td><td>Frequent writes and infrequent reads to the LBA range indicated.</td></tr>
<tr><td>5h</td><td>Frequent writes and frequent reads to the LBA range indicated.</td></tr>
<tr><td>6h</td><td>One time read. E.g., command is due to virus scan, backup, file copy, or archive.</td></tr>
<tr><td>7h</td><td>Speculative read. The command is part of a prefetch operation.</td></tr>
<tr><td>8h</td><td>The LBA range is going to be overwritten in the near future.</td></tr>
<tr><td>9h to Fh</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>
</td></tr>
</table>

Figure 378: Read – Command Dword 14

Bits	Description
31:00	**Expected Initial Logical Block Reference Tag (EILBRT):** This field specifies the Initial Logical Block Reference Tag expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

Figure 379: Read – Command Dword 15

Bits	Description
31:16	**Expected Logical Block Application Tag Mask (ELBATM):** This field specifies the Application Tag Mask expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.
15:00	**Expected Logical Block Application Tag (ELBAT):** This field specifies the Application Tag expected value. . If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

6.9.1 Command Completion

When the command is completed with success or failure, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

Read command specific status values are defined in Figure 380.

Figure 380: Read – Command Specific Status Values

Value	Description
80h	**Conflicting Attributes:** The attributes specified in the command are conflicting.
81h	**Invalid Protection Information:** The Protection Information Field (PRINFO) (refer to Figure 376) settings specified in the command are invalid for the Protection Information with which the namespace was formatted (refer to the PI field in Figure 332 and the DPS field in Figure 249) or the EILBRT field is invalid (refer to section 8.3.1.5).

6.10 Reservation Acquire command

The Reservation Acquire command is used to acquire a reservation on a namespace, preempt a reservation held on a namespace, and abort a reservation held on a namespace.

The command uses Command Dword 10 and a Reservation Acquire data structure in memory. If the command uses PRPs for the data transfer, then PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Figure 381: Reservation Acquire – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the location of a data buffer where data is transferred from. Refer to Figure 106 for the definition of this field.

Figure 382: Reservation Acquire – Command Dword 10

Bits	Description
31:16	Reserved
15:08	**Reservation Type (RTYPE):** This field specifies the type of reservation to be created. The field is defined in Figure 384.
07:04	Reserved
03	**Ignore Existing Key (IEKEY):** If this bit is set to a '1', the controller shall return an error of Invalid Field In Command. If this bit is cleared to '0', then the Current Reservation Key is checked.
02:00	**Reservation Acquire Action (RACQA):** This field specifies the action that is performed by the command. **RACQA Value** / **Description** 000b – Acquire 001b – Preempt 010b – Preempt and Abort 011b to 111b – Reserved

Figure 383: Reservation Acquire Data Structure

Bytes	Description
07:00	**Current Reservation Key (CRKEY):** The field specifies the current reservation key associated with the host.

Figure 383: Reservation Acquire Data Structure

Bytes	Description
15:08	**Preempt Reservation Key (PRKEY):** If the Reservation Acquire Action is set to 001b (i.e., Preempt) or 010b (i.e., Preempt and Abort), then this field specifies the reservation key to be unregistered from the namespace. For all other Reservation Acquire Action values, this field is reserved.

Figure 384: Reservation Type Encoding

Value	Description
0h	Reserved
1h	Write Exclusive Reservation
2h	Exclusive Access Reservation
3h	Write Exclusive - Registrants Only Reservation
4h	Exclusive Access - Registrants Only Reservation
5h	Write Exclusive - All Registrants Reservation
6h	Exclusive Access - All Registrants Reservation
7h to FFh	Reserved

6.10.1 Command Completion

When the command is completed, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

6.11 Reservation Register command

The Reservation Register command is used to register, unregister, or replace a reservation key.

The command uses Command Dword 10 and a Reservation Register data structure in memory (refer to Figure 387). If the command uses PRPs for the data transfer, then PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Figure 385: Reservation Register – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the location of a data buffer where data is transferred from. Refer to Figure 106 for the definition of this field.

Figure 386: Reservation Register – Command Dword 10

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>31:30</td><td>Change Persist Through Power Loss State (CPTPL): This field allows the Persist Through Power Loss (PTPL) state associated with the namespace to be modified as a side effect of processing this command. If the Reservation Persistence Feature (refer to section 5.21.1.28) is saveable, then any change to the PTPL state as a result of processing this command shall be applied to both the current value and the saved value of that feature.

<table>
<tr><th>CPTPL Value</th><th>Description</th></tr>
<tr><td>00b</td><td>No change to PTPL state</td></tr>
<tr><td>01b</td><td>Reserved</td></tr>
<tr><td>10b</td><td>Set PTPL state to ‘0’. Reservations are released and registrants are cleared on a power on.</td></tr>
<tr><td>11b</td><td>Set PTPL state to ‘1’. Reservations and registrants persist across a power loss.</td></tr>
</table>
</td></tr>
<tr><td>29:04</td><td>Reserved</td></tr>
<tr><td>03</td><td>Ignore Existing Key (IEKEY): If this bit is set to a ‘1’, then Reservation Register Action (RREGA) field values that use the Current Reservation Key (CRKEY) shall succeed regardless of the value of the Current Reservation Key field in the command (i.e., the current reservation key is not checked).</td></tr>
<tr><td>02:00</td><td>Reservation Register Action (RREGA): This field specifies the registration action that is performed by the command.

<table>
<tr><th>RREGA Value</th><th>Description</th></tr>
<tr><td>000b</td><td>Register Reservation Key</td></tr>
<tr><td>001b</td><td>Unregister Reservation Key</td></tr>
<tr><td>010b</td><td>Replace Reservation Key</td></tr>
<tr><td>011b to 111b</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

Figure 387: Reservation Register Data Structure

Bytes	Description
07:00	**Current Reservation Key (CRKEY):** If the Reservation Register Action is 001b (i.e., Unregister Reservation Key) or 010b (i.e., Replace Reservation Key), then this field contains the current reservation key associated with the host. For all other Reservation Register Action values, this field is reserved. The controller ignores the value of this field when the Ignore Existing Key (IEKEY) bit is set to ‘1’.
15:08	**New Reservation Key (NRKEY):** If the Reservation Register Action field is cleared to 000b (i.e., Register Reservation Key) or 010b (i.e., Replace Reservation Key), then this field contains the new reservation key associated with the host. For all other Reservation Register Action values, this field is reserved.

6.11.1 Command Completion

When the command is completed, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

6.12 Reservation Release command

The Reservation Release command is used to release or clear a reservation held on a namespace.

The command uses Command Dword 10 and a Reservation Release data structure in memory. If the command uses PRPs for the data transfer, then PRP Entry 1 and PRP Entry 2 fields are used. If the

command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Figure 388: Reservation Release – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the location of a data buffer where data is transferred from. Refer to Figure 106 for the definition of this field.

Figure 389: Reservation Release – Command Dword 10

Bits	Description
31:16	Reserved
15:08	**Reservation Type (RTYPE):** If the Reservation Release Action field is cleared to 000b (i.e., Release), then this field specifies the type of reservation that is being released. The reservation type in this field shall match the current reservation type. If the reservation type in this field does not match the current reservation type, then the controller should return an error of Invalid Field In Command. This field is defined in Figure 384.
07:04	Reserved
03	**Ignore Existing Key (IEKEY):** If this bit is set to a '1', the controller shall return an error of Invalid Field in Command. If this bit is cleared to '0', then the Current Reservation Key is checked.
02:00	**Reservation Release Action (RRELA):** This field specifies the reservation action that is performed by the command. **Value** / **Description** 000b – Release 001b – Clear 010b to 111b – Reserved

Figure 390: Reservation Release Data Structure

Bytes	O/M	Description
7:0	M	**Current Reservation Key (CRKEY):** The field specifies the current reservation key associated with the host.

6.12.1 Command Completion

When the command is completed, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

6.13 Reservation Report command

The Reservation Report command returns a Reservation Status data structure to memory that describes the registration and reservation status of a namespace.

The size of the Reservation Status data structure is a function of the number of controllers in the NVM subsystem that are associated with hosts that are registrants of the namespace (i.e., there is a Registered Controller data structure and/or Registered Controller extended data structure for each such controller). The controller returns the data structure in Figure 394 if the host has selected a 64-bit Host Identifier and the data structure in Figure 395 if the host has selected a 128-bit Host Identifier (refer to section 5.21.1.26).

If a 64-bit Host Identifier has been specified and the Extended Data Structure bit is set to '1' in Command Dword 11, then the controller shall abort the command with the status code of Host Identifier Inconsistent Format. If a 128-bit Host Identifier has been specified and the Extended Data Structure bit is cleared to '0'

in Command Dword 11, then the controller shall abort the command with the status code of Host Identifier Inconsistent Format.

The command uses Command Dword 10 and Command Dword 11. If the command uses PRPs for the data transfer, then PRP Entry 1 and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the SGL Entry 1 field is used. All other command specific fields are reserved.

Figure 391: Reservation Report – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the location of a data buffer where data is transferred to. Refer to Figure 106 for the definition of this field.

Figure 392: Reservation Report – Command Dword 10

Bits	Description
31:00	**Number of Dwords (NUMD):** This field specifies the number of dwords of the Reservation Status data structure to transfer. This is a 0's based value. If this field corresponds to a length that is less than the size of the Reservation Status data structure, then only that specified portion of the data structure is transferred. If this field corresponds to a length that is greater than the size of the Reservation Status data structure, then the entire contents of the data structure are transferred and no additional data is transferred.

Figure 393: Reservation Report – Command Dword 11

Bits	Description
31:01	Reserved
00	**Extended Data Structure (EDS):** If set to '1', then the controller returns the extended data structure defined in Figure 395. If cleared to '0', then the controller returns the data structure defined in Figure 394.

Figure 394: Reservation Status Data Structure

Bytes	Description
03:00	**Generation (GEN):** This field contains a 32-bit wrapping counter that is incremented any time any one the following occur: • a Reservation Register command completes successfully on any controller associated with the namespace; • a Reservation Release command with Reservation Release Action (RRELA) set to 001b (i.e., Clear) completes successfully on any controller associated with the namespace; and • a Reservation Acquire command with Reservation Acquire Action (RACQA) set to 001b (Preempt) or 010b (Preempt and Abort) completes successfully on any controller associated with the namespace. If the value of this field is FFFFFFFFh, then the field shall be cleared to 0h when incremented (i.e., rolls over to 0h).
04	**Reservation Type (RTYPE):** This field indicates whether a reservation is held on the namespace. A value of 0h indicates that no reservation is held on the namespace. A non-zero value indicates a reservation is held on the namespace and the reservation type is defined in Figure 384.
06:05	**Number of Registered Controllers (REGCTL):** This field indicates the number of controllers that are associated with hosts that are registrants of the namespace. This indicates the number of Registered Controller data structures and/or Registered Controller extended data structures contained in this data structure.
08:07	Reserved

Figure 394: Reservation Status Data Structure

Bytes	Description
09	**Persist Through Power Loss State (PTPLS):** This field indicates the Persist Through Power Loss State associated with the namespace. **PTPLS Value** / **Description** 0 – Reservations are released and registrants are cleared on a power on. 1 – Reservations and registrants persist across a power loss.
23:10	Reserved
47:24	**Registered Controller Data Structure 0**
	...
24*n+47: 24*(n+1)	**Registered Controller Data Structure n**

Figure 395: Reservation Status Extended Data Structure

Bytes	Description
23:00	Refer to Figure 394 for definition.
63:24	Reserved
127:64	**Registered Controller Extended Data Structure 0**
	...
64*(n+1)+63: 64*(n+1)	**Registered Controller Extended Data Structure n**

Figure 396: Registered Controller Data Structure

Bytes	Description
01:00	**Controller ID (CNTLID):** This field contains the controller ID (i.e., the value of the CNTLID field in the Identify Controller data structure) of the controller whose status is reported in this data structure. If the controller is a dynamic controller (refer to the NVMe over Fabrics specification) that is not associated with a host, then the Controller ID field shall be set to FFFFh.
02	**Reservation Status (RCSTS):** This field indicates the reservation status of the controller described by this data structure. Bits 7:1 are reserved Bit 0 is set to '1' if the controller is associated with a host that holds a reservation on the namespace.
07:03	Reserved
15:08	**Host Identifier (HOSTID):** This field contains the 64-bit Host Identifier of the controller described by this data structure.
23:16	**Reservation Key (RKEY):** This field contains the reservation key of the host associated with the controller described by this data structure.

Figure 397: Registered Controller Extended Data Structure

Bytes	Description
01:00	**Controller ID (CNTLID):** Refer to Figure 396 for definition.
02	**Reservation Status (RCSTS):** Refer to Figure 396 for definition.
07:03	Reserved
15:08	**Reservation Key (RKEY):** Refer to Figure 396 for definition.

Figure 397: Registered Controller Extended Data Structure

Bytes	Description
31:16	**Host Identifier (HOSTID):** This field contains the 128-bit Host Identifier of the controller described by this data structure.
63:32	Reserved

6.13.1 Command Completion

When the command is completed, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

6.14 Verify command

The Verify command verifies integrity of stored information by reading data and metadata, if applicable, for the LBAs indicated without transferring any data or metadata to the host. A Verify operation consists of the controller actions (e.g., reading) that verify integrity of stored information during execution of a Verify command. The command may specify protection information to be checked as part of the Verify operation.

Verify operations may be implemented via integrity checks of stored data and metadata. Metadata integrity checks shall include protection information if the Verify command specifies checking of protection information and the namespace is formatted with protection information.

If reading the data and metadata, if applicable, would result in an error being returned, then an error shall be returned as a result of the Verify operation on that data and metadata, if applicable. In this situation, the error that results from integrity checks may differ from the error that would result from reading (e.g., there is no requirement that the Verify and Read commands return the same error). Setting the Limited Retry (LR) bit to ‘1’ shall have the same effect in both the Read and Verify commands.

All data that is read or has its integrity checked by a Verify operation shall be included in the value of the Data Units Read field in the SMART/Health Information log page, refer to 5.14.1.2.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 14, and Command Dword 15 fields.

Figure 398: Verify – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field indicates the 64-bit address of the first logical block of data to be verified as part of the operation. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63:32.

Figure 399: Verify – Command Dword 12

Bits	Description
31	**Limited Retry (LR):** If set to ‘1’, then the controller should apply limited retry efforts. If cleared to ‘0’, then the controller should apply all available error recovery means before completing the command with failure.
30	**Force Unit Access (FUA):** If set to ‘1’, then the controller shall flush any data and metadata specified by the Verify command from any volatile cache before performing the Verify operation and shall perform the Verify operation on data and metadata that have been committed to non-volatile media. There is no implied ordering with other commands. If cleared to ‘0’, then this bit has no effect.

Figure 399: Verify – Command Dword 12

Bits	Description
29:26	**Protection Information Field (PRINFO):** Specifies the protection information action and check field, as defined in Figure 359. The Protection Information Check (PRCHK) field in the PRINFO field specifies the protection information to be checked by the Verify operation. The Protection Information Action (PRACT) bit in the PRINFO field is cleared to '0' by the host. If the PRACT bit is not cleared to '0', then the controller shall abort the command with a status of Invalid Field in Command.
25:16	Reserved
15:00	**Number of Logical Blocks (NLB):** This field indicates the number of logical blocks to be verified. This is a 0's based value.

Figure 400: Verify – Command Dword 14

Bits	Description
31:00	**Expected Initial Logical Block Reference Tag (EILBRT):** This field specifies the Initial Logical Block Reference Tag expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

Figure 401: Verify – Command Dword 15

Bits	Description
31:16	**Expected Logical Block Application Tag Mask (ELBATM):** This field specifies the Application Tag Mask expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.
15:00	**Expected Logical Block Application Tag (ELBAT):** This field specifies the Application Tag expected value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

6.14.1 Command Completion

Upon completion of the Verify command, the controller posts a completion queue entry (CQE) to the associated I/O Completion Queue. The status code types and values that may be used in a CQE for the Verify command include the status code type and status code values for all Media and Data Integrity Errors for the NVM Command Set that are applicable to the Read command (e.g., Unrecovered Read Error). Refer to Figure 127 and to Figure 133.

Verify command specific status values are defined in Figure 402.

Figure 402: Verify – Command Specific Status Values

Value	Description
81h	**Invalid Protection Information:** The Protection Information Field (PRINFO) (refer to Figure 399) settings specified in the command are invalid for the Protection Information with which the namespace was formatted (refer to the PI field in Figure 332 and the DPS field in Figure 249) or the EILBRT field is invalid (refer to section 8.3.1.5).

6.15 Write command

The Write command writes data and metadata, if applicable, to the I/O controller for the logical blocks indicated. The host may also specify protection information to include as part of the operation.

The command uses Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 13, Command Dword 14, and Command Dword 15 fields. If the command uses PRPs for the data transfer, then the Metadata Pointer, PRP Entry 1, and PRP Entry 2 fields are used. If the command uses SGLs for the data transfer, then the Metadata SGL Segment Pointer and SGL Entry 1 fields are used.

Figure 403: Write – Metadata Pointer

Bits	Description
63:00	**Metadata Pointer (MPTR):** This field contains the Metadata Pointer, if applicable. Refer to Figure 106 for the definition of this field.

Figure 404: Write – Data Pointer

Bits	Description
127:00	**Data Pointer (DPTR):** This field specifies the location of a data buffer where data is transferred from. Refer to Figure 106 for the definition of this field.

Figure 405: Write – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field indicates the 64-bit address of the first logical block to be written as part of the operation. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63:32.

Figure 406: Write – Command Dword 12

Bits	Description
31	**Limited Retry (LR):** If set to '1', the controller should apply limited retry efforts. If cleared to '0', the controller should apply all available error recovery means to write the data to the NVM.
30	**Force Unit Access (FUA):** If set to '1', then for data and metadata, if any, associated with logical blocks specified by the Write command, the controller shall write that data and metadata, if any, to non-volatile media before indicating command completion. There is no implied ordering with other commands. If cleared to '0', then this bit has no effect.
29:26	**Protection Information Field (PRINFO):** Specifies the protection information action and check field, as defined in Figure 359.
25:24	Reserved
23:20	**Directive Type (DTYPE)**: Specifies the Directive Type associated with the Directive Specific field (refer to section 9.1).
19:16	Reserved
15:00	**Number of Logical Blocks (NLB):** This field indicates the number of logical blocks to be written. This is a 0's based value.

Figure 407: Write – Command Dword 13

Bits	Description
31:16	**Directive Specific (DSPEC)**: Specifies the Directive Specific value associated with the Directive Type field (refer to section 9.1).
15:08	Reserved

Figure 407: Write – Command Dword 13

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>07:00</td><td>
Dataset Management (DSM): This field indicates attributes for the LBA(s) being written.
<table>
<tr><th>Bits</th><th>Attribute</th><th>Definition</th></tr>
<tr><td>07</td><td>Incompressible</td><td>If set to ‘1’, then data is not compressible for the logical blocks indicated. If cleared to ‘0’, then no information on compression is provided.</td></tr>
<tr><td>06</td><td>Sequential Request</td><td>If set to ‘1’, then this command is part of a sequential write that includes multiple Write commands. If cleared to ‘0’, then no information on sequential access is provided.</td></tr>
<tr><td>05:04</td><td>Access Latency</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>00b</td><td>None. No latency information provided.</td></tr>
<tr><td>01b</td><td>Idle. Longer latency acceptable.</td></tr>
<tr><td>10b</td><td>Normal. Typical latency.</td></tr>
<tr><td>11b</td><td>Low. Smallest possible latency.</td></tr>
</table>
</td></tr>
<tr><td>03:00</td><td>Access Frequency</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0h</td><td>No frequency information provided.</td></tr>
<tr><td>1h</td><td>Typical number of reads and writes expected for this LBA range.</td></tr>
<tr><td>2h</td><td>Infrequent writes and infrequent reads to the LBA range indicated.</td></tr>
<tr><td>3h</td><td>Infrequent writes and frequent reads to the LBA range indicated.</td></tr>
<tr><td>4h</td><td>Frequent writes and infrequent reads to the LBA range indicated.</td></tr>
<tr><td>5h</td><td>Frequent writes and frequent reads to the LBA range indicated.</td></tr>
<tr><td>6h</td><td>One time write. E.g., command is due to virus scan, backup, file copy, or archive.</td></tr>
<tr><td>7h to Fh</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>
</td></tr>
</table>

Figure 408: Write – Command Dword 14

Bits	Description
31:00	**Initial Logical Block Reference Tag (ILBRT):** This field specifies the Initial Logical Block Reference Tag value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

Figure 409: Write – Command Dword 15

Bits	Description
31:16	**Logical Block Application Tag Mask (LBATM):** This field specifies the Application Tag Mask value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.
15:00	**Logical Block Application Tag (LBAT):** This field specifies the Application Tag value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

6.15.1 Command Completion

When the command is completed with success or failure, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

Write command specific errors are defined in Figure 410.

Figure 410: Write – Command Specific Status Values

Value	Description
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
80h	**Conflicting Attributes:** The attributes specified in the command are conflicting.
81h	**Invalid Protection Information:** The Protection Information Field (PRINFO) (refer to Figure 406) settings specified in the command are invalid for the Protection Information with which the namespace was formatted (refer to the PI field in Figure 332 and the DPS field in Figure 249) or the ILBRT field is invalid (refer to section 8.3.1.5).
82h	**Attempted Write to Read Only Range:** The LBA range specified contains read-only blocks. The controller shall not return this status value if the read-only condition on the media is a result of a change in the write protection state of a namespace (refer to section 8.19).

6.16 Write Uncorrectable command

The Write Uncorrectable command is used to mark a range of logical blocks as invalid. When the specified logical block(s) are read after this operation, a failure is returned with Unrecovered Read Error status. To clear the invalid logical block status, a write operation is performed on those logical blocks.

The fields used are Command Dword 10, Command Dword 11, and Command Dword 12 fields. All other command specific fields are reserved.

Figure 411: Write Uncorrectable – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field specifies the 64-bit address of the first logical block to become uncorrectable as part of the operation. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63: 32.

Figure 412: Write Uncorrectable – Command Dword 12

Bits	Description
31:16	Reserved
15:00	**Number of Logical Blocks (NLB):** This field specifies the number of logical blocks to become uncorrectable. This is a 0's based value.

6.16.1 Command Completion

If the command is completed, then the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

Figure 413: Write Uncorrectable – Command Specific Status Values

Bit	Description
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
82h	**Attempted Write to Read Only Range:** The LBA range specified contains read-only blocks. The controller shall not return this status value if the read-only condition on the media is a result of a change in the write protection state of a namespace (refer to section 8.19).

6.17 Write Zeroes command

The Write Zeroes command is used to set a range of logical blocks to zero. Non-PI related metadata for this command, if any, shall be all bytes cleared to 0h. The protection information for logical blocks written to the media is updated based on CDW12.PRINFO. If the Protection Information Action bit (PRACT) is cleared to '0', then the protection information for this command shall be all zeroes. If the Protection Information Action bit (PRACT) is set to '1', then the protection information shall be based on the End-to-end Data Protection Type Settings (DPS) field in the Identify Namespace data structure (refer to Figure 249) and the CDW14.ILBRT, CDW15. LBATM, and CDW15. LBAT fields in the Write Zeroes command.

After successful completion of this command, the value returned by subsequent reads of logical blocks in this range shall be all bytes cleared to 0h until a write occurs to this LBA range.

If the Deallocate bit (CDW12.DEAC) is set to '1' in a Write Zeroes command, and the namespace supports clearing all bytes to 0h in the values read (e.g., bits 2:0 in the DLFEAT field are set to 001b) from a deallocated logical block and its metadata (excluding protection information), then for each specified logical block, the controller:

- should deallocate that logical block;
- shall return all bytes cleared to 0h in the values read from:
  - that logical block; and
  - that logical blocks metadata (excluding protection information);

  and
- shall return the protection information in that logical block as specified in section 6.7.1.1.

If the Deallocate bit is cleared to '0' in a Write Zeroes command, and the namespace supports clearing all bytes to 0h in the values read (e.g., bits 2:0 in the DLFEAT field are set to 001b) from a deallocated logical block and its metadata (excluding protection information), then, for each specified logical block, the controller:

- may deallocate that logical block;
- shall return all bytes cleared to 0h in the values read from:
  - that logical block; and
  - that logical blocks metadata (excluding protection information);

  and
- shall return the protection information in that logical block based on CDW12.PRINFO in that Write Zeroes command.

For each logical block in the range specified by a Write Zeroes command, if the namespace does not support that logical block clearing all bytes to 0h in the values read from that logical block and its metadata (excluding the protection information) read, then the controller shall not deallocate that logical block.

The fields used are Command Dword 10, Command Dword 11, Command Dword 12, Command Dword 14, and Command Dword 15 fields.

Figure 414: Write Zeroes – Command Dword 10 and Command Dword 11

Bits	Description
63:00	**Starting LBA (SLBA):** This field indicates the 64-bit address of the first logical block to be written as part of the operation. Command Dword 10 contains bits 31:00; Command Dword 11 contains bits 63:32.

Figure 415: Write Zeroes – Command Dword 12

Bits	Description
31	**Limited Retry (LR):** If set to '1', the controller should apply limited retry efforts. If cleared to '0', the controller should apply all available error recovery means to write the data to the NVM.

Figure 415: Write Zeroes – Command Dword 12

Bits	Description
30	**Force Unit Access (FUA):** If set to '1', then the controller shall write the data, and metadata, if any, to non-volatile media before indicating command completion. There is no implied ordering with other commands. If cleared to '0', then this bit has no effect.
29:26	**Protection Information Field (PRINFO):** Specifies the protection information action and check field, as defined in Figure 359. The Protection Information Check (PRCHK) field shall be cleared to 000b.
25	**Deallocate (DEAC):** If set to '1', then the host is requesting that the controller deallocate the specified logical blocks. If cleared to '0', then the host is not requesting that the controller deallocate the specified logical blocks.
24:16	Reserved
15:00	**Number of Logical Blocks (NLB):** This field indicates the number of logical blocks to be written. This is a 0's based value.

Figure 416: Write Zeroes – Command Dword 14

Bits	Description
31:00	**Initial Logical Block Reference Tag (ILBRT):** This field indicates the Initial Logical Block Reference Tag value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

Figure 417: Write Zeroes – Command Dword 15

Bits	Description
31:16	**Logical Block Application Tag Mask (LBATM):** This field indicates the Application Tag Mask value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.
15:00	**Logical Block Application Tag (LBAT):** This field indicates the Application Tag value. If the namespace is not formatted to use end-to-end protection information, then this field is ignored. Refer to section 8.3.

6.17.1 Command Completion

Upon completion of the Write Zeroes command, the controller shall post a completion queue entry to the associated I/O Completion Queue indicating the status for the command.

Write Zeroes command specific status values are defined in Figure 418.

Figure 418: Write Zeroes – Command Specific Status Values

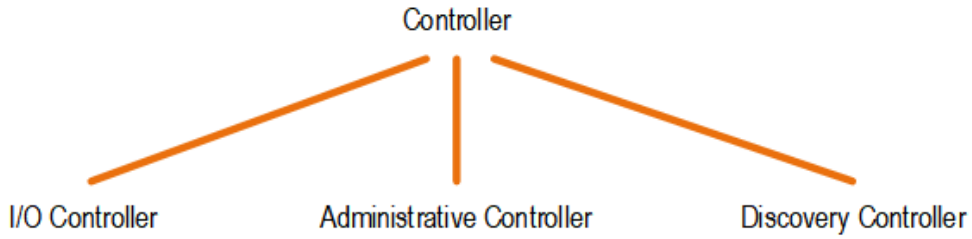
Value	Description
20h	**Namespace is Write Protected:** The command is prohibited while the namespace is write protected (refer to section 8.19).
81h	**Invalid Protection Information:** The Protection Information Field (PRINFO) (refer to Figure 415) settings specified in the command are invalid for the Protection Information with which the namespace was formatted (refer to the PI field in Figure 332 and the DPS field in Figure 249) or the ILBRT field is invalid (refer to section 8.3.1.5).
82h	**Attempted Write to Read Only Range:** The LBA range specified contains read-only blocks. The controller shall not return this status value if the read-only condition on the media is a result of a change in the write protection state of a namespace (refer to section 8.19).

7 Controller Architecture

7.1 Introduction

A controller is the interface between a host and an NVM subsystem. As shown in Figure 419, there are three types of controllers. An I/O controller is a general-purpose controller that supports commands that provide access to logical block data and metadata stored on an NVM subsystem's non-volatile storage medium and may support commands that provide management capabilities. An administrative controller is a controller that should support commands that provide management capabilities, but does not support commands that provide access to logical block data and metadata stored on an NVM subsystem's non-volatile storage medium. Finally, a discovery controller is a special type of controller used in NVMe over Fabrics to provide access to a Discovery Log Page.

Figure 419: Controller Types



The Controller Type (CNTRLTYPE) field in the Identify Controller data structure indicates a controller's type. Regardless of controller type, all controllers implement one Admin Submission Queue and one Admin Completion Queue. Depending on the controller type, a controller may also support one or more I/O Submission Queues and I/O Completion Queues.

Host software submits commands to a controller through pre-allocated Submission Queues. A controller is alerted to newly submitted commands through SQ Tail Doorbell register writes. The difference between the previous doorbell register value and the current register write indicates the number of commands that were submitted.

A controller fetches commands from the Submission Queue(s) and processes them. Except for fused operations, there are no ordering restrictions for processing of commands within or across Submission Queues. Host software should not submit commands to a Submission Queue that may not be re-ordered arbitrarily. Data associated with the processing of a command may or may not be committed to the NVM subsystem non-volatile memory storage medium in the order that commands are submitted.

Host software submits commands of higher priorities to the appropriate Submission Queues. Priority is associated with the Submission Queue itself, thus the priority of the command is based on the Submission Queue to which that command was submitted. The controller arbitrates across the Submission Queues based on fairness and priority according to the arbitration scheme specified in section 4.13.

Upon completion of the command execution by the NVM subsystem, the controller presents completion queue entries to the host through the appropriate Completion Queues. If MSI-X or multiple message MSI is in use, then the interrupt vector indicates the Completion Queue(s) with possible new command completions for the host to process. If pin-based interrupts or single message MSI interrupts are used, host software interrogates the Completion Queue(s) for new completion queue entries. The host updates the CQ Head doorbell register to release Completion Queue entries to the controller and to clear the associated interrupt.

There are no ordering restrictions for completions to the host. Each completion queue entry identifies the Submission Queue Identifier and Command Identifier of the associated command. Host software uses this information to correlate the completions with the commands submitted to the Submission Queue(s).

Host software is responsible for creating I/O Submission Queues and I/O Completion Queues prior to using those queue pairs to submit commands to the controller. I/O Submission Queues and I/O Completion

Queues are created using the Create I/O Submission Queue command (refer to section 5.4) and the Create I/O Completion Queue command (refer to section 5.3).

7.1.1 I/O Controller

An I/O controller is a general purpose controller that supports commands that provide access to an NVM subsystem's non-volatile storage medium and may support commands that provide management capabilities.

Figure 420 shows an NVM subsystem with three I/O controllers. I/O controller one has two attached namespaces, private namespace A and shared namespace B. I/O controller two also has two attached namespaces, private namespace C and shared namespace B. I/O controller three has no attached namespaces. At some later point in time shared namespace B may be attached to I/O controller three.

Figure 420: NVM Subsystem with Three I/O Controllers

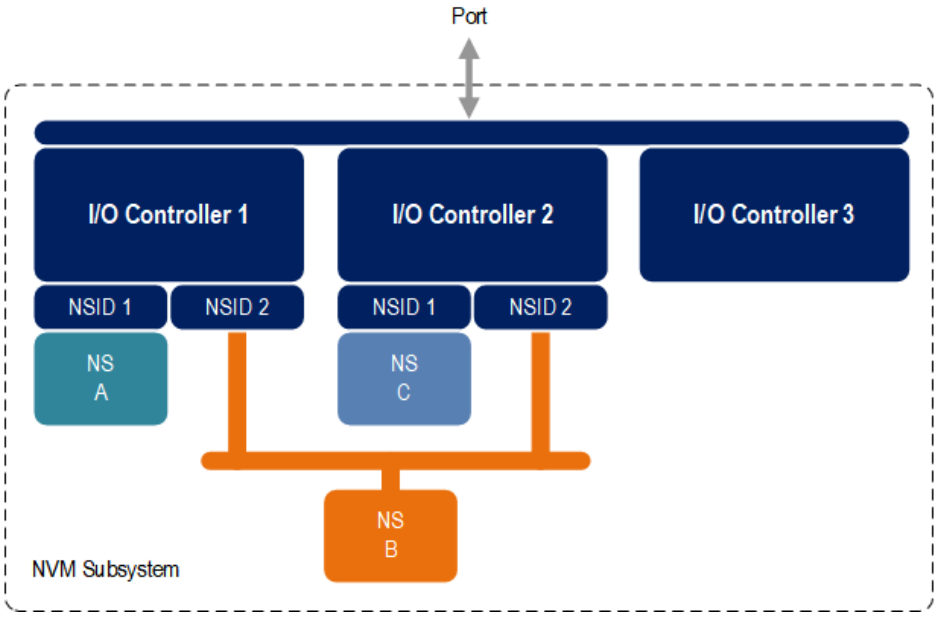


Figure 421 to Figure 422 define commands that are mandatory, optional, and prohibited for an I/O controller.

Figure 421: I/O Controller – Admin Command Support

Command	Command Support Requirements [1]
Delete I/O Submission Queue	M
Create I/O Submission Queue	M
Get Log Page	M
Delete I/O Completion Queue	M
Create I/O Completion Queue	M
Identify	M
Abort	M
Set Features	M
Get Features	M
Asynchronous Event Request	M
Namespace Management	O
Firmware Commit	O
Firmware Image Download	O
Device Self-test	O

Figure 421: I/O Controller – Admin Command Support

Command	Command Support Requirements [1]
Namespace Attachment	O
Keep Alive	NOTE 2
Directive Send	O
Directive Receive	O
Virtualization Management	O
NVMe-MI Send	O
NVMe-MI Receive	O
Doorbell Buffer Config	O
NVMe over Fabrics Commands	Refer to the NVMe over Fabrics specification
I/O Command Set Specific Admin Command	O
Vendor Specific	O

Notes:
1. O = Optional, M = Mandatory, P = Prohibited
2. For NVMe over PCIe implementations, the Keep Alive command is optional. For NVMe over Fabrics implementations, the associated NVMe Transport binding defines whether the Keep Alive command is optional or mandatory.

Figure 422: I/O Controller – NVM Command Set Specific Admin Command Support

Command	Command Support Requirements [1]
Format NVM	O
Security Send	O
Security Receive	O
Sanitize	O
Get LBA Status	O

Notes:
1. O = Optional, M = Mandatory, P = Prohibited

Figure 423: I/O Controller – NVM Command Set Support

Command	Command Support Requirements [1]
Flush	M
Write	M
Read	M
Write Uncorrectable	O
Compare	O
Write Zeroes	O
Dataset Management	O
Verify	O
Reservation Register	O [2]
Reservation Report	O [2]
Reservation Acquire	O [2]
Reservation Release	O [2]
Vendor Specific	O

Notes:
1. O = Optional, M = Mandatory, P = Prohibited
2. Mandatory if reservations are supported as indicated in the Identify Controller data structure.

Figure 424 and Figure 425 define log pages that are mandatory, optional, and prohibited for an I/O controller.

Figure 424: I/O Controller – Log Page Support

Log Page Name	Command Support Requirements [1]
Error Information	M
SMART / Health Information (Controller scope)	M
SMART / Health Information (NVM subsystem scope)	O
Firmware Slot Information	M
Changed Namespace List	O
Commands Supported and Effects	O
Device Self-test	O
Telemetry Host-Initiated	O
Telemetry Controller-Initiated	O
Endurance Group Information	O
Predictable Latency Per NVM Set	O
Predictable Latency Event Aggregate	O
Asymmetric Namespace Access	O
Persistent Event	O
LBA Status Information	O
Endurance Group Event Aggregate	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited	

Figure 425: I/O Controller – NVM Command Set Specific Log Page Support

Log Page Name	Command Support Requirements [1]
Reservation Notification	O
Sanitize Status	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited	

Figure 426 and Figure 427 define features that are mandatory, optional, and prohibited for an I/O controller.

Figure 426: I/O Controller – Feature Support

Feature Name	Feature Support Requirements [1]	Logged in Persistent Event Log [1]
Arbitration	M	O
Power Management	M	NR
LBA Range Type	O	NR
Temperature Threshold	M	O
Error Recovery	M	O
Volatile Write Cache	O	O
Number of Queues	M	O
Interrupt Coalescing	NOTE 2	O
Interrupt Vector Configuration	NOTE 2	O
Write Atomicity Normal	M	O
Asynchronous Event Configuration	M	NR
Autonomous Power State Transition	O	O
Host Memory Buffer	O	O
Timestamp	O	P
Keep Alive Timer	O	O
Host Controlled Thermal Management	O	O

Figure 426: I/O Controller – Feature Support

Feature Name	Feature Support Requirements [1]	Logged in Persistent Event Log [1]
Non-Operational Power State Config	O	O
Read Recovery Level Config	O	O
Predictable Latency Mode Config	O	O
Predictable Latency Mode Window	O	P
LBA Status Information Attributes	O	O
Host Behavior Support	O	O
Sanitize Config	O	O
Endurance Group Event Configuration	O	O

Notes:
1. O = Optional, M = Mandatory, P = Prohibited, NR = Not Recommended
2. The feature is mandatory for NVMe over PCIe. This feature is not supported for NVMe over Fabrics.

Figure 427: I/O Controller – NVM Command Set Specific Feature Support

Feature Name	Feature Support Requirements [1]	Logged in Persistent Event Log [1]
Software Progress Marker	O	NR
Host Identifier	O [2]	O
Reservation Notification Mask	O [3]	O
Reservation Persistence	O [3]	O
Namespace Write Protection Config	O	O

Notes:
1. O = Optional, M = Mandatory, P = Prohibited, NR = Not Recommended
2. Mandatory if reservations are supported as indicated in the Identify Controller data structure.
3. Mandatory if reservations are supported by the namespace as indicated by a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure.

7.1.2 Administrative Controller

An administrative controller is a controller whose intended purpose is to provide NVM subsystem management capabilities. While an I/O controller may support these same management capabilities, an administrative controller has fewer mandatory capabilities. Unlike an I/O controller, an administrative controller does not support commands that provide access to logical block data and metadata stored on an NVM subsystem's non-volatile storage medium. This prevents a host managing an NVM subsystem using an administrative controller from accessing user data. Finally, an administrative controller has a dedicated PCI programming interface value (refer to CC.PI field) allowing a dedicated NVMe management driver to be loaded instead of a generic NVMe driver.

Examples of management capabilities that may be supported by an administrative controller include the following.

- Ability to efficiently poll NVM subsystem health status via NVMe-MI using the NVMe-MI Send and NVMe-MI Receive commands;
- Ability to manage an NVMe enclosure via NVMe-MI using the NVMe-MI Send and NVMe-MI Receive commands;
- Ability to manage NVM subsystem namespaces using the Namespace Attachment and Namespace commands;
- Ability to perform virtualization management using the Virtualization Management command; and
- Ability to reset an entire NVM subsystem using the NVM Subsystem Reset (NSSR) register.

Since an administrative controller does not provide access to logical block data and metadata stored on an NVM subsystem's non-volatile storage medium, the administrative controller shall not support I/O queues or namespaces attached to the administrative controller.

An administrative controller is required to support the mandatory Admin commands listed in Figure 430. An administrative controller may support one or more I/O Command Sets. When an Administrative controller supports an I/O Command Set, then only I/O Command Set Specific Admin commands may be supported since an Administrative controller only has an Admin Queue and no I/O Queues.

Figure 428 shows an NVM subsystem with one administrative controller and two I/O controllers within an NVM subsystem that contains a non-volatile storage medium and namespaces. I/O controller one has two attached namespaces, private namespace A and shared namespace B. I/O controller two also has two attached namespaces, private namespace C and shared namespace B. Since an administrative controller does not provide access to logical block data and metadata stored on an NVM subsystem's non-volatile storage medium, the administrative controller has no attached namespaces. The administrative controller in this example may be used for tasks such as NVM subsystem namespace management and efficiently polling NVM subsystem health status via NVMe-MI. While this example shows a single administrative controller, an NVM subsystem may support zero or more administrative controllers.

Figure 428: NVM Subsystem with One Administrative and Two I/O Controllers

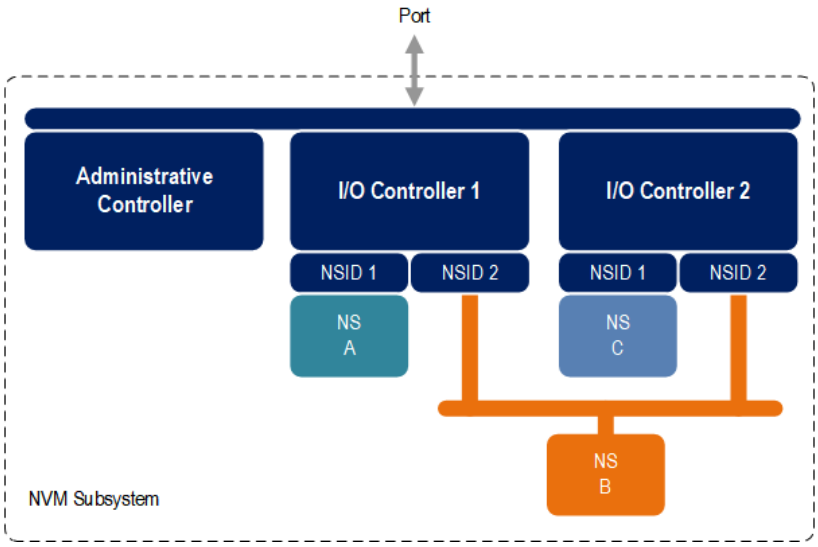


Figure 429 shows an NVM subsystem with one administrative controller within an NVM subsystem that contains no non-volatile storage medium or namespaces. The administrative controller in this example may be used to manage an NVMe enclosure using NVMe-MI. Since the administrative controller is used for a very specific dedicated purpose, the implementer of such an administrative controller may choose to implement only the mandatory capabilities along with the NVMe-MI Send and NVMe-MI Receive commands.

Figure 429: NVM Subsystem with One Administrative Controller

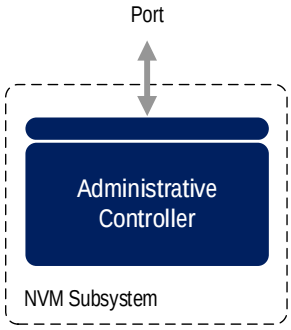


Figure 430 and Figure 431 define commands that are mandatory, optional, and prohibited for an administrative controller. Since an administrative controller does not support I/O queues, NVM Command Set commands that are not admin commands are not supported. A host may utilize the Commands Supported and Effects log page to determine optional commands that are supported by an Administrative controller.

Figure 430: Administrative Controller – Admin Command Support

Command	Command Support Requirements [1]
Delete I/O Submission Queue	P
Create I/O Submission Queue	P
Get Log Page	M
Delete I/O Completion Queue	P
Create I/O Completion Queue	P
Identify	M
Abort	O
Set Features	O [3]
Get Features	O [3]
Asynchronous Event Request	O [4]
Namespace Management	O
Firmware Commit	O
Firmware Image Download	O
Device Self-test	O
Namespace Attachment	O
Keep Alive	NOTE 2
Directive Send	O
Directive Receive	O
Virtualization Management	O
NVMe-MI Send	O
NVMe-MI Receive	O
Doorbell Buffer Config	O
NVMe over Fabrics Commands	Refer to the NVMe over Fabrics specification
I/O Command Set Specific Admin Command	O

Figure 430: Administrative Controller – Admin Command Support

Command	Command Support Requirements [1]
Vendor Specific	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited 2. For NVMe over PCIe implementations, the Keep Alive command is optional. For NVMe over Fabrics implementations, the associated NVMe Transport binding defines whether the Keep Alive command is optional or mandatory. 3. Mandatory if any of the features in Figure 434 are implemented. 4. Mandatory if Telemetry Log, Firmware Commit, or SMART/Health Critical Warnings are supported.	

Figure 431: Administrative Controller – NVM Command Set Specific Admin Command Support

Command	Command Support Requirements [1]
Format NVM	O
Security Send	O
Security Receive	O
Sanitize	O
Get LBA Status	P
Notes: 1. O = Optional, M = Mandatory, P = Prohibited	

Figure 432 and Figure 433 defines log pages that are mandatory, optional, and prohibited for an administrative controller.

Figure 432: Administrative Controller – Log Page Support

Log Page Name	Command Support Requirements [1]
Error Information	M
SMART / Health Information (Controller scope)	O
SMART / Health Information (NVM subsystem scope)	O
Firmware Slot Information	O
Changed Namespace List	O
Commands Supported and Effects	M
Device Self-test	O
Telemetry Host-Initiated	O
Endurance Group Information	O
Predictable Latency Per NVM Set	O
Predictable Latency Event Aggregate	O
Asymmetric Namespace Access	P
Persistent Event	O
LBA Status Information	P
Endurance Group Event Aggregate	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited	

Figure 433: Administrative Controller – NVM Command Set Specific Log Page Support

Log Page Name	Command Support Requirements [1]
Reservation Notification	P

Figure 433: Administrative Controller – NVM Command Set Specific Log Page Support

Log Page Name	Command Support Requirements [1]
Sanitize Status	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited	

Figure 434 and Figure 435 defines features that are mandatory, optional, and prohibited for an administrative controller. If any feature is supported, then the Set Features and Get Features commands shall be supported.

Figure 434: Administrative Controller – Feature Support

Feature Name	Feature Support Requirements [1]	Logged in Persistent Event Log [1]
Arbitration	P	P
Power Management	O	NR
LBA Range Type	P	P
Temperature Threshold	O	O
Error Recovery	P	P
Volatile Write Cache	P	P
Number of Queues	P	P
Interrupt Coalescing	NOTE 2	NOTE 2
Interrupt Vector Configuration	NOTE 2	NOTE 2
Write Atomicity Normal	P	P
Asynchronous Event Configuration	O [3]	NR
Autonomous Power State Transition	O	O
Host Memory Buffer	O	O
Timestamp	O	P
Keep Alive Timer	O	O
Host Controlled Thermal Management	O	O
Non-Operational Power State Config	O	O
Read Recovery Level Config	O	O
Predictable Latency Mode Config	O	P
Predictable Latency Mode Window	O	O
LBA Status Information Attributes	P	O
Host Behavior Support	O	O
Sanitize Config	O	O
Endurance Group Event Configuration	O	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited, NR = Not Recommended 2. The feature is optional for NVMe over PCIe. This feature is not supported for NVMe over Fabrics. Mandatory if Telemetry Log, Firmware Commit or SMART/Health Critical Warnings are supported.		

Figure 435: Administrative Controller – NVM Command Set Specific Feature Support

Feature Name	Feature Support Requirements [1]	Logged in Persistent Event Log [1]
Software Progress Marker	O	NR
Host Identifier	O [2]	O
Reservation Notification Mask	O [3]	O
Reservation Persistence	O [3]	O

Figure 435: Administrative Controller – NVM Command Set Specific Feature Support

Feature Name	Feature Support Requirements [1]	Logged in Persistent Event Log [1]
Namespace Write Protection Config	O	O
Notes: 1. O = Optional, M = Mandatory, P = Prohibited, NR = Not Recommended 2. Mandatory if reservations are supported as indicated in the Identify Controller data structure. Mandatory if reservations are supported by the namespace as indicated by a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure.		

7.1.3 Discovery Controller

A discovery controller is a special type of controller used in NVMe over Fabrics to provide access to a Discovery Log Page. Refer to the NVMe over Fabrics specification for more information.

7.2 Command Submission and Completion Mechanism (Informative)

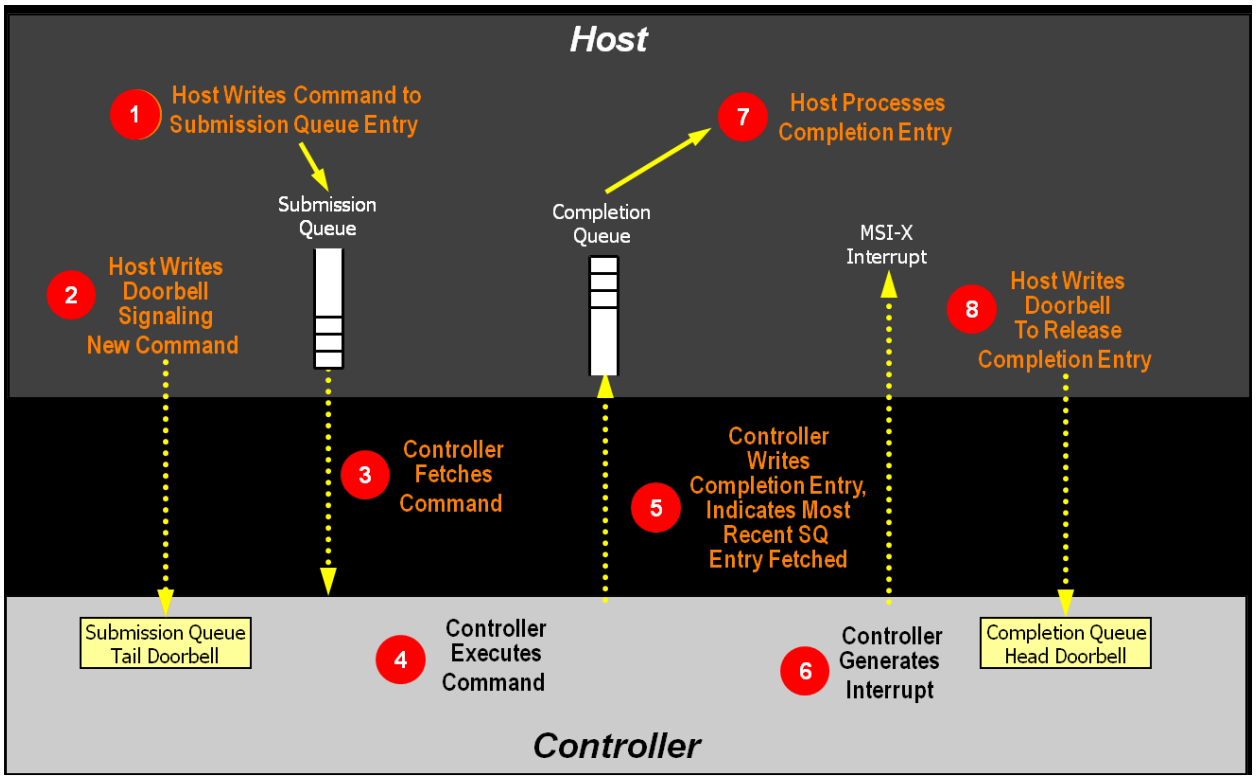
This section describes the command issue and completion mechanism. It also describes how commands are built by host software and command completion processing.

7.2.1 Command Processing

This section describes command submission and completion processing. Figure 436 shows the steps that are followed to submit and complete a command. The steps are:

1. The host places one or more commands for execution in the next free Submission Queue slot(s) in memory;
2. The host updates the Submission Queue Tail Doorbell register with the new value of the Submission Queue Tail entry pointer. This indicates to the controller that a new command(s) is submitted for processing;
3. The controller transfers the command(s) from in the Submission Queue slot(s) into the controller for future execution. Arbitration is the method used to determine the Submission Queue from which the controller starts processing the next candidate command(s), refer to section 4.13;
4. The controller then proceeds with execution of the next command(s). Commands may complete out of order (the order submitted or started execution);
5. After a command has completed execution, the controller places a completion queue entry in the next free slot in the associated Completion Queue. As part of the completion queue entry, the controller indicates the most recent Submission Queue entry that has been consumed by advancing the Submission Queue Head pointer in the completion entry. Each new completion queue entry has a Phase Tag inverted from the previous entry to indicate to the host that this completion queue entry is a new entry;
6. The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
7. The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
8. The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

Figure 436: Command Processing



7.2.2 Basic Steps when Building a Command

When host software builds a command for the controller to execute, it first checks to make sure that the appropriate Submission Queue (SQx) is not full. The Submission Queue is full when the number of entries in the queue is one less than the queue size. Once an empty slot (pFreeSlot) is available:

1. Host software builds a command at SQx[pFreeSlot] with:
   a. CDW0.OPC is set to the appropriate command to be executed by the controller;
   b. CDW0.FUSE is set to the appropriate value, depending on whether the command is a fused operation;
   c. CDW0.CID is set to a unique identifier for the command when combined with the Submission Queue identifier;
   d. The Namespace Identifier, NSID field, is set to the namespace the command applies to;
   e. MPTR shall be filled in with the offset to the beginning of the Metadata Region, if there is a data transfer and the namespace format contains metadata as a separate buffer;
   f. PRP1 and/or PRP2 (or SGL Entry 1 if SGLs are used) are set to the source/destination of data transfer, if there is a data transfer; and
   g. CDW10 – CDW15 are set to any command specific information;
   and
2. Host software writes the corresponding Submission Queue doorbell register (SQxTDBL) to submit one or more commands for processing.

The write to the Submission Queue doorbell register triggers the controller to consume one or more new commands contained in the Submission Queue entry. The controller indicates the most recent SQ entry that has been consumed as part of reporting completions. Host software may use this information to determine when SQ slots may be re-used for new commands.

7.2.3 Processing Completed Commands

Host software processes the interrupt generated by the controller for command completion(s). If MSI-X or multiple message MSI is in use, then the interrupt vector implies the Completion Queue(s) with new command completions for the host to process. If pin-based interrupts or single message MSI interrupts are used, then host software interrogates the Completion Queue(s) to determine if new completion queue entries are present for the host to process.

Once the host software determines the Completion Queue (CQy) that generated the interrupt:

1. Host software reads a completion queue entry from the specified Completion Queue;
2. Host software processes the CQ entry to identify the Submission Queue entry that generated this completion. DW2.SQID indicates the Submission Queue ID and DW3.CID indicates the command that generated the completion;
3. DW3.SF indicates the status of the completion;
4. Host software indicates available Completion Queue slots by updating the corresponding Completion Queue Head Doorbell register (CQyHDBL). By updating CQyHDBL, the associated interrupt is cleared; and
5. If there were errors, noted in the DW3.SF field, host software performs error recovery actions (refer to section 10.1).

7.2.4 Command Related Resource Retirement

As part of reporting completions, the controller indicates the most recent Submission Queue entry that has been consumed. Submission Queue slots containing consumed Submission Queue entries are free and may be re-used by host software to submit new commands.

If a completion queue entry is posted for a command, then host software may re-use the associated PRP List(s) for that command and other resources (an exception is the PRP List for I/O Submission Queues and I/O Completion Queues).

7.2.5 Command Examples

7.2.5.1 Creating an I/O Submission Queue

This example describes how host software creates an I/O Submission Queue that utilizes non-contiguous PRP entries. Creating an I/O Submission Queue that utilizes a PRP List is only valid if the controller supports non-contiguous queues as indicated in CAP.CQR.

Prior to creating an I/O Submission Queue, host software shall create the I/O Completion Queue that the SQ uses with the Create I/O Completion Queue command.

To create an I/O Submission Queue, host software builds a Create I/O Submission Queue command for the Admin Submission Queue. Host software builds the Create I/O Submission Queue command in the next free Admin Submission Queue command location. The attributes of the command are:

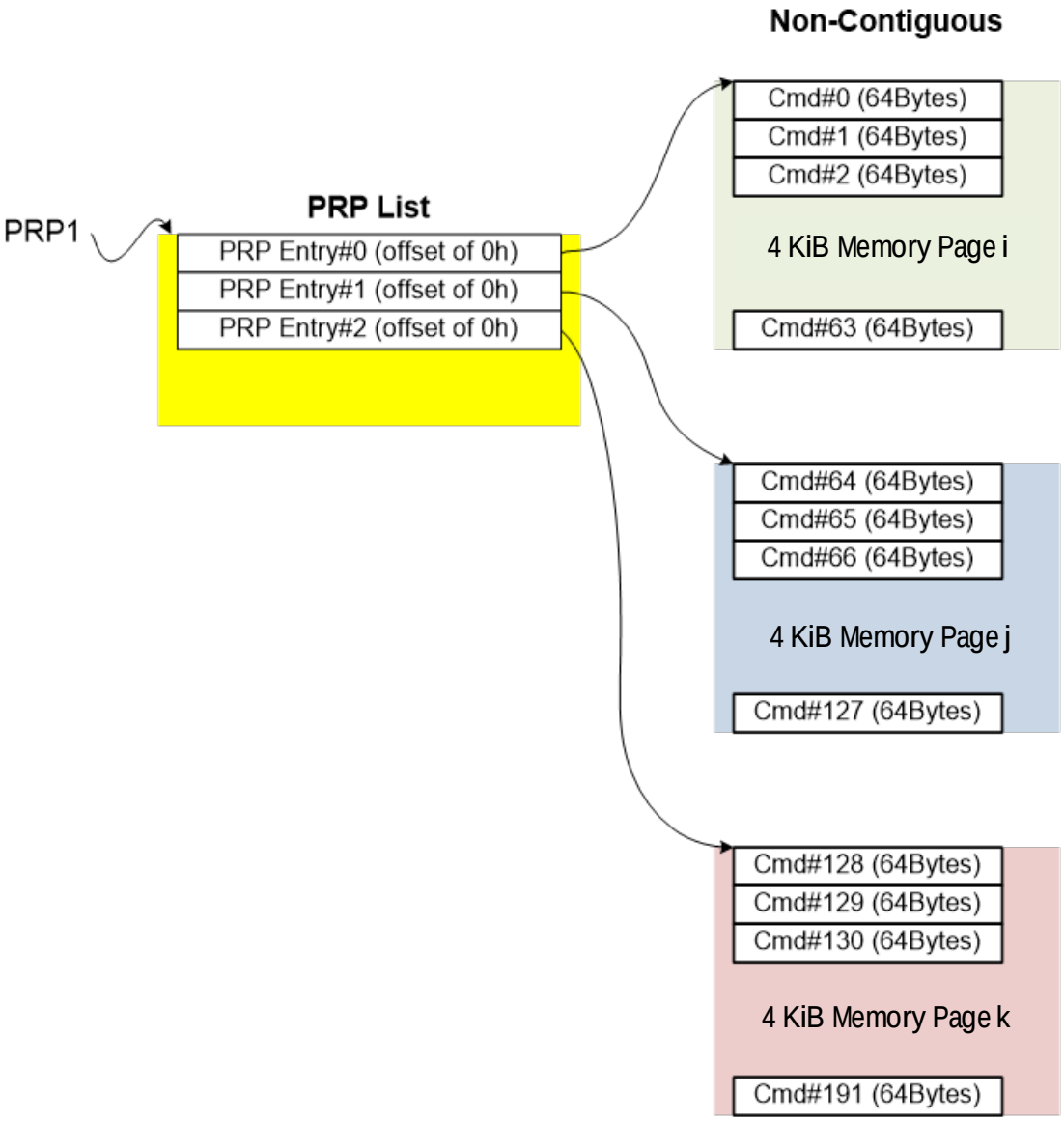
- CDW0.OPC is set to 01h;
- CDW0.FUSE is cleared to 00b indicating that this is not a fused operation;
- CDW0.CID is set to a free command identifier;
- The NSID field is cleared to 0h; Submission Queues are not specific to a namespace;
- MPTR is cleared to 0h; metadata is not used for this command;
- PRP1 is set to the physical address of the PRP List. The PRP List is shown in Figure 437 for a PRP List with three entries;
- PRP2 is cleared to 0h; PRP Entry 2 is not used for this command;
- CDW10.QSIZE is set to the size of queue to create. In this case, the value is set to 191, indicating a queue size of 192 entries. The queue size shall not exceed the maximum queue entries supported, indicated in the CAP.MQES field;

- CDW10.QID is set to the Submission Queue identifier;
- CDW11.CQID is set to the I/O Completion Queue identifier where command completions are posted;
- CDW11.QPRIO is set to 10b, indicating a Medium priority queue; and
- CDW11.PC is cleared to ‘0’ indicating that the data buffer indicated by PRP1 is not physically contiguously.

After the command is built, host software submits the command for execution by writing the Admin Submission Queue doorbell (SQ0TDBL) to indicate to the controller that this command is available for processing.

Host software shall maintain the PRP List unmodified in host memory until the Submission Queue is deleted.

Figure 437: PRP List Describing I/O Submission Queue



7.2.5.2 Executing a Fused Operation

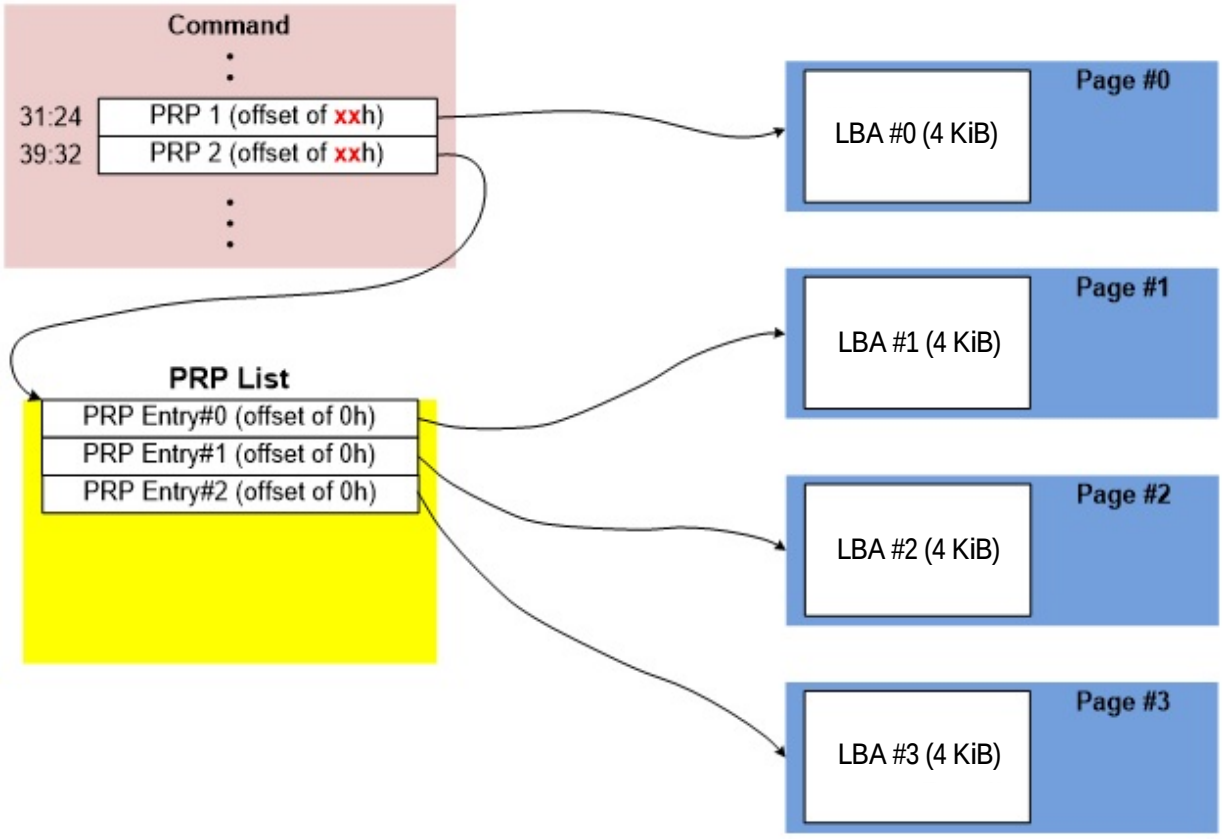
This example describes how host software creates and executes a fused command, specifically Compare and Write for a total of 16 KiB of data. In this case, there are two commands that are created. The first command is the Compare, referred to as CMD0. The second command is the Write, referred to as CMD1. In this case, end-to-end data protection is not enabled and the size of each logical block is 4 KiB.

To build commands for a fused operation, host software utilizes the next two available adjacent command locations in the appropriate I/O Submission Queue.

The attributes of the Compare command are:

- CMD0.CDW0.OPC is set to 05h for Compare;
- CMD0.CDW0.FUSE is set to 01b indicating that this is the first command of a fused operation;
- CMD0.CDW0.CID is set to a free command identifier;
- CMD0.NSID is set to identify the appropriate namespace;
- If metadata is being used in a separate buffer, then the location of that buffer is specified in the CMD0.MPTR field;
- The physical address of the first page of the data to compare:
  - If PRPs are used, CMD0.PRP1 is set to the physical address of the first page of the data to compare and CMD0.PRP2 is set to the physical address of the PRP List. The PRP List is shown in Figure 438 for a PRP List with three entries; or
  - If the command uses SGLs, CMD0.SGL1 is set to an appropriate SGL segment descriptor depending on whether more than one descriptor is needed;
- CMD0.CDW10.SLBA is set to the first LBA to compare against. Note that this field also spans Command Dword 11;
- CMD0.CDW12.LR is cleared to ‘0’ to indicate that the controller should apply all available error recovery means to retrieve the data for comparison;
- CMD0.CDW12.FUA is cleared to ‘0’, indicating that the data may be read from any location, including a volatile cache, in the NVM subsystem;
- CMD0.CDW12.PRINFO is cleared to 0h since end-to-end protection is not enabled;
- CMD0.CDW12.NLB is set to 3h, indicating that four logical blocks of a size of 4 KiB each are to be compared against;
- CMD0.CDW14 is cleared to 0h since end-to-end protection is not enabled; and
- CMD0.CDW15 is cleared to 0h since end-to-end protection is not enabled.

Figure 438: PRP List Describing Data to Compare



The attributes of the Write command are:

- CMD1.CDW0.OPC is set to 01h for Write;
- CMD1.CDW0.FUSE is set to 10b indicating that this is the second command of a fused operation;
- CMD1.CDW0.CID is set to a free command identifier;
- CMD1.NSID is set to identify the appropriate namespace. This value shall be the same as CMD0.NSID;
- If metadata is being used in a separate buffer, then the location of that buffer is specified in the CMD1.MPTR field;
- The physical address of the first page of data to write is identified:
  - If the command uses PRPs, then CMD1.PRP1 is set to the physical address of the first page of the data to write and CMD1.PRP2 is set to the physical address of the PRP List. The PRP List includes three entries; or
  - If the command uses SGLs, CMD1.SGL1 is set to an appropriate SGL segment descriptor depending on whether more than one descriptor is needed;
- CMD1.CDW10.SLBA is set to the first LBA to compare against. Note that this field also spans Command Dword 11. This value shall be the same as CMD0.CDW10.SLBA;
- CMD1.CDW12.LR is cleared to ‘0’ to indicate that the controller should apply all available error recovery means to write the data to the NVM;
- CMD1.CDW12.FUA is cleared to ‘0’, indicating that the data may be written to any location, including a volatile cache, in the NVM subsystem;
- CMD1.CDW12.PRINFO is cleared to 0h since end-to-end protection is not enabled;
- CMD1.CDW12.NLB is set to 3h, indicating that four logical blocks of a size of 4 KiB each are to be compared against. This value shall be the same as CMD0.CDW12.NLB;

- CMD1.CDW14 is cleared to 0h since end-to-end protection is not enabled; and
- CMD1.CDW15 is cleared to 0h since end-to-end protection is not enabled.

After the commands are built, host software submits the commands for execution by writing the appropriate I/O Submission Queue doorbell (SQxTDBL) to indicate to the controller that these commands are submitted. Note that the doorbell write shall indicate both commands have been submitted at one time.

7.3 Resets

7.3.1 NVM Subsystem Reset

An NVM Subsystem Reset is initiated when:

- Main power is applied to the NVM subsystem;
- A value of 4E564D65h (“NVMe”) is written to the NSSR.NSSRC field;
- Requested using a method defined in the NVMe Management Interface specification; or
- A vendor specific event occurs.

When an NVM Subsystem Reset occurs, the entire NVM subsystem is reset. This includes the initiation of a Controller Level Reset on all controllers that make up the NVM subsystem, disabling of the Persistent Memory Region associated with all controllers that make up the NVM subsystem, and a transition to the Detect LTSSM state by all PCI Express ports of the NVM subsystem.

The occurrence of an NVM Subsystem Reset while power is applied to the NVM subsystem is reported by the initial value of the CSTS.NSSRO field following the NVM Subsystem Reset. This field may be used by host software to determine if the sudden loss of communication with a controller was due to an NVM Subsystem Reset or some other condition.

The ability for host software to initiate an NVM Subsystem Reset by writing to the NSSR.NSSRC field is an optional capability of a controller indicated by the state of the CAP.NSSRS field. An implementation may protect the NVM subsystem from an inadvertent NVM Subsystem Reset by not providing this capability to one or more controllers that make up the NVM subsystem.

The occurrence of a vendor specific event that results in an NVM Subsystem Reset is intended to allow implementations to recover from a severe NVM subsystem internal error that prevents continued normal operation (e.g., fatal hardware or firmware error).

7.3.2 Controller Level Reset

The following methods initiate a Controller Level Reset:

- NVM Subsystem Reset;
- Conventional Reset (refer to the PCI Express Base Specification);
- Function Level Reset (refer to the PCI Express Base Specification); and
- Controller Reset (i.e., CC.EN transitions from ‘1’ to ‘0’).

A Controller Level Reset consists of the following actions:

- The controller stops processing any outstanding Admin or I/O commands;
- All I/O Submission Queues are deleted;
- All I/O Completion Queues are deleted;
- The controller is brought to an Idle state. When this is complete, CSTS.RDY is cleared to ‘0’; and
- All controller registers defined in section 3 and internal controller state are reset, except as follows:
  - the Admin Queue registers (AQA, ASQ, or ACQ) are not reset as part of a Controller Reset;
  - the Controller Memory Buffer Memory Space Control register (CMBMSC) is reset as part of neither a Controller Reset nor a Function Level Reset; and

- the Persistent Memory Region Memory Space Control Upper register (PMRMSCU) and the Persistent Memory Region Memory Space Control Lower register (PMRMSCL) are not reset as part of a Controller Reset.

In all Controller Level Reset cases except a Controller Reset, the PCI register space is reset as defined by the PCI Express Base specification. Refer to the PCI Express specification for further details.

To continue after a Controller Level Reset, the host shall:

- Update register state as appropriate;
- Set CC.EN to '1';
- Wait for CSTS.RDY to be set to '1';
- Configure the controller using Admin commands as needed;
- Create I/O Completion Queues and I/O Submission Queues as needed; and
- Proceed with normal I/O operations.

Note that all Controller Level Reset cases except a Controller Reset result in the controller immediately losing communication with the host. In all these cases, the controller is unable to indicate any aborts or update any completion queue entries.

7.3.3 Queue Level

The host may reset and/or reconfigure the I/O Submission and I/O Completion Queues by resetting them. A queue level reset is performed by deleting and then recreating the queue. In this process, the host should wait for all pending commands to the appropriate I/O Submission Queue(s) to complete. To perform the reset, the host submits the Delete I/O Submission Queue or Delete I/O Completion Queue command to the Admin Queue specifying the identifier of the queue to be deleted. After successful command completion of the queue delete operation, the host then recreates the queue by submitting the Create I/O Submission Queue or Create I/O Completion Queue command. As part of the creation operation, the host may modify the attributes of the queue.

The host should ensure that the appropriate I/O Submission Queue or I/O Completion Queue is idle before deleting that queue. Submitting a queue deletion command causes any pending commands to be aborted by the controller; this may or may not result in a completion queue entry being posted for the aborted command(s). Note that if a queue level reset is performed on an I/O Completion Queue, the I/O Submission Queues that are utilizing the I/O Completion Queue should be deleted before the I/O Completion Queue is reset and recreated after the I/O Completion Queue is recreated. The behavior of an I/O Submission Queue without a corresponding I/O Completion Queue is undefined.

7.4 Queue Management

7.4.1 Queue Setup and Initialization

To setup and initialize I/O Submission Queues and I/O Completion Queues for use, host software follows these steps:

1. Configures the Admin Submission and Completion Queues by initializing the Admin Queue Attributes (AQA), Admin Submission Queue Base Address (ASQ), and Admin Completion Queue Base Address (ACQ) registers appropriately;
2. Configure the size of the I/O Submission Queues (CC.IOSQES) and I/O Completion Queues (CC.IOCQES);
3. Submits a Set Features command with the Number of Queues attribute set to the requested number of I/O Submission Queues and I/O Completion Queues. The completion queue entry for this Set Features command indicates the number of I/O Submission Queues and I/O Completion Queues allocated by the controller;
4. Determines the maximum number of entries supported per queue (CAP.MQES) and whether the queues are required to be physically contiguous (CAP.CQR);

5. Creates I/O Completion Queues within the limitations of the number allocated by the controller and the queue attributes supported (maximum entries and physically contiguous requirements) by using the Create I/O Completion Queue command; and
6. Creates I/O Submission Queues within the limitations of the number allocated by the controller and the queue attributes supported (maximum entries and physically contiguous requirements) by using the Create I/O Submission Queue command.

At the end of this process, I/O Submission Queues and I/O Completion Queues have been setup and initialized and may be used to complete I/O commands.

7.4.2 Queue Coordination

There is one Admin Queue pair associated with multiple I/O queue pairs. The Admin Submission Queue and Completion Queue are used to carry out functions that impact the entire controller. An I/O Submission Queue and Completion Queue may be used to carry out I/O (read/write) operations and may be distributed across CPU cores and threads.

An Admin command may impact one or more I/O queue pairs. The host should ensure that Admin actions are coordinated with threads that are responsible for the I/O queue pairs to avoid unnecessary error conditions. The details of this coordination are outside the scope of this specification.

7.4.3 Queue Abort

To abort a large number of commands, the recommended procedure is to delete and recreate the I/O Submission Queue. Specifically, to abort all commands that are submitted to the I/O Submission Queue host software should issue a Delete I/O Submission Queue command for that queue. After the queue has been successfully deleted, indicating that all commands have been completed or aborted, then host software should recreate the queue by submitting a Create I/O Submission Queue command. Host software may then re-submit commands to the associated I/O Submission Queue.

7.5 Interrupts

The interrupt architecture allows for efficient reporting of interrupts such that the host may service interrupts through the least amount of overhead.

The specification allows the controller to be configured to report interrupts in one of four modes. The four modes are: pin-based interrupt, single message MSI, multiple message MSI, and MSI-X. It is recommended that MSI-X be used whenever possible to enable higher performance, lower latency, and lower CPU utilization for processing interrupts.

Interrupt aggregation, also referred to as interrupt coalescing, mitigates host interrupt overhead by reducing the rate at which interrupt requests are generated by a controller. This reduced host overhead typically comes at the expense of increased latency. Rather than prescribe a specific interrupt aggregation algorithm, this specification defines the mechanisms a host may use to communicate interrupt aggregation parameters to a controller and leaves the specific interrupt aggregation algorithm used by a controller as vendor specific. Interrupts associated with the Admin Completion Queue should not be delayed.

The Aggregation Threshold field in the Interrupt Coalescing feature (refer to section 5.21.1.8) specifies the minimum interrupt aggregation threshold on a per vector basis. This value defines the number of Completion Queue entries that when aggregated on a per interrupt vector basis reduces host interrupt processing overhead below a host determined threshold. This value is provided to the controller as a recommendation by the host and a controller is free to generate an interrupt before or after this aggregation threshold is achieved. The specific manner in which this value is used by the interrupt aggregation algorithm implemented by a controller is implementation specific.

The Aggregation Time field in the Interrupt Coalescing feature (refer to section 5.21.1.8) specifies the maximum delay that a controller may apply to a Completion Queue entry before an interrupt is signaled to the host. This value is provided to the controller as a recommendation by the host and a controller is free to generate an interrupt before or after this aggregation time is achieved. A controller may apply this value on a per vector basis or across all vectors. The specific manner in which this value is used by the interrupt aggregation algorithm implemented by a controller is implementation specific.

Although support of the Get Features and Set Features commands associated with interrupt coalescing is required, the manner in which the Aggregation Threshold and Aggregation Time fields are used is implementation specific. For example, an implementation may ignore these fields and not implement interrupt coalescing.

7.5.1 Pin Based, Single MSI, and Multiple MSI Behavior

This is the mode of interrupt operation if any of the following conditions are met:

- Pin based interrupts are being used – MSI (MSICAP.MC.MSIE='0') and MSI-X are disabled;
- Single MSI is being used – MSI is enabled (MSICAP.MC.MSIE='1'), MSICAP.MC.MME=000b, and MSI-X is disabled; or
- Multiple MSI is being used – Multiple-message MSI is enabled (MSICAP.MC.MSIE='1'), MSICAP.MC.MME is set to a value between 001b and 101b inclusive, and MSI-X is disabled.

Within the controller there is an interrupt status register (IS) that is not visible to the host. In this mode, the IS register determines whether the PCI interrupt line shall be driven active or an MSI message shall be sent. Each bit in the IS register corresponds to an interrupt vector. The IS bit is set to '1' when the following conditions are true:

- There is one or more unacknowledged completion queue entries in a Completion Queue that utilizes this interrupt vector;
- The Completion Queue(s) with unacknowledged completion queue entries has interrupts enabled in the "Create I/O Completion Queue" command; and
- The corresponding INTM bit exposed to the host is cleared to '0', indicating that the interrupt is not masked.

For single and multiple MSI, the INTM register masks interrupt delivery prior to MSI logic. As such, an interrupt on a vector masked by INTM does not cause the corresponding Pending bit to assert within the MSI Capability Structure.

If MSIs are not enabled, IS[0] being set to '1' causes the PCI interrupt line to be active (electrical '0'). If MSIs are enabled, any change to the IS register that causes an unmasked status bit to transition from '0' to '1' or clearing of a mask bit to '0' whose corresponding status bit is set to '1' shall cause an MSI to be sent. Therefore, while in wire mode, a single wire remains active, while in MSI mode, several messages may be sent, as each edge triggered event on a port shall cause a new message.

In order to clear an interrupt for a particular interrupt vector, host software shall acknowledge all completion queue entries for Completion Queues associated with the interrupt vector.

Figure 439: Pin Based, Single MSI, and Multiple MSI Behavior

Status of IS Register	Pin-based Action	MSI Action
All bits '0' Note: May be caused by corresponding bit(s) in the INTM register being set to '1', masking the corresponding interrupt.	Wire inactive	No action
One or more bits set to '1' Note: May be caused by corresponding bit(s) in the INTM register being cleared to '0', unmasking the corresponding interrupt.	Wire active	New message sent
One or more bits set to '1', new bit gets set to '1'	Wire active	New message sent

Figure 439: Pin Based, Single MSI, and Multiple MSI Behavior

Status of IS Register	Pin-based Action	MSI Action
One or more bits set to '1', some (but not all) bits in the IS register are cleared to '0' (i.e., host software acknowledges some of the associated completion queue entries)	Wire active	New message sent
One or more bits set to '1', all bits in the IS register are cleared to '0' (i.e., host software acknowledges all associated completion queue entries)	Wire inactive	No action

7.5.1.1 Host Software Interrupt Handling

It is recommended that host software utilize the Interrupt Mask Set and Interrupt Mask Clear (INTMS/INTMC) registers to efficiently handle interrupts when configured to use pin based or MSI messages. Specifically, within the interrupt service routine, host software should set the appropriate mask register bits to '1' to mask interrupts via the INTMS register. In the deferred procedure call, host software should process all completion queue entries and acknowledge the completion queue entries have been processed by writing the associated CQyHDBL doorbell registers. When all completion queue entries have been processed, host software should unmask interrupts by clearing the appropriate mask register bits to '0 via the INTMC register.

It is recommended that the MSI interrupt vector associated with the CQ(s) being processed be masked during processing of completion queue entries within the CQ(s) to avoid spurious and/or lost interrupts. For single message or multiple message MSI, the INTMS and INTMC registers should be used to appropriately mask interrupts during completion queue entry processing.

7.5.1.1.1 Interrupt Example (Informative)

An example of the host software flow for processing interrupts is described in this section. This example assumes multiple message MSI is used and that interrupt vector 3 is associated with I/O Completion Queue 3:

1. The controller posts a completion queue entry to I/O Completion Queue 3. The controller sets IS[3] to '1' in its internal IS register. The controller asserts an interrupt to the host;
2. The interrupt service routine (ISR) is triggered;
3. Host software scans all I/O Completion Queues associated with the asserted MSI vector to determine the location of new completion queue entries. In this case, a new completion queue entry has been posted to I/O Completion Queue 3;
4. Host software writes 08h to the INTMS register to mask interrupts for interrupt vector 3, which is associated with I/O Completion Queue 3;
5. The controller masks interrupt vector 3, based on the host write to the INTMS register;
6. Host software schedules a deferred procedure call (DPC) to process the completed command;
7. The deferred procedure call (DPC) is triggered;
8. Host software processes new completion queue entries for I/O Completion Queue 3, completing the associated commands to the OS. Host software updates CQyHDBL to acknowledge the processed completion queue entries and clear the interrupt associated with those completion queue entries. If all completion queue entries have been acknowledged by host software, the controller de-asserts interrupt vector 3; and
9. Host software unmasks interrupt vector 3 by writing 08h to the INTMC register.

7.5.1.2 Differences Between Pin Based and MSI Interrupts

Single MSI is similar to the pin based interrupt behavior mode. The primary difference is the method of reporting the interrupt. Instead of communicating the interrupt through an INTx virtual wire, an MSI message

is generated to the host. Unlike INTx virtual wire interrupts which are level sensitive, MSI interrupts are edge sensitive.

Pin based and single MSI only use one interrupt vector. Multiple MSI may use up to 32 interrupt vectors.

For multiple MSI, the controller advertises the requested number of MSI interrupt vectors in the Multiple Message Capable (MMC) field in the Message Signaled Interrupt Message Control (MC) register. The MSICAP.MC.MMC field represents a power-of-2 wrapper on the number of requested vectors. For example, if three vectors are requested, then the MSICAP.MC.MMC field shall be '010' (four vectors).

Multiple-message MSI allows completions to be aggregated on a per vector basis. If sufficient MSI vectors are allocated, each Completion Queue(s) may send its own interrupt message, as opposed to a single message for all completions.

7.5.2 MSI-X Based Behavior

This is the mode of interrupt operation if the MSI-X is being used – (multiple-message) MSI is disabled (MSICAP.MC.MSIE='0') and (MSICAP.MC.MME=000b) and MSI-X is enabled. This is the preferred interrupt behavior to use.

MSI-X, similar to multiple-message MSI, allows completions to be aggregated on a per vector basis. However, the maximum number of vectors is 2K. MSI-X also allows each interrupt to send a unique message data corresponding to the vector.

MSI-X allows completions to be aggregated on a per vector basis. Each Completion Queue(s) may send its own interrupt message, as opposed to a single message for all completions.

When generating an MSI-X message, the following checks occur before generating the message:

- The Function Mask bit in the MSI-X Message Control register is not set to '1'; and
- The corresponding vector mask in the MSI-X table structure is not set to '1'.

If either of the mask bits are set to '1', the corresponding pending bit in the MSI-X PBA structure is set to '1' to indicate that an interrupt is pending for that vector. The MSI for that vector is later generated when both the mask bits are reset to '0'.

It is recommended that the interrupt vector associated with the CQ(s) being processed be masked during processing of completion queue entries within the CQ(s) to avoid spurious and/or lost interrupts. The interrupt mask table defined as part of MSI-X should be used to mask interrupts.

7.6 Controller Initialization and Shutdown Processing

This section describes the recommended procedure for initializing the controller and for shutdown processing prior to a power-off condition.

7.6.1 Initialization

The host should perform the following actions in sequence to initialize the controller to begin executing commands:

1. Set the PCI and PCI Express registers described in section 2 appropriately based on the system configuration. This includes configuration of power management features. A single interrupt (e.g., pin-based, single-MSI, or single MSI-X) should be used until the number of I/O Queues is determined;
2. The host waits for the controller to indicate that any previous reset is complete by waiting for CSTS.RDY to become '0';
3. The Admin Queue should be configured. The Admin Queue is configured by setting the Admin Queue Attributes (AQA), Admin Submission Queue Base Address (ASQ), and Admin Completion Queue Base Address (ACQ) to appropriate values;

4. The controller settings should be configured. Specifically:
   a. The arbitration mechanism should be selected in CC.AMS;
   b. The memory page size should be initialized in CC.MPS; and
   c. The I/O Command Set that is to be used should be selected in CC.CSS or CC.CSS field should be set to the value indicating that only the Admin Command Set is supported;
5. The controller should be enabled by setting CC.EN to '1';
6. The host should wait for the controller to indicate that the controller is ready to process commands. The controller is ready to process commands when CSTS.RDY is set to '1';
7. The host should determine the configuration of the controller by issuing the Identify command, specifying the Identify Controller data structure. The host should then determine the configuration of each namespace by issuing the Identify command for each namespace, specifying the Identify Namespace data structure;
8. If the controller implements I/O queues, then the host should determine the number of I/O Submission Queues and I/O Completion Queues supported using the Set Features command with the Number of Queues feature identifier. After determining the number of I/O Queues, the MSI and/or MSI-X registers should be configured;
9. If the controller implements I/O queues, then the host should allocate the appropriate number of I/O Completion Queues based on the number required for the system configuration and the number supported by the controller. The I/O Completion Queues are allocated using the Create I/O Completion Queue command;
10. If the controller implements I/O queues, then the host should allocate the appropriate number of I/O Submission Queues based on the number required for the system configuration and the number supported by the controller. The I/O Submission Queues are allocated using the Create I/O Submission Queue command; and
11. To enable asynchronous notification of optional events, the host should issue a Set Features command specifying the events to enable. To enable asynchronous notification of events, the host should submit an appropriate number of Asynchronous Event Request commands. This step may be done at any point after the controller signals that the controller is ready (i.e., CSTS.RDY is set to '1').

After performing these steps, the controller shall be ready to process Admin or I/O commands issued by the host.

For exit of the D3 power state, the initialization steps outlined should be followed.

7.6.1.1 Software Progress Marker

The Software Progress Marker feature, defined in section 5.21.1.25, indicates the number of times pre-boot software has loaded prior to the OS successfully loading. If the pre-boot software load count becomes large, there may be issues with cached data within the NVM since the OS driver software has not set this field to 0h recently. In this case, the OS driver software may choose to use the NVM more conservatively (e.g., not utilize cached data).

The Software Progress Marker should be updated by both Pre-boot and OS driver software as part of completing initialization.

7.6.2 Shutdown

It is recommended that the host perform an orderly shutdown of the controller by following the procedure in this section when a power-off or shutdown condition is imminent.

The host should perform the following actions in sequence for a normal shutdown:

1. Stop submitting any new I/O commands to the controller and allow any outstanding commands to complete;

2. If the controller implements I/O queues, then the host should delete all I/O Submission Queues, using the Delete I/O Submission Queue command. A result of the successful completion of the Delete I/O Submission Queue command is that any remaining commands outstanding are aborted;
3. If the controller implements I/O queues, then the host should delete all I/O Completion Queues, using the Delete I/O Completion Queue command; and
4. The host should set the Shutdown Notification (CC.SHN) field to 01b to indicate a normal shutdown operation. The controller indicates when shutdown processing is completed by updating the Shutdown Status (CSTS.SHST) field to 10b.

For entry to the D3 power state, the shutdown steps outlined for a normal shutdown should be followed.

The host should perform the following actions in sequence for an abrupt shutdown:

1. Stop submitting any new I/O commands to the controller; and
2. The host should set the Shutdown Notification (CC.SHN) field to 10b to indicate an abrupt shutdown operation. The controller indicates when shutdown processing is completed by updating the Shutdown Status (CSTS.SHST) field to 10b.

It is recommended that the host wait a minimum of the RTD3 Entry Latency reported in the Identify Controller data structure for the shutdown operations to complete; if the value reported in RTD3 Entry Latency is 0h, then the host should wait for a minimum of one second. It is not recommended to disable the controller via the CC.EN field. This causes a Controller Reset which may impact the time required to complete shutdown processing. While shutdown processing is in progress, the controller may abort any command with a status code of Commands Aborted due to Power Loss Notification.

It is safe to power off the controller when CSTS.SHST indicates shutdown processing is complete (regardless of the value of CC.EN). It remains safe to power off the controller until CC.EN transitions from ‘0’ to ‘1’.

To start executing commands on the controller after a shutdown operation, a Controller Reset (CC.EN cleared from ‘1’ to ‘0’) is required. The initialization sequence should then be executed.

It is an implementation choice whether the host aborts all outstanding commands to the Admin Queue prior to the shutdown. The only commands that should be outstanding to the Admin Queue at shutdown are Asynchronous Event Request commands.

7.7 Asynchronous Event Request Host Software Recommendations (Informative)

This section describes the recommended host software procedure for Asynchronous Event Requests.

The host sends *n* Asynchronous Event Request commands (refer to section 7.6.1, step 11). When an Asynchronous Event Request completes (providing Event Type, Event Information, and Log Page details):

- If the event(s) in the reported Log Page may be disabled with the Asynchronous Event Configuration feature (refer to section 5.21.1.11), then host software issues a Set Features command for the Asynchronous Event Configuration feature specifying to disable reporting of all events that utilize the Log Page reported. Host software should wait for the Set Features command to complete;
- Host software issues a Get Log Page command requesting the Log Page reported as part of the Asynchronous Event Command completion. Host software should wait for the Get Log Page command to complete;
- Host software parses the returned Log Page. If the condition is not persistent, then host software should re-enable all asynchronous events that utilize the Log Page. If the condition is persistent, then host software should re-enable all asynchronous events that utilize the Log Page except for the one(s) reported in the Log Page. The host re-enables events by issuing a Set Features command for the Asynchronous Event Configuration feature;
- Host software should issue an Asynchronous Event Request command to the controller (restoring to *n* the number of these commands outstanding); and

- If the reporting of event(s) was disabled, host software should enable reporting of the event(s) using the Asynchronous Event Configuration feature. If the condition reported may persist, host software should continue to monitor the event (e.g., spare below threshold) to determine if reporting of the event should be re-enabled.

7.8 Feature Values

The Get Features command, (refer to section 5.13), and Set Features command, (refer to section 5.21), may be used to read and modify operating parameters of the controller. The operating parameters are grouped and identified by Feature Identifiers. Each Feature Identifier contains one or more attributes that may affect the behavior of the Feature.

If bit 4 is set to '1' in the Optional NVM Command Support (ONCS) field of the Identify Controller data structure in Figure 251, then for each Feature, there are three settings: default, saved, and current. If bit 4 is cleared to '0' in the Optional NVM Command Support field of the Identify Controller data structure, then the controller only supports a current and default value for each Feature. In this case, the current value may be persistent across power states based on the information specified in Figure 275 and Figure 276.

Each Feature has supported capabilities (refer to Figure 188), which are discovered by using the Supported Capabilities value in the Select field in Get Features (refer to Figure 187).

The default value for each Feature is vendor specific and set by the manufacturer unless otherwise specified. The default value is not changeable.

The saved value is the value that the Feature has after a Controller Level Reset. A Feature may be saveable. If a Feature is not saveable, then:

a) the default value is used after a Controller Level Reset; and
b) a Get Features command to read the saved value returns the default value.

The current value for a Feature is the value in active use by the controller for that Feature.

A Set Feature command uses the value specified by the command to set:

a) The current value for that Feature; or
b) The current value for that Feature, and the saved value for that Feature, if that Feature is saveable.

Feature settings may apply to:

a) the controller (i.e., the feature is not namespace specific); or
b) a namespace (i.e., the feature is namespace specific).

For feature values that apply to the controller:

a) if the NSID field is cleared to 0h or set to FFFFFFFFh, then:

   - the Set Features command shall set the specified feature value for the controller; and
   - the Get Features command shall return the current setting of the requested feature value for the controller;

   and

b) if the NSID field is set to a valid namespace identifier (refer to section 6.1), then:

   - the Set Features command shall abort with a status code of Feature Not Namespace Specific; and
   - the Get Features command shall return the current setting of the requested feature value for the controller.

For feature values that apply to a namespace:

a) if the NSID field is set to an active namespace identifier (refer to section 6.1), then:

- the Set Features command shall set the specified feature value of the specified namespace; and
- the Get Features command shall return the current setting of the requested feature value for the specified namespace;

b) if the NSID field is set to FFFFFFFFh, then:

- the Set Features command shall, unless otherwise specified, set the specified feature value for all namespaces attached to the controller processing the command; and
- the Get Features command shall, unless otherwise specified in section 5.21.1, abort with a status code of Invalid Namespace or Format;

and

c) if the NSID field is set to any other value, then the Set Features command and the Get Features command shall abort as described in the rules for namespace identifier usage in Figure 106.

If the controller supports the Save field in the Set Features command and the Select field in the Get Features command, then any Feature Identifier that is namespace specific may be saved on a per namespace basis.

There are mandatory and optional Feature Identifiers defined in Figure 275 and Figure 276. If a Get Features command or Set Features command is processed that specifies a Feature Identifier that is not supported, then the controller shall abort the command with a status of Invalid Field in Command.

7.9 NVMe Qualified Names

NVMe Qualified Names (NQNs) are used to uniquely describe a host or NVM subsystem for the purposes of identification and authentication. The NVMe Qualified Name for the NVM subsystem is specified in the Identify Controller data structure. An NQN is permanent for the lifetime of the host or NVM subsystem.

An NVMe Qualified Name is encoded as a string of Unicode characters with the following properties:

- The encoding is UTF-8 (refer to RFC 3629);
- The following characters are used in formatting:
  - dash (‘-‘=U+002d);
  - dot (‘.’=U+002e); and
  - colon (‘:’=U+003a);
- The maximum name is 223 bytes in length; and
- The string is null terminated.

There are two supported NQN formats. The first format may be used by any organization that owns a domain name. This naming format may be used to create a human interpretable string to describe the host or NVM subsystem. This format consists of:

- The string “nqn”;
- A date code, in “yyyy-mm” format. This date shall be during a time interval when the naming authority owned the domain name used in this format. The date code uses the Gregorian calendar. All digits and the dash shall be included;
- The string “.” (i.e., the ASCII period character);
- The reverse domain name of the naming authority that is creating the NQN; and
- A colon (:) prefixed string that the owner of the domain name assigns that does not exceed the maximum length. The naming authority is responsible to ensure that the NQN is worldwide unique.

The reverse domain name in an NQN that uses this format shall not be “org.nvmexpress”.

The following are examples of NVMe Qualified Names that may be generated by “Example NVMe, Inc.”

- nqn.2014-08.com.example:nvme:nvm-subsystem-sn-d78432; and
- nqn.2014-08.com.example:nvme.host.sys.xyz.

The second format may be used to create a unique identifier when there is not a naming authority or there is not a requirement for a human interpretable string. This format consists of:

- The string “nqn”;
- The string “2014-08.org.nvmexpress:uuid:”; and
- A 128-bit UUID based on the definition in RFC 4122 represented as a string formatted as “*11111111-2222-3333-4444-555555555555*”.

The following is an example of an NVMe Qualified Name using the UUID-based format:

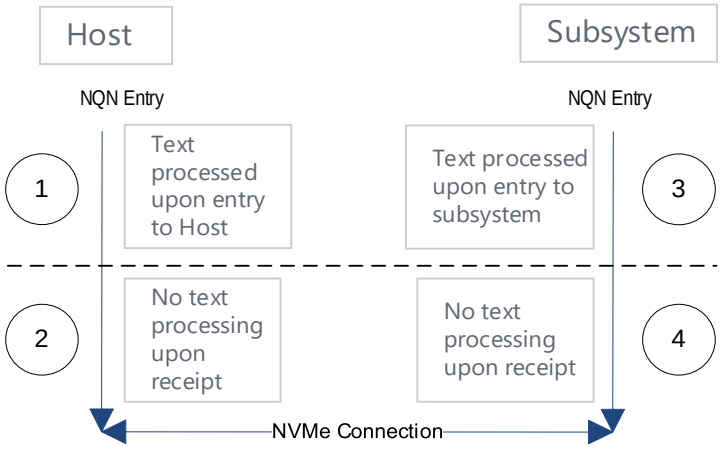
- nqn.2014-08.org.nvmexpress:uuid:f81d4fae-7dec-11d0-a765-00a0c91e6bf6.

NVMe hosts, controllers and NVM subsystems compare (e.g., for equality) NVMe Qualified Names used by NVMe as binary strings without any text processing or text comparison logic that is specific to the Unicode character set or locale (e.g., case folding or conversion to lower case, Unicode normalization). Any such text processing:

a) may occur as part of entry of NVMe Qualified Names into NVMe hosts and NVM subsystems; and
b) should not occur as part of receiving NVMe Qualified Names via an NVMe connection, as shown in Figure 440.

Upon entry (e.g., at point 1 in Figure 440, described as “input” in RFC4122), NVMe host software may process an NVMe Qualified Name (e.g., for conversion to lower case based on the Unicode locale). Upon entry (e.g., at point 3 in Figure 440, described as “input” in RFC4122), a controller may process an NVMe Qualified Name (e.g., for conversion to lower case based on the Unicode locale). Upon receipt by the host (e.g., at point 2 in Figure 440) of an NVMe Qualified Name from the controller, no text process (e.g., no case folding) should occur. Upon receipt by the controller (e.g., at point 4 in Figure 440) of an NVMe Qualified Name from the host, no text processing (e.g., no case folding) should occur.

Figure 440: NQN Processing



7.10 Identifier Format and Layout (Informative)

This section provides guidance for proper implementation of various identifiers defined in the Identify Controller, Identify Namespace, and Namespace Identification Descriptor data structures.

7.10.1 PCI Vendor ID (VID) and PCI Subsystem Vendor ID (SSVID)

The PCI Vendor ID (VID, bytes 01:00) and PCI Subsystem Vendor ID (SSVID, bytes 03:02) are defined in the Identify Controller data structure. The values are assigned by the PCI SIG. Each identifier is a 16-bit number in little endian format.

Example:

- VID = ABCDh; and
- SSVID = 1234h.

Figure 441: PCI Vendor ID (VID) and PCI Subsystem Vendor ID (SSVID)

Byte	00	01	02	03
Value	CDh	ABh	34h	12h

7.10.2 Serial Number (SN) and Model Number (MN)

The Serial Number (SN, bytes 23:04) and Model Number (MN, bytes 63:24) are defined in the Identify Controller data structure. The values are ASCII strings assigned by the vendor. Each identifier is in big endian format.

Example (Value shown as ASCII characters):

- SN = “SN1”; and
- MN = “M2”.

Figure 442: Serial Number (SN) and Model Number (MN)

Bytes	04	05	06	23 to 07	24	25	63 to 26
Value	53h (‘S’)	4Eh (‘N’)	31h (‘1’)	20h (‘ ‘)	4Dh (‘M’)	32h (‘2’)	20h (‘ ‘)

7.10.3 IEEE OUI Identifier (IEEE)

The IEEE OUI Identifier (OUI, bytes 75:73) is defined in the Identify Controller data structure. The value is assigned by the IEEE Registration Authority. The identifier is in little endian format.

Example:

- OUI = ABCDEFh.

Figure 443: IEEE OUI Identifier (IEEE)

Byte	73	74	75
Value	EFh	CDh	ABh

7.10.4 IEEE Extended Unique Identifier (EUI64)

The IEEE Extended Unique Identifier (EUI64, bytes 127:120) is defined in the Identify Namespace data structure. Tutorials are available at https://standards.ieee.org/develop/regauth/tut/index.html. IEEE defines three formats that may be used in this field: MA-L, MA-M, and MA-S. The examples in this section use the MA-L format.

The MA-L format is defined as a string of eight octets:

Figure 444: IEEE Extended Unique Identifier (EUI64), MA-L Format

EUI[0]	EUI[1]	EUI[2]	EUI[3]	EUI[4]	EUI[5]	EUI[6]	EUI[7]
OUI			Extension Identifier				

EUI64 is defined in big endian format. The OUI field differs from the OUI Identifier which is in little endian format as described in section 7.10.3.

Example:

- OUI Identifier = ABCDEFh; and
- Extension Identifier = 0123456789h.

Figure 445: IEEE Extended Unique Identifier (EUI64), OUI Identifier

Byte	120	121	122	123	124	125
Value	ABh	CDh	EFh	01h	23h	45h
Field	OUI			Extension Identifier		

Figure 446: IEEE Extended Unique Identifier (EUI64), Ext. ID (cont)

Byte	126	127
Value	67h	89h
Field	Ext ID (cont)	

The MA-L format is similar to the World Wide Name (WWN) format defined as IEEE Registered designator (NAA = 5) as shown below.

Figure 447: MA-L similarity to WWN

Byte	0	1	2	3	4	5	6	7
EUI64	OUI			Extension Identifier				
WWN (NAA = 5)	5h	OUI		Vendor Specific Identifier				

7.10.5 Namespace Globally Unique Identifier (NGUID)

The Namespace Globally Unique Identifier (NGUID, bytes 119:104) is defined in the Identify Namespace data structure. The NGUID is composed of an IEEE OUI, an extension identifier, and a vendor specific extension identifier. The extension identifier and vendor specific extension identifier are both assigned by the vendor and may be considered as a single field. NGUID is defined in big endian format. The OUI field differs from the OUI Identifier which is in little endian format as described in section 7.10.3.

Example:

- OUI Identifier = ABCDEFh;
- Extension Identifier = 0123456789h; and
- Vendor Specific Extension Identifier = FEDCBA9876543210h.

Figure 448: Namespace Globally Unique Identifier (NGUID)

Byte	104	105	106	107	108	109
Value	FEh	DCh	BAh	98h	76h	54h
Field	Vendor Specific Extension Identifier					

Figure 449: Namespace Globally Unique Identifier (NGUID), OUI

Byte	110	111	112	113	114	115
Value	32h	10h	ABh	CDh	EFh	01h
Field	VSP Ex ID (cont)		OUI			Ex ID

Figure 450: Namespace Globally Unique Identifier (NGUID), Extension Identifier (continued)

Byte	116	117	118	119
Value	23h	45h	67h	89h
Field	Extension Identifier (continued)			

The NGUID format is similar to the World Wide Name (WWN) format as IEEE Registered Extended designator (NAA = 6) as shown below.

Figure 451: Namespace Globally Unique Identifier (NGUID), NGUID similarity to WWN

Byte	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
NGUID	Vendor Specific Extension Identifier								OUI			Extension Identifier				
WWN (NAA = 6)	6h	OUI			Vendor Specific Identifier				Vendor Specific Identifier Extension							

7.10.6 Universally Unique Identifier (UUID)

The Universally Unique Identifier is defined in RFC 4122 and contained in the Namespace Identification Descriptor (refer to Figure 253). Byte ordering requirements for a UUID are described in RFC 4122.

7.11 Unique Identifier

The NVM Subsystem NVMe Qualified Name specified in the Identify Controller data structure (refer to Figure 251) should be used (e.g., by host software) as the unique identifier for the NVM subsystem. If the controller complies with an older version of this specification that does not include the NVM Subsystem NQN, then the PCI Vendor ID, Serial Number, and Model Number fields in the Identify Controller data structure and the NQN Starting String “nqn.2014.08.org.nvmexpress:” may be combined by the host to form a globally unique value that identifies the NVM subsystem (e.g., for host software that uses NQNs). The method shown in Figure 452 should be used by the host to construct an NVM Subsystem NQN for older NVM subsystems that do not provide an NQN in the Identify Controller data structure. The mechanism used by the vendor to assign Serial Number and Model Number values to ensure uniqueness is outside the scope of this specification.

Figure 452: NQN Construction for Older NVM Subsystems

Bytes	Description
26:00	**NQN Starting String (NSS):** Contains the 27 letter ASCII string ”nqn.2014-08.org.nvmexpress:”.
30:27	**PCI Vendor ID (VID):** Contains the company vendor identifier that is assigned by the PCI SIG as a hexadecimal ASCII string.
34:31	**PCI Subsystem Vendor ID (SSVID):** Contains the company vendor identifier that is assigned by the PCI SIG for the subsystem as a hexadecimal ASCII string.
54:35	**Serial Number (SN):** Contains the serial number for the NVM subsystem that is assigned by the vendor as an ASCII string.
94:55	**Model Number (MN):** Contains the model number for the NVM subsystem that is assigned by the vendor as an ASCII string.
222:95	**Padding (PAD):** Contains spaces (ASCII character 20h).

An NVM subsystem may contain multiple controllers. All of the controllers that make up an NVM subsystem share the same NVM subsystem unique identifier. The Controller ID (CNTLID) value returned in the Identify Controller data structure may be used to uniquely identify a controller within an NVM subsystem. The Controller ID value when combined with the NVM subsystem identifier forms a globally unique value that

identifies the controller. The mechanism used by the vendor to assign Controller ID values is outside the scope of this specification.

The Identify Namespace data structure (refer to Figure 249) contains the IEEE Extended Unique Identifier (EUI64) and the Namespace Globally Unique Identifier (NGUID) fields. The Namespace Identification Descriptor data structure (refer to Figure 253) contains the Namespace UUID. EUI64 is an 8-byte EUI-64 identifier (refer to section 7.10.4), NGUID is a 16-byte identifier based on EUI-64 (refer to section 7.10.5), and Namespace UUID is a 16-byte identifier described in RFC 4122 (refer to section 7.10.6).

When creating a namespace, the controller shall indicate a globally unique value in one or more of the following:

a) the EUI64 field;
b) the NGUID field; or
c) a Namespace Identification Descriptor with the Namespace Identifier Type field set to 3h.

If the EUI64 field is cleared to 0h and the NGUID field is cleared to 0h, then the namespace shall support a valid Namespace UUID in the Namespace Identification Descriptor data structure.

If the UIDREUSE bit in the NSFEAT field is cleared to ‘0’, then a controller may reuse a non-zero NGUID/EUI64 value for a new namespace after the original namespace using the value has been deleted. If the UIDREUSE bit is set to ‘1’, then a controller shall not reuse a non-zero NGUID/EUI64 for a new namespace after the original namespace using the value has been deleted.

7.12 Keep Alive

The Keep Alive timer is a watchdog timer intended to detect a malfunctioning connection, controller, or host. The Keep Alive Timeout Interval is the period during which the Keep Alive Timer is activated.

A Keep Alive Timeout Interval on the controller starts when:

- a successful Completion Queue entry is posted for a Set Features command with Feature Identifier 0Fh and a non-zero KATO field.

A Keep Alive Timeout Interval on the host starts when:

- a Set Features command with Feature Identifier 0Fh and a non-zero KATO field is posted to the Admin submission queue; or
- a Keep Alive command was posted to the Admin submission queue.

Both on the host and the controller the Keep Alive Timeout Interval ends the time specified by the KATO field after the interval started (refer to Figure 306). A Keep Alive Timeout occurs when the Keep Alive Timer expires. The Keep Alive Timer expires:

- if TBKAS is cleared to ‘0’, at the end of the Keep Alive Timeout Interval and no Keep Alive Command was processed during the Keep Alive Timeout Interval (refer to section 7.12.1); and
- if TBKAS is set to ‘1’, at the end of the Keep Alive Timeout Interval and no Admin command or I/O command was processed during the Keep Alive Timeout Interval (refer to section 7.12.2).

The Keep Alive Timeout is the maximum time a connection remains established without processing a Keep Alive command. The Keep Alive timer in the controller expires when a Keep Alive command is not received within the Keep Alive Timeout interval.

The Keep Alive timer is active if:

- CC.EN is set to ‘1’;
- CSTS.RDY is set to ‘1’;
- CC.SHN is cleared to ‘00b’;
- CSTS.SHST is cleared to ‘00b’; and
- the Keep Alive Timer feature has been enabled with a KATO field (refer to section 5.21.1.15 or the Fabric Connect command in the NVMe over Fabrics specification) set to a non-zero value,

otherwise, the Keep Alive timer is inactive and a Keep Alive Timeout shall not occur. Activating an inactive Keep Alive timer (e.g., enabling a controller with the Keep Alive feature in use, enabling a controller that supports NVMe-oF where the Connect command specified a non-zero Keep Alive Timeout (refer to the NVMe over Fabrics specification)) shall initialize the Keep Alive timer to the Keep Alive Timeout (KATO) value.

The host may consider a Keep Alive Timeout to have occurred when the completion of the Keep Alive command is not received within the Keep Alive Timeout interval. The host is intended to send Keep Alive commands at a faster rate than the Keep Alive Timeout accounting for transport roundtrip times, transport delays, command execution times, and the Keep Alive Timer granularity.

If a Keep Alive Timer expires:

- the controller records an Error Information Log Entry with the status code Keep Alive Timeout Expired and sets the Controller Fatal Status (CSTS.CFS) bit to '1'; and
- the host assumes all outstanding commands are not completed and re-issues commands as appropriate.

The Keep Alive command restarts the timeout period; other commands have no effect on the timeout. The controller should process the Keep Alive command as soon as the command is fetched.

The NVMe Transport binding specification defines for the associated NVMe Transport:

- the minimum Keep Alive Timeout value;
- the maximum Keep Alive Timeout value; and
- if support for the Keep Alive feature is required.

NVMe Transports that do not detect a connection loss in a timely manner shall require that the Keep Alive feature be enabled. If a command attempts to disable the Keep Alive timer by setting the Keep Alive Timeout value to 0h or to a value that exceeds the maximum allowed by the associated NVMe Transport binding specification, a status value of Keep Alive Timeout Invalid shall be returned. If a command sets the Keep Alive Timeout value to a value that is less than the minimum supported by the NVMe Transport or less than the minimum supported by the specific implementation, then the controller sets the Keep Alive Timeout value to that minimum value.

7.12.1 Keep Alive Command Based Keep Alive

Keep Alive Command Based Keep Alive restricts the Keep Alive Timer on both the host and the controller to be restarted only upon the processing of a Keep Alive command. This mode is in use if TBKAS is cleared to '0'.

The Keep Alive Timeout is the maximum time a connection remains established without processing a Keep Alive command. If the Keep Alive Timer in the controller expires and a Keep Alive command has not been processed within the Keep Alive Timeout Interval, then the controller may consider a Keep Alive Timeout to have occurred. If the Keep Alive Timer in the host expires and a completion of a Keep Alive command has not been received with the Keep Alive Timeout Interval, then the host may consider a Keep Alive Timeout to have occurred. The host should send Keep Alive commands at half of the Keep Alive Timeout accounting for transport roundtrip times, transport delays, command processing times, and the Keep Alive Timer granularity.

7.12.2 Traffic Based Keep Alive

Traffic Based Keep Alive (TBKAS) allows the host and controller to restart the Traffic Based Keep Alive Timer in the presence of Admin or I/O command processing. The controller support for TBKAS is indicated in the Controller Attributes in the Identify Controller data structure (refer to Figure 251). If the Controller does not support Traffic Based Keep Alive (TBKAS is cleared to '0'), then the operation of the Keep Alive feature is described in section 7.12.1.

The Traffic Based Keep Alive Timeout occurs if a connection remains established without processing an Admin command or an I/O command during the Keep Alive Timeout Interval. If an Admin command or an I/O command is processed within the Keep Alive Timeout Interval, then upon the expiration of the Keep Alive Timer, the Keep Alive Timer shall be restarted.

The controller may consider a Keep Alive Timeout to have occurred if no Admin command or no I/O command is transferred to the controller (as defined in section 4.11) within the Keep Alive Timeout Interval. If an Admin command or an I/O command is transferred to the Controller within the Keep Alive Timeout Interval, then upon the expiration of the Keep Alive Timer the controller shall restart the Keep Alive Timer.

The host may consider a Traffic Based Keep Alive Timeout to have occurred if the host does not receive a completion of any Admin command or any I/O command within the Keep Alive Timeout Interval. If an Admin command or an I/O command is completed within the Keep Alive Timeout Interval, then upon expiration of the Keep Alive Timer, the host shall restart the Keep Alive Timer. The host should check for a command completion entry for any Admin commands and I/O commands at half of the Keep Alive Timeout accounting for transport roundtrip times, transport delays, command processing times, and the Keep Alive Timer granularity. To prevent the controller from detecting a Keep Alive Timeout, if no Admin command and no I/O command is sent to the controller during half of the Keep Alive Timeout Interval, the host should send a Keep Alive Command.

7.12.3 Keep Alive for NVMe over PCIe Implementations

The Keep Alive feature is not required for NVMe over PCIe implementations. The PCIe Transport does not impose any limitations on the minimum and maximum Keep Alive Timeout value.

7.13 Updating Controller Doorbell Registers using a Shadow Doorbell Buffer

7.13.1 Shadow Doorbell Buffer Overview

Controllers that support the Doorbell Buffer Config command are typically emulated controllers where this feature is used to enhance the performance of host software running in Virtual Machines. If supported by the controller, host software may enable Shadow Doorbell buffers by submitting the Doorbell Buffer Config command (refer to section 5.7).

After the completion of the Doorbell Buffer Config command, host software shall submit commands by updating the appropriate entry in the Shadow Doorbell buffer instead of updating the controller's corresponding doorbell register. If updating an entry in the Shadow Doorbell buffer changes the value from being less than or equal to the value of the corresponding EventIdx buffer entry to being greater than that value, then the host shall also update the controller's corresponding doorbell register to match the value of that entry in the Shadow Doorbell buffer. Queue wrap conditions shall be taken into account in all comparisons in this paragraph.

The controller may read from the Shadow Doorbell buffer and update the EventIdx buffer at any time (e.g., before the host writes to the controller's doorbell register).

7.13.2 Example Algorithm for Controller Doorbell Register Updates (Informative)

Host software may use modular arithmetic where the modulus is the queue depth to decide if the controller doorbell register should be updated, specifically:

- Compute *X* as the new doorbell value minus the corresponding EventIdx value, modulo queue depth; and
- Compute *Y* as the new doorbell value minus the old doorbell value in the shadow doorbell buffer, also modulo queue depth.

If *X* is less than or equal to *Y*, the controller doorbell register should be updated with the new doorbell value.

7.14 Privileged Actions

Privileged actions are actions (e.g., command, register write) that affect or have the potential to affect the state of the entire NVM subsystem and not only the controller and/or namespace with which the action is associated.

Admin commands that are privileged include Namespace Management, Namespace Attachment, Virtualization Management, Format NVM, Set Features with Feature Identifier 17h (i.e., Sanitize Config, refer to section 5.21.1.23), and Sanitize. A privileged register action is NVM Subsystem Reset. Vendor specific commands and registers may also be privileged.

8 Features

8.1 Firmware Update Process

The process for a firmware update to be activated by a reset is:

1. The host issues a Firmware Image Download command to download the firmware image to the controller. There may be multiple portions of the firmware image to download, thus the offset for each portion of the firmware image being downloaded is specified in the Firmware Image Download command. The data provided in the Firmware Image Download command should conform to the Firmware Update Granularity indicated in the Identify Controller data structure or the firmware update may fail;
2. After the firmware is downloaded to the controller, the next step is for the host to submit a Firmware Commit command. The Firmware Commit command verifies that the last firmware image downloaded is valid and commits that image to the firmware slot indicated for future use. A firmware image that does not start at offset zero, contains gaps, or contains overlapping regions is considered invalid. A controller may employ additional vendor specific means (e.g., checksum, CRC, cryptographic hash or a digital signature) to determine the validity of a firmware image:
    a. The Firmware Commit command may also be used to activate a firmware image associated with a previously committed firmware slot;
3. The last step is to perform a reset that then causes the firmware image specified in the Firmware Slot field in the Firmware Commit command to be activated. The reset may be an NVM Subsystem Reset, Conventional Reset, Function Level Reset, or Controller Reset (CC.EN transitions from '1' to '0'):
    a. In some cases a Conventional Reset or NVM Subsystem Reset is required to activate a Firmware image. This requirement is indicated by Firmware Commit command specific status (refer to section 5.11.1);

    and
4. After the reset has completed, host software re-initializes the controller. This includes re-allocating I/O Submission and Completion Queues. Refer to section 7.6.1.

The process for a firmware update to be activated without a reset is:

1. The host issues a Firmware Image Download command to download the firmware image to the controller. There may be multiple portions of the firmware image to download, thus the offset for each portion of the firmware image being downloaded is specified in the Firmware Image Download command. The data provided in the Firmware Image Download command should conform to the Firmware Update Granularity indicated in the Identify Controller data structure or the firmware update may fail;
2. The host submits a Firmware Commit command with a Commit Action of 011b which specifies that the image should be activated immediately without reset. The downloaded image should replace the image in the firmware slot. If no image was downloaded since the last reset or Firmware Commit command, (i.e., the first step was skipped), then the controller shall verify and activate the image in the specified slot. If the controller starts to activate the firmware, any controllers affected by the new firmware send a Firmware Activation Starting asynchronous event to the host if Firmware Activation Notices are enabled (refer to Figure 291):
    a. The Firmware Commit command may also be used to activate a firmware image associated with a previously committed firmware slot;
3. The controller completes the Firmware Commit command. The following actions are taken in certain error scenarios:
    a. If the firmware image is invalid, then the controller reports the appropriate error (e.g., Invalid Firmware Image);
    b. If the firmware activation was not successful because a Controller Level Reset is required to activate this firmware, then the controller reports an error of Firmware Activation Requires Controller Level Reset and the image is applied at the next Controller Level Reset;

c. If the firmware activation was not successful because an NVM Subsystem Reset is required to activate this firmware, then the controller reports an error of Firmware Activation Requires NVM Subsystem Reset and the image is applied at the next NVM Subsystem Reset;
d. If the firmware activation was not successful because a Conventional Reset is required to activate this firmware, then the controller reports an error of Firmware Activation Requires Conventional Reset and the image is applied at the next Conventional Reset; and
e. If the firmware activation was not successful because the firmware activation time would exceed the MTFA value reported in the Identify Controller data structure, then the controller reports an error of Firmware Activation Requires Maximum Time Violation. In this case, to activate the firmware, the Firmware Commit command needs to be re-issued and the image activated using a reset.

If the controller transitions to the $D3_{cold}$ state (refer to the PCI Express Base Specification) after the submission of a Firmware Commit command that attempts to activate a firmware image and before the completion of that command, then the controller may resume operation with either the firmware image active at the time the Firmware Commit command was submitted or the firmware image that was activated by that command.

If the firmware is not able to be successfully loaded, then the controller shall revert to the firmware image present in the most recently activated firmware slot or the baseline read-only firmware image, if available, and indicate the failure as an asynchronous event with a Firmware Image Load Error.

If a host overwrites (i.e., updates) the firmware in the active firmware slot, then the previously active firmware image may no longer be available. As a result, any action (e.g., power cycling the controller) that requires the use of that firmware slot may instead use the firmware image that is currently in that firmware slot.

Host software should not update multiple firmware images simultaneously. After downloading an image, host software issues a Firmware Commit command before downloading additional firmware images. Processing of the first Firmware Download command after completion of a Firmware Commit command shall cause the controller to discard remaining portions, if any, of downloaded images. If a reset occurs between a firmware download and completion of the Firmware Commit command, then the controller shall discard all portion(s), if any, of downloaded images.

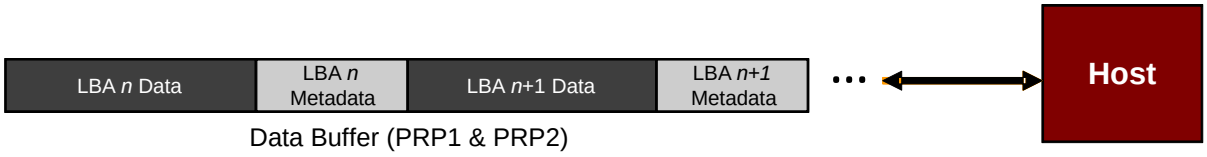
8.2 Metadata Handling

The controller may support metadata per logical block. Metadata is additional data allocated on a per logical block basis. There is no requirement for how the host makes use of the metadata area. One of the most common usages for metadata is to convey end-to-end protection information.

The metadata may be transferred by the controller to or from the host in one of two ways. The mechanism used is selected when the namespace is formatted.

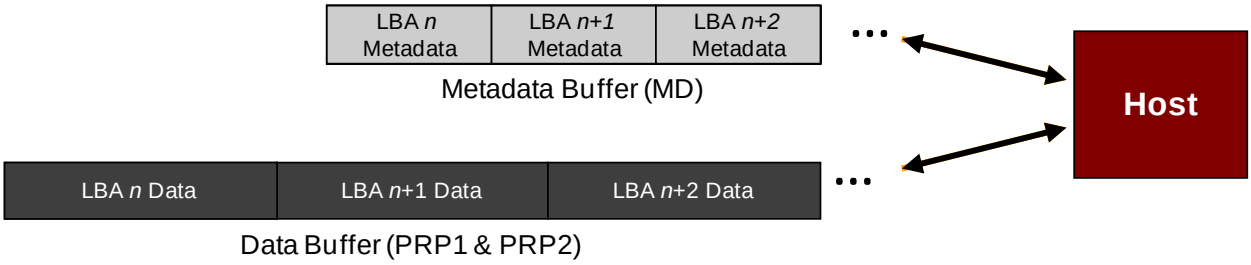
The first mechanism for transferring the metadata is as a contiguous part of the logical block that the metadata is associated with. The metadata is transferred at the end of the associated logical block, forming an extended logical block. This mechanism is illustrated in Figure 453. In this case, both the logical block data and logical block metadata are pointed to by the PRP1 and PRP2 pointers (or SGL Entry 1 if SGLs are used).

Figure 453: Metadata – Contiguous with LBA Data, Forming Extended LBA



The second mechanism for transferring the metadata is as a separate buffer of data. This mechanism is illustrated in Figure 454. In this case, the metadata is pointed to with the Metadata Pointer, while the logical block data is pointed to by the Data Pointer. When a command uses PRPs for the metadata in the command, the metadata is required to be physically contiguous. When a command uses SGLs for the metadata in the command, the metadata is not required to be physically contiguous.

Figure 454: Metadata – Transferred as Separate Buffer



One of the transfer mechanisms shall be selected for each namespace when the namespace is formatted; transferring a portion of metadata with one mechanism and a portion with the other mechanism is not supported.

If end-to-end data protection is used, then the Protection Information field for each logical block is contained in the metadata.

8.3 End-to-end Data Protection (Optional)

To provide robust data protection from the application to the NVM media and back to the application itself, end-to-end data protection may be used. If this optional mechanism is enabled, then additional protection information (e.g., CRC) is added to the logical block that may be evaluated by the controller and/or host software to determine the integrity of the logical block. This additional protection information, if present, is either the first eight bytes of metadata or the last eight bytes of metadata, based on the format of the namespace. For metadata formats with more than eight bytes, if the protection information is contained within the first eight bytes of metadata, then the CRC does not cover any metadata bytes. For metadata formats with more than eight bytes, if the protection information is contained within the last eight bytes of metadata, then the CRC covers all metadata bytes up to but excluding these last eight bytes. As described in section 8.2, metadata and hence this protection information may be configured to be contiguous with the logical block data or stored in a separate buffer.

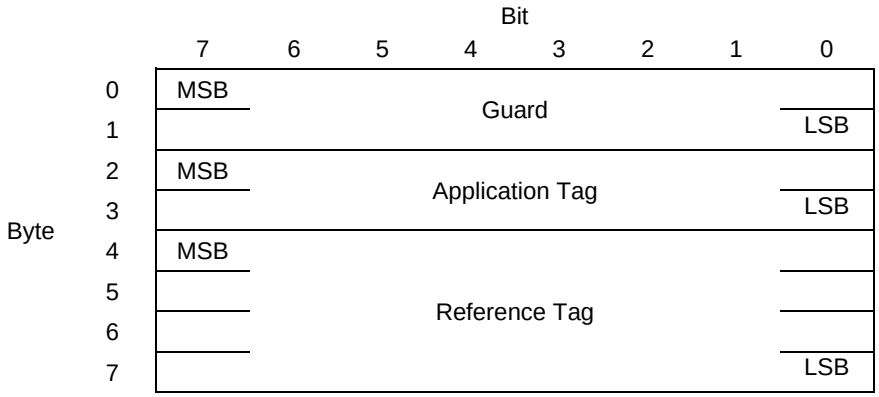
The most commonly used data protection mechanisms in Enterprise implementations are SCSI Protection Information, commonly known as Data Integrity Field (DIF), and the Data Integrity Extension (DIX). The primary difference between these two mechanisms is the location of the protection information. In DIF, the protection information is contiguous with the logical block data and creates an extended logical block, while in DIX, the protection information is stored in a separate buffer. The end-to-end data protection mechanism defined by this specification is functionally compatible with both DIF and DIX. DIF functionality is achieved by configuring the metadata to be contiguous with logical block data (as shown in Figure 453), while DIX functionality is achieved by configuring the metadata and data to be in separate buffers (as shown in Figure 454).

The NVM Express interface supports the same end-to-end protection types defined in the SCSI Protection information model specified in SBC-3. The type of end-to-end data protection (i.e., Type 1, Type 2, or Type 3) is selected when a namespace is formatted and is reported in the Identify Namespace data structure (refer to Figure 249).

The Protection Information format is shown in Figure 455 and is contained in the metadata associated with each logical block. The Guard field contains a CRC-16 computed over the logical block data. The formula used to calculate the CRC-16 is defined in SBC-3. In addition to a CRC-16, DIX also specifies an optional

IP checksum that is not supported by the NVM Express interface. The Application Tag is an opaque data field not interpreted by the controller and that may be used to disable checking of protection information. The Reference Tag associates logical block data with an address and protects against misdirected or out-of-order logical block transfer. Like the Application Tag, the Reference Tag may also be used to disable checking of protection information.

Figure 455: Protection Information Format



8.3.1 PRACT Bit

The protection information processing performed as a side effect of Read and Write commands is controlled by the Protection Information Action (PRACT) bit in the command.

8.3.1.1 Protection Information and Write Commands

Figure 456 provides some examples of the protection information processing that may occur as a side effect of a Write command.

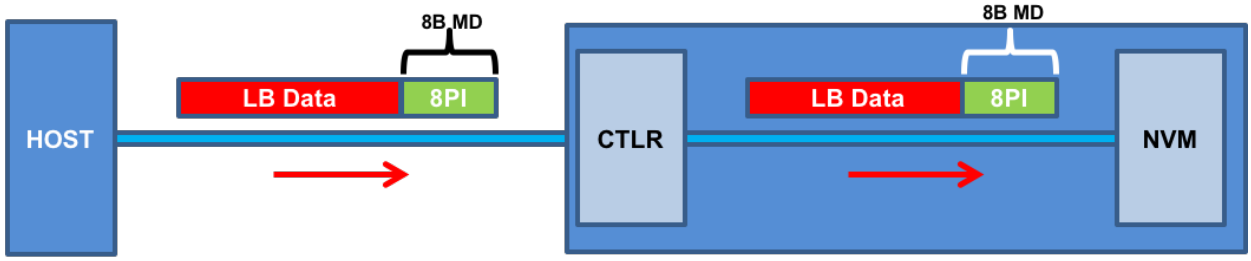
If the namespace is not formatted with end-to-end data protection, then logical block data and metadata is transferred from the host to the NVM with no protection information related processing by the controller.

If the namespace is formatted with protection information and the PRACT bit is cleared to ‘0’, then logical block data and metadata, which contains the protection information and may contain additional metadata, are transferred from the host buffer to NVM (i.e., the metadata field remains the same size in the NVM and the host buffer). As the logical block data and metadata passes through the controller, the protection information is checked. If a protection information check error is detected, the command completes with the status code of the error detected (i.e., End-to-end Guard Check Error, End-to-end Application Tag Check Error, or End-to-end Reference Tag Check Error).

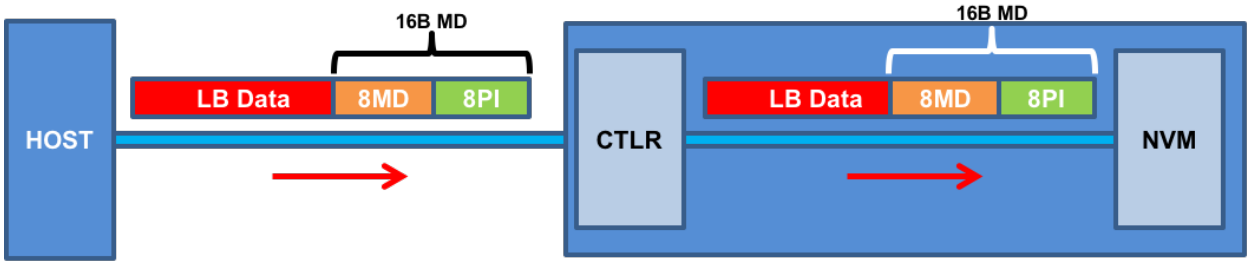
If the namespace is formatted with protection information and the PRACT bit is set to ‘1’, then:

1. If the namespace is formatted with Metadata Size equal to 8 (refer to Figure 250), then the logical block data is transferred from the host buffer to the controller. As the logical block data passes through the controller, the controller generates and appends protection information to the end of the logical block data, and the logical block data and protection information are written to NVM (i.e., the metadata is not resident within the host buffer); and
2. If the namespace is formatted with Metadata Size greater than 8, then the logical block data and the metadata are transferred from the host buffer to the controller. As the metadata passes through the controller, the controller overwrites the protection information portion of the metadata. The logical block data and metadata are written to the NVM (i.e., the metadata field remains the same size in the NVM and the host buffer). The location of the protection information within the metadata is configured when the namespace is formatted (refer to the DPS field in Figure 249).

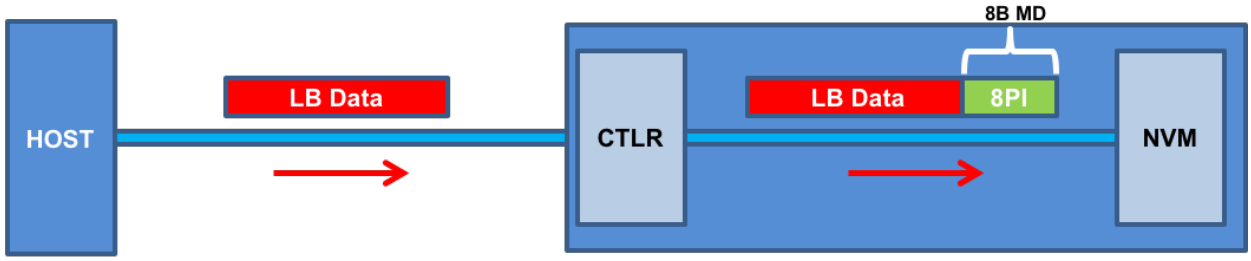
Figure 456: Write Command Protection Information Processing



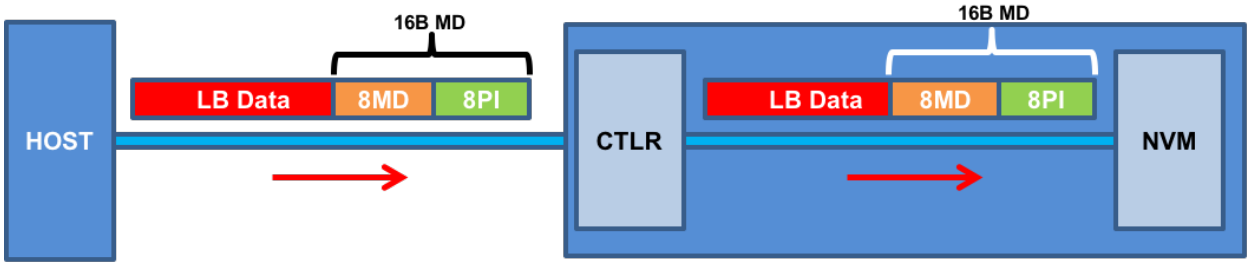
a) MD=8, PI, PRACT=0: Metadata remains same size in NVM and host buffer



b) MD>8 (e.g., 16), PI, PRACT=0: Metadata remains same size in NVM and host buffer



c) MD=8, PI, PRACT=1: Metadata not resident in host buffer



d) MD>8 (e.g., 16), PI, PRACT=1: Metadata remains same size in NVM and host buffer

NOTE: In cases (b) and (d) the Protection Information could be before or after the 8 bytes of metadata.

8.3.1.2 Protection Information and Read Commands

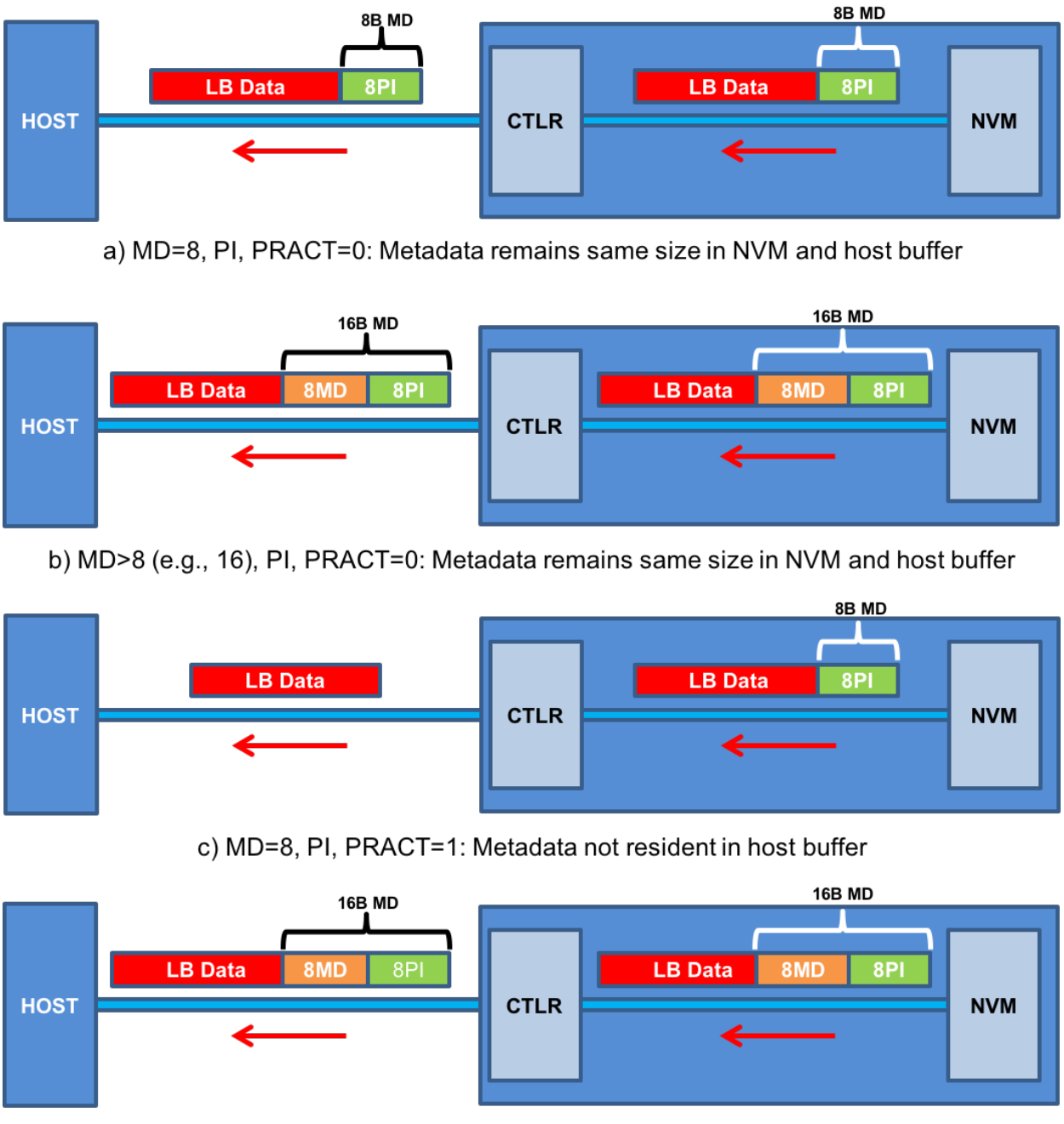
Figure 457 provides some examples of the protection information processing that may occur as a side effect of Read command processing.

If the namespace is formatted with protection information and the PRACT bit is cleared to '0', then the logical block data and metadata, which in this case contains the protection information and possibly additional host metadata, is transferred by the controller from the NVM to the host buffer (i.e., the metadata field remains the same size in the NVM and the host buffer). As the logical block data and metadata pass through the controller, the protection information within the metadata is checked. If a protection information check error is detected, the command completes with the status code of the error detected (i.e., End-to-end Guard Check Error, End-to-end Application Tag Check Error, or End-to-end Reference Tag Check Error).

If the namespace is formatted with protection information and the PRACT bit is set to '1', then:

a) if the namespace is formatted with Metadata Size equal to 8 (refer to Figure 250), the logical block data and metadata (which in this case is, by definition, the protection information)~~,~~ is read from the NVM by the controller. As the logical block and metadata pass through the controller, the protection information is checked. If a protection information check error is detected, the command completes with the status code of the error detected (i.e., End-to-end Guard Check Error, End-to-end Application Tag Check Error, or End-to-end Reference Tag Check Error). After processing the protection information, the controller only returns the logical block data to the host (i.e., the metadata is not resident within the host buffer); and
b) if the namespace is formatted with Metadata Size greater than 8, the logical block data and the metadata, which in this case contains the protection information and additional host formatted metadata, is read from the NVM by the controller. As the logical block and metadata pass through the controller, the protection information embedded within the metadata is checked. If a protection information check error is detected, the command completes with the status code of the error detected (i.e., End-to-end Guard Check Error, End-to-end Application Tag Check Error, or End-to-end Reference Tag Check Error). After processing the protection information, the controller passes the logical block data and metadata, with the embedded protection information unchanged, to the host (i.e., the metadata field remains the same size in the NVM as within the host buffer).

Figure 457: Read Command Protection Information Processing



a) MD=8, PI, PRACT=0: Metadata remains same size in NVM and host buffer

b) MD>8 (e.g., 16), PI, PRACT=0: Metadata remains same size in NVM and host buffer

c) MD=8, PI, PRACT=1: Metadata not resident in host buffer

d) MD>8 (e.g., 16), PI, PRACT=1: Metadata remains same size in NVM and host buffer

NOTE: In cases (b) and (d) the PI could be before or after the 8 bytes of metadata.

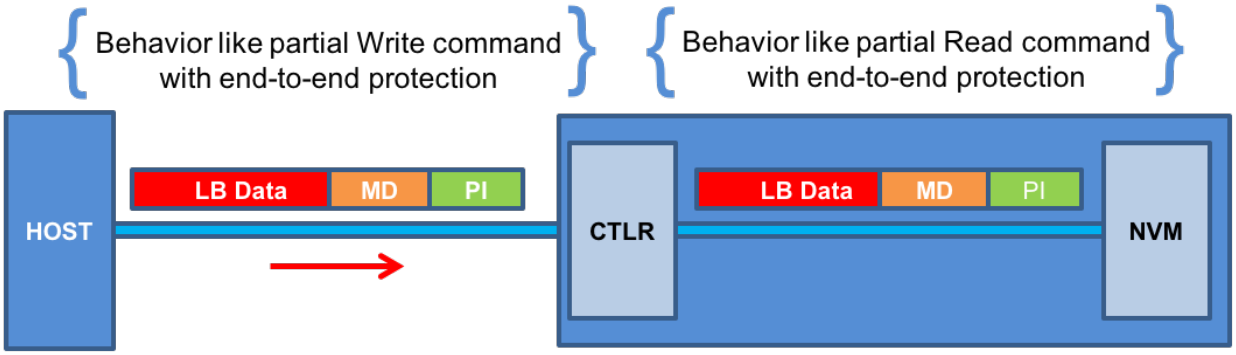
8.3.1.3 Protection Information for Fused Operations

Protection processing for fused operations is the same as those for the individual commands that make up the fused operation.

8.3.1.4 Protection Information and Compare commands

Figure 458 illustrates the protection information processing that may occur as a side effect of Compare command processing. Compare command processing parallels both Write and Read commands. For the portion of the Compare command that transfers data and protection information from the host to the controller, the protection information checks performed by the controller parallels the Write command protection information checks (refer to section 8.3.1.1). For the portion of the Compare command that transfers data and protection information from the NVM media to the controller, the protection information checks performed by the controller parallels the Read command protection information checks (refer to section 8.3.1.2).

Figure 458: Protection Information Processing for Compare



Protection Information with PRACT bit set to '0' (i.e., pass)

8.3.2 Control of Protection Information Checking (PRCHK)

Checking of protection information consists of the following operations performed by the controller.

- If bit 2 of the Protection Information Check (PRCHK) field of the command is set to '1', then the controller compares the protection information Guard field to the CRC-16 computed over the logical block data.
- If bit 1 of the PRCHK field is set to '1', then the controller compares unmasked bits in the protection information Application Tag field to the Logical Block Application Tag (LBAT) field in the command. A bit in the protection information Application Tag field is masked if the corresponding bit is cleared to '0' in the Logical Block Application Tag Mask (LBATM) field or the Expected Logical Block Application Tag Mask (ELBATM) field of the command.
- If bit 0 of the PRCHK field is set to '1' and the namespace is formatted for Type 1 or Type 2 protection, then the controller compares the protection Information Reference Tag field to the computed reference tag. The computed reference tag depends on the Protection Type:
    - If the namespace is formatted for Type 1 protection, the value of the computed reference tag for the first logical block of the command is the value contained in the Initial Logical Block Reference Tag (ILBRT) or Expected Initial Logical Block Reference Tag (EILBRT) field in the command, and the computed reference tag is incremented for each subsequent logical block. The controller shall complete the command with a status of Invalid Protection Information if the ILBRT field or the EILBRT field does not match the least significant four bytes of the SLBA field.
      Note: Unlike SCSI Protection Information Type 1 protection which implicitly uses the least significant four bytes of the LBA, the controller always uses the ILBRT or EILBRT field and requires host software to initialize the ILBRT or EILBRT field to the least significant four bytes of the LBA when Type 1 protection is used.

  - If the namespace is formatted for Type 2 protection, the value of the computed reference tag for the first logical block of the command is the value contained in the Initial Logical Block Reference Tag (ILBRT) or Expected Initial Logical Block Reference Tag (EILBRT) field in the command, and the computed reference tag is incremented for each subsequent logical block.
- If bit 0 of the PRCHK field is set to '1' and the namespace is formatted for Type 3 protection, then the controller:
  - should not compare the protection Information Reference Tag field to the computed reference tag; and
  - may ignore the ILBRT and EILBRT fields. If a command is aborted as a result of bit 0 of the PRCHK field being set to '1', then that command should be aborted with a status code of Invalid Protection Information, but may be aborted with a status code of Invalid Field in Command.

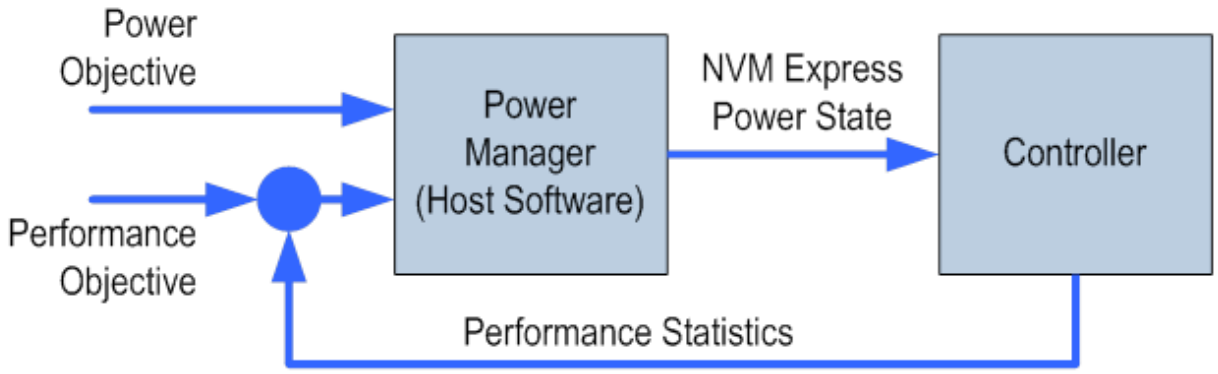
Protection checking may be disabled as a side effect of the value of the protection information Application Tag and Reference Tag fields regardless of the state of the PRCHK field in the command. If the namespace is formatted for Type 1 or Type 2 protection, then all protection information checks are disabled regardless of the state of the PRCHK field when the protection information Application Tag has a value of FFFFh. If the namespace is formatted for Type 3 protection, then all protection information checks are disabled regardless of the state of the PRCHK field when the protection information Application Tag has a value of FFFFh and the protection information Reference Tag has a value of FFFFFFFFh.

Inserted protection information consists of the computed CRC-16 in the Guard field, the LBAT field value in the Application Tag, and the computed reference tag in the Reference Tag field.

8.4 Power Management

The power management capability allows the host to manage NVM subsystem power statically or dynamically. Static power management consists of the host determining the maximum power that may be allocated to an NVM subsystem and setting the NVM Express power state to one that consumes this amount of power or less. Dynamic power management is illustrated in Figure 459 and consists of the host modifying the NVM Express power state to best satisfy changing power and performance objectives. This power management mechanism is meant to complement and not replace autonomous power management or thermal management performed by a controller.

Figure 459: Dynamic Power Management



The number of power states implemented by a controller is returned in the Number of Power States Supported (NPSS) field in the Identify Controller data structure. A controller shall support at least one power state and may optionally support up to a total of 32 power states. Power states are contiguously numbered starting with zero such that each subsequent power state consumes less than or equal to the maximum

power consumed in the previous state. Thus, power state zero indicates the maximum power that the NVM subsystem is capable of consuming.

Associated with each power state is a Power State Descriptor in the Identify Controller data structure (refer to Figure 252). The descriptors for all implemented power states may be viewed as forming a table as shown in the example in Figure 460 for a controller with seven implemented power states. Note that Figure 460 is illustrative and does not include all fields in the power state descriptor. The Maximum Power (MP) field indicates the sustained maximum power that may be consumed in that state, where power measurement methods are outside the scope of this specification. The controller may employ autonomous power management techniques to reduce power consumption below this level, but under no circumstances is power allowed to exceed this level except for non-operational power states as described in section 8.4.1.

Figure 460: Example Power State Descriptor Table

Power State	Maximum Power (MP)	Entry Latency (ENTLAT)	Exit Latency (EXLAT)	Relative Read Throughput (RRT)	Relative Read Latency (RRL)	Relative Write Throughput (RWT)	Relative Write Latency (RWL)
0	25 W	5 µs	5 µs	0	0	0	0
1	18 W	5 µs	7 µs	0	0	1	0
2	18 W	5 µs	8 µs	1	0	0	0
3	15 W	20 µs	15 µs	2	0	2	0
4	10 W	20 µs	30 µs	1	1	3	0
5	8 W	50 µs	50 µs	2	2	4	0
6	5 W	20 µs	5,000 µs	4	3	5	1

The Idle Power (IDLP) field indicates the typical power consumed by the NVM subsystem over 30 seconds in the power state when idle (i.e., there are no pending commands register accesses, background processes, nor device self-test operations). The measurement starts after the NVM subsystem has been idle for 10 seconds.

The Active Power (ACTP) field indicates the largest average power of the NVM subsystem over a 10 second window on a particular workload (refer to section 8.4.3). Active Power measurement starts when the first command is submitted and ends when the last command is completed. The largest average power over a 10 second window, consumed by the NVM subsystem in that state is reported in the Active Power field. If the workload completes faster than 10 seconds, the average active power should be measured over the period of the workload. Non-operational states shall set Active Power Scale, Active Power Workload, and Active Power fields to 0h.

The host may dynamically modify the power state using the Set Features command and determine the current power state using the Get Features command. The host may directly transition between any two supported power states. The Entry Latency (ENTLAT) field in the Power State Descriptor data structure indicates the maximum amount of time in microseconds to enter that power state and the Exit Latency (EXLAT) field indicates the maximum amount of time in microseconds to exit that state.

The maximum amount of time to transition between any two power states is equal to the sum of the old state's exit latency and the new state's entry latency. The host is not required to wait for a previously submitted power state transition to complete before initiating a new transition. The maximum amount of time for a sequence of power state transitions to complete is equal to the sum of transition times for each individual power state transition in the sequence.

Associated with each power state descriptor are Relative Read Throughput (RRT), Relative Write Throughput (RWT), Relative Read Latency (RRL) and Relative Write Latency (RWL) fields that provide the host with an indication of relative performance in that power state. Relative performance values provide an ordering of performance characteristics between power states. Relative performance values may repeat, may be skipped, and may be assigned in any order (i.e., increasing power states are not required to have increasing relative performance values).

A lower relative performance value indicates better performance (e.g., higher throughput or lower latency). For example, in Figure 460 power state 1 has higher read throughput than power state 2, and power states 0 through 3 all have the same read latency. Relative performance ordering is only with respect to a single performance characteristic. Thus, although the relative read throughput value of one power state may equal the relative write throughput value of another power state, this does not imply that the actual read and write performance of these two power states are equal.

The default NVM Express power state is implementation specific and shall correspond to a state that does not consume more power than the lowest value specified in the form factor specification used by the PCI Express SSD. The host shall never select a power state that consumes more power than the PCI Express slot power limit control value expressed by the Captured Slot Power Limit Value (CSPLV) and Captured Slot Power Limit Scale (CSPLS) fields of the PCI Express Device Capabilities (PXDCAP) register. Hosts that do not dynamically manage power should set the power state to the lowest numbered state that satisfies the PCI Express slot power limit control value.

If a controller implements the PCI Express Dynamic Power Allocation (DPA) capability and that capability is enabled (i.e., the Substate Control Enable bit is set to '1'), then the maximum power that may be consumed by the NVM subsystem is equal to the minimum value specified by the DPA substate or the NVM Express power state, whichever is lower.

8.4.1 Non-Operational Power States

A power state may be a non-operational power state, as indicated by Non-Operational State (NOPS) field in Figure 252. In a non-operational power state, memory-mapped I/O (MMIO) accesses, configuration register accesses and Admin Queue commands are serviced. No I/O commands are processed by the controller while in a non-operational power state. The host should wait until there are no pending I/O commands prior to issuing a Set Features command to change the current power state of the device to a non-operational power state, and not submit new I/O commands until the Set Features command completes. Issuing an I/O command in parallel may result in the controller being in an unexpected power state.

When in a non-operational power state, regardless of whether autonomous power state transitions are enabled, the controller shall autonomously transition back to the most recent operational power state when an I/O Submission Queue Tail Doorbell is written.

While in a non-operational state, a controller may exceed the power advertised by the state for the following purposes:

- servicing a memory-mapped I/O (MMIO) or configuration register access (e.g., Controller Configuration (refer to section 3.1.5));
- processing a command submitted to the Admin Submission Queue and processing background operations, if any, initiated by that command (e.g., Device Self-test command (refer to section 5.8), Sanitize command (refer to section 5.24)); or
- if Non-Operational Power State Permissive Mode is supported and enabled, executing controller initiated background operations (refer to section 5.21.1.17).

For all of the cases in the preceding paragraph, the controller shall:

- logically remain in the current non-operational power state unless an I/O command is received or if an explicit transition is requested by a Set Features command with the Power Management identifier; and
- not exceed the maximum power advertised for the most recent operational power state.

8.4.2 Autonomous Power State Transitions

The controller may support autonomous power state transitions, as indicated in the Identify Controller data structure in Figure 251. Autonomous power state transitions provide a mechanism for the host to configure the controller to automatically transition between power states on certain conditions without software intervention.

The entry condition to transition to the Idle Transition Power State is that the controller has been in idle for a continuous period of time exceeding the Idle Time Prior to Transition time specified. The controller is idle when there are no commands outstanding to any I/O Submission Queue. If a controller has an operation in process (e.g., device self-test operation) that would cause controller power to exceed that advertised for the proposed non-operational power state, then the controller should not autonomously transition to that state.

The power state to transition to shall be a non-operational power state (a non-operational power state may autonomously transition to another non-operational power state). If an operational power state is specified, then the controller should abort the command with a status of Invalid Field in Command. Refer to section 8.4.1 for more details.

8.4.3 NVM Subsystem Workloads

The workload values described in this section may specify a workload hint in the Power Management Feature (refer to section 5.21.1.2) to inform the NVM subsystem or indicate the conditions for the active power level.

Active power values in the power state descriptors are specified for a particular workload since they may vary based on the workload of the NVM subsystem. The workload field indicates the conditions to observe the energy values. If Active Power is indicated for a power state, a corresponding workload shall also be indicated.

The workload values are described in Figure 461.

Figure 461: Workload Hints

Value	Description
000b	**No Workload:** The workload is unknown or not provided.
001b	**Workload #1:** Extended Idle Period with a Burst of Random Writes. Workload #1 consists of five (5) minutes of idle followed by thirty-two (32) random write commands of size 1 MiB submitted to a single controller while all other controllers in the NVM subsystem are idle, and then thirty (30) seconds of idle.
010b	**Workload #2:** Heavy Sequential Writes. Workload #2 consists of 80,000 sequential write commands of size 128 KiB submitted to a single controller while all other controllers in the NVM subsystem are idle. The submission queue(s) should be sufficiently large allowing the host to ensure there are multiple commands pending at all times during the workload.
011b to 111b	Reserved

8.4.4 Runtime D3 Transitions

In Runtime D3 (RTD3) main power is removed from the controller. Auxiliary power may or may not be provided. RTD3 is used for additional power savings when the controller is expected to be idle for a period of time.

To enable host software to determine when to use RTD3, the controller reports the latency to enter RTD3 and the latency to resume from RTD3 in the Identify Controller data structure in Figure 251. The host may use the sum of these two values to evaluate whether the expected idle period is long enough to benefit from a transition to RTD3.

The RTD3 Resume Latency is the expected elapsed time from the time power is applied until the controller is able to:

a) process and complete I/O commands; and
b) access the NVM associated with attached namespace(s), if any, as part of I/O command processing.

The latency reported is based on a normal shutdown with optimal controller settings preceding the RTD3 resume. The latency reported assumes that host software enables and initializes the controller and sends a 4 KiB read operation.

The RTD3 Entry Latency is the expected elapsed time from the time CC.SHN is set to 01b by host software until CSTS.SHST is set to 10b by the controller. When CSTS.SHST is set to 10b, it is safe for host software to remove power from the controller.

In this specification, RTD3 refers to the $D3_{cold}$ power state described in the PCI Express specification. RTD3 does not include the PCI Express $D3_{hot}$ power state because main power is not removed from the controller in the $D3_{hot}$ power state. Refer to the PCI Express Base Specification for details on the $D3_{hot}$ power state and the $D3_{cold}$ power state.

8.4.5 Host Controlled Thermal Management

A controller may support host controlled thermal management (HCTM), as indicated in the Host Controlled Thermal Management Attributes of the Identify Controller data structure in Figure 251. Host controlled thermal management provides a mechanism for the host to configure a controller to automatically transition between active power states or perform vendor specific thermal management actions in order to attempt to meet thermal management requirements specified by the host. If active power states transitions are used to attempt to meet these thermal management requirements specified by the host, then those active power states transitions are vendor specific.

The host specifies and enables the thermal management requirements by setting the Thermal Management Temperature 1 field and/or Thermal Management Temperature 2 field (refer to section 5.21.1.16) in a Set Features command to a non-zero value. The supported range of values for the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field are indicated in the Identify Controller data structure in Figure 251.

The Thermal Management Temperature 1 specifies that if the Composite Temperature (refer to Figure 199) is:

a) at or above this value; and
b) less than the Thermal Management Temperature 2, if non-zero,

then the controller should start transitioning to lower power active power states or perform vendor specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature (e.g., transition to an active power state that performs light throttling).

The Thermal Management Temperature 2 field specifies that if the Composite Temperature is at or above this value, then the controller shall start transitioning to lower power active power states or perform vendor specific thermal management actions regardless of the impact on performance in order to attempt to reduce the Composite Temperature (e.g., transition to an active power state that performs heavy throttling).

If the controller is currently in a lower power active power state or performing vendor specific thermal management actions because of this feature (e.g., throttling performance) because the Composite Temperature:

a) is at or above the current value of the Thermal Management Temperature 1 field; and
b) is below the current value of the Thermal Management Temperature 2 field,

and the Composite Temperature decreases to a value below the current value of the Thermal Management Temperature 1 field, then the controller should return to the active power state that the controller was in prior to going to a lower power active power state or stop performing vendor specific thermal management actions because of this feature, the Composite Temperature and the current value of the Thermal Management Temperature 1 field.

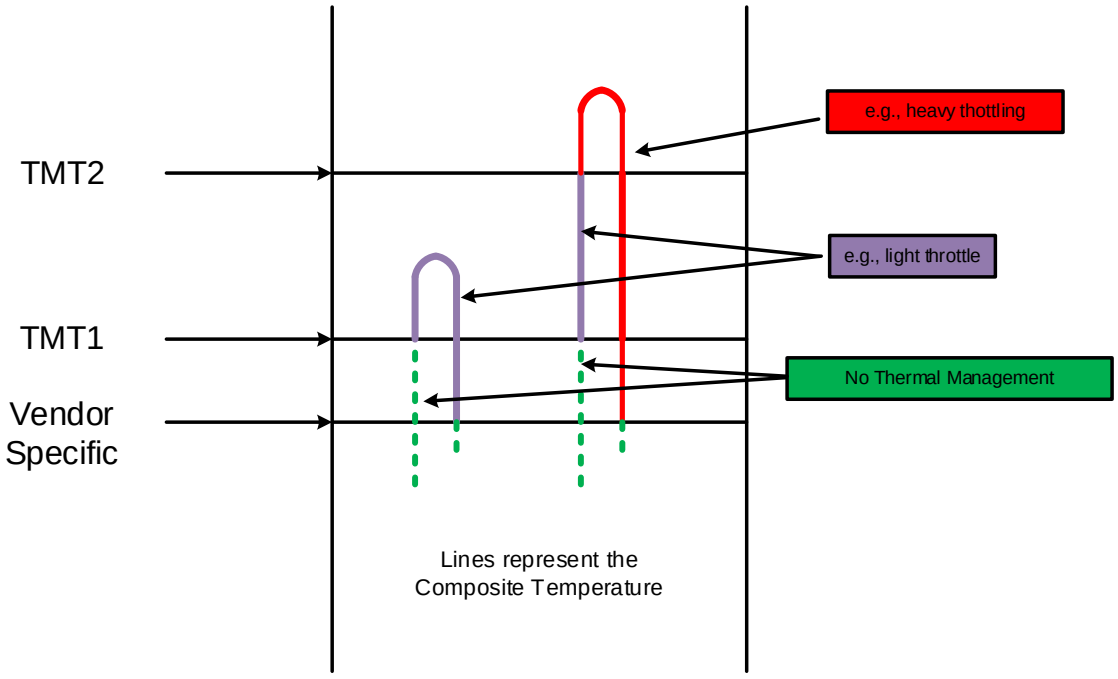
If the controller is currently in a lower power active power state or performing vendor specific thermal management actions because the Composite Temperature is at or above the current value of the Thermal Management Temperature 2 field and the Composite Temperature decreases to below the current value of the Thermal Management Temperature 1 field, then the controller should return to the active power state

that the controller was in prior to going to a lower power active power state or stop performing vendor specific thermal management actions because of this feature, and the Composite Temperature.

The temperature at which the controller stops being in a lower power active power state or performing vendor specific thermal management actions because of this feature is vendor specific (i.e., hysteresis is vendor specific).

Figure 462 shows examples of how the Composite Temperature may be effected by this feature.

Figure 462: HCTM Example



Note: Since the host controlled thermal management (HCTM) feature uses the Composite Temperature, the actual interactions between a platform (e.g., tablet, or laptop) and two different device implementations may vary even with the same Thermal Management Temperature 1 and Thermal Management Temperature 2 temperature settings. The use of this feature requires validation between those devices implementations and the platform in order to be used effectively.

8.5 Virtualization Enhancements (Optional)

Virtualized environments may use an NVM subsystem with multiple controllers to provide virtual or physical hosts direct I/O access. The NVM subsystem is composed of primary controller(s) and secondary controller(s), where the secondary controller(s) depend on primary controller(s) for dynamically assigned resources. A host may issue the Identify command to a primary controller specifying the Secondary Controller List to discover the secondary controllers associated with that primary controller.

Controller resources may be assigned or removed from a controller using the Virtualization Management command issued to a primary controller. The following types of controller resources are defined:

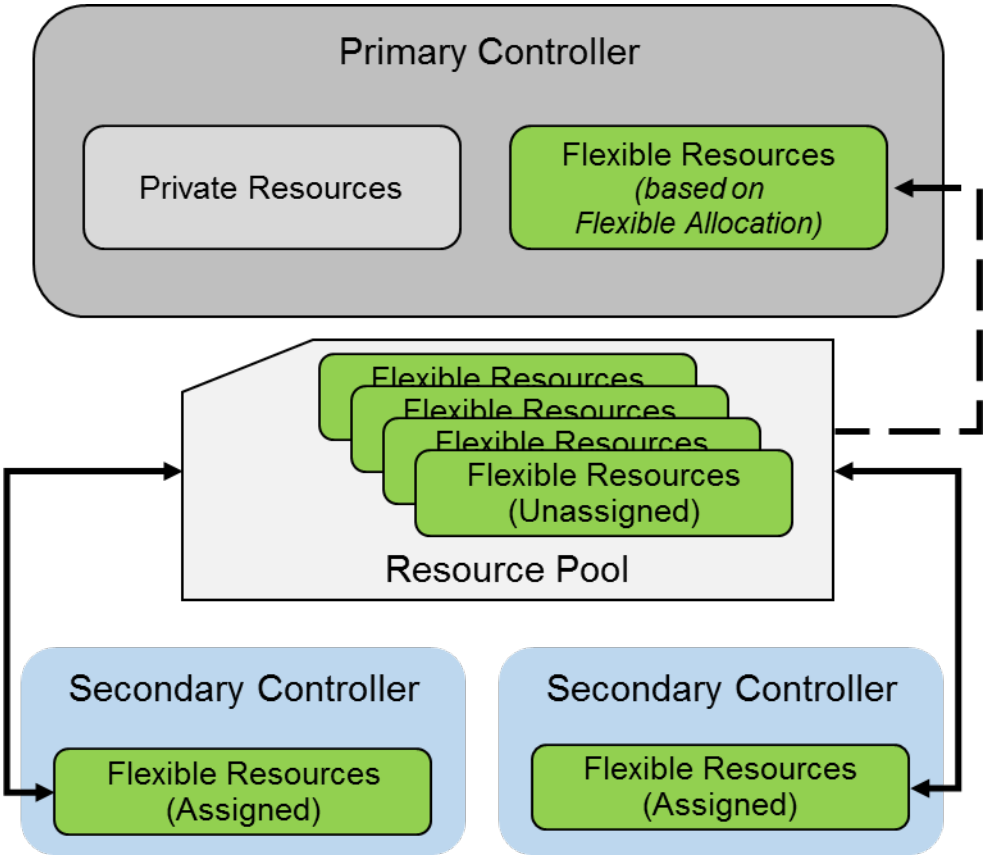
- Virtual Queue Resource (VQ Resource): a type of controller resource that manages one Submission Queue (SQ) and one Completion Queue (CQ) (refer to section 8.5.1); and
- Virtual Interrupt Resource (VI Resource): a type of controller resource that manages one interrupt vector (refer to section 8.5.2).

Flexible Resources are controller resources that may be assigned to the primary controller or one of its secondary controllers. The Virtualization Management command is used to provision the Flexible Resources between a primary controller and one of its secondary controller(s). A primary controller's allocation of Flexible Resources may be modified using the Virtualization Management command and the change takes effect after any Controller Level Reset other than a Controller Reset (i.e., CC.EN transitions from '1' to '0'). A secondary controller only supports having Flexible Resources assigned or removed when in the Offline state.

Private Resources are controller resources that are permanently assigned to a primary or secondary controller. These resources are not supported by the Virtualization Management command.

The primary controller is allowed to have a mix of Private and Flexible Resources for a particular controller resource type. If there is a mix, then the Private Resources occupy the lower contiguous range of resource identifiers starting with 0. Secondary controllers shall have all Private or all Flexible Resources for a particular resource type. Controller resources assigned to a secondary controller always occupy a contiguous range of identifiers with no gaps, starting with 0. If a particular controller resource type is supported as indicated in the Controller Resource Types field of the Primary Controller Capabilities Structure, then all secondary controllers shall have that controller resource type assigned as a Flexible Resource. Figure 463 shows the controller resource allocation model for a controller resource type that is assignable as a Flexible Resource.

Figure 463: Controller Resource Allocation



For each controller resource type supported, the Primary Controller Capabilities Structure (refer to Figure 256) defines:

- The total number of Flexible Resources;
- The total number of Private Resources for the primary controller;
- The maximum number of Flexible Resources that may be assigned to a secondary controller using the Virtualization Management command; and
- The assignment of resources to the primary controller.

Primary and secondary controllers may implement all features of this specification, except where commands are defined as being only supported by a primary controller. It is recommended that only primary controllers support the privileged actions described in section 7.14 so that untrusted hosts using secondary controllers do not impact the entire NVM subsystem state.

The Secondary Controller List structure returned by the Identify command is used to determine the topology of secondary controllers and the resources assigned. The secondary controller shall be in the Offline state to configure resources. The Virtualization Management command is used to transition the secondary controller between the Online state and the Offline state. Refer to section 8.5.3 for details on the Online and Offline states.

To support the Virtualization Enhancements capability, the NVM subsystem shall support the following:

- One or more primary controllers, each of which supports:
  - One or more secondary controllers;
  - A pool of unassigned Flexible Resources that supports allocation to a primary controller and dynamic assignment to its associated secondary controllers;
  - Two or more Private Resource queue pairs;
  - Indicate support for the Virtualization Management command in the Optional Admin Command Support (OACS) field in the Identify Controller data structure;
  - The Virtualization Management command;
  - The Primary Controller Capabilities Structure defined in Figure 256 (Identify command with CNS value of 14h);
  - The Secondary Controller List defined in Figure 257 (Identify command with CNS value of 15h); and
  - The Namespace Management capability (refer to section 8.12);
- One or more secondary controllers; and
- Flexible Resources, each of which supports all of the following:
  - Assignment and removal by exactly one primary controller; and
  - Assignment to no more than one controller at a time.

Within an NVM subsystem that supports both the Virtualization Enhancements capability and SR-IOV (refer to section 8.5.4), all controllers that are SR-IOV PFs shall be primary controllers, and all controllers that are SR-IOV VFs shall be secondary controllers of their associated PFs.

8.5.1 VQ Resource Definition

A Virtual Queue Resource (VQ Resource) is a type of controller resource that manages one CQ and one SQ. For a VQ Resource that is assigned to a controller, its resource identifier is equivalent to its Queue Identifier.

The Controller Resource Types field of the Primary Controller Capabilities Structure indicates whether VQ Resources are supported. If VQ Resources are unsupported, a primary controller and its associated secondary controllers have all queues as Private Resources. The rest of this section assumes that VQ Resources are supported.

The secondary controller is assigned VQ Resources using the Virtualization Management command. The number of VQ Resources assigned is discoverable in the Secondary Controller List entry for the associated

secondary controller. The number of VQ Resources assigned may also be discovered using the Get Features command with the Number of Queues Feature identifier (refer to section 5.21.1.7).

If a secondary controller has no assigned VQ Resources, then that controller remains in the Offline state. A secondary controller is not able to transition to the Online state until VQ Resources for an Admin Queue and one or more I/O Queues have been assigned to that controller (i.e., the minimum number of VQ Resources that may be assigned is two).

A primary controller that supports VQ Resources shall have at least two queue pairs that are Private Resources to ensure there is a minimum of an Admin Queue pair and one I/O queue pair for the primary controller at all times. A primary controller may be allocated VQ Resources using the Primary Controller Flexible Allocation action of the Virtualization Management command. The VQ resources allocated take effect after a Controller Level Reset and are persistent across power cycles and resets. The number of VQ Resources currently allocated is discoverable in the Primary Controller Capabilities Structure. The number of VQ Resources currently allocated may also be discovered using the Get Features command with the Number of Queues Feature identifier (refer to section 5.21.1.7).

8.5.2 VI Resource Definition

A Virtual Interrupt Resource (VI Resource) is a type of controller resource that manages one interrupt vector, such as an MSI-X vector. For a VI Resource that is assigned to a controller, its resource identifier is equivalent to its interrupt vector number.

The Controller Resource Types field of the Primary Controller Capabilities Structure indicates whether VI Resources are supported. If VI Resources are unsupported, a primary controller and its associated secondary controllers have all interrupts as Private Resources. The rest of this section assumes that VI Resources are supported.

The secondary controller is assigned VI Resources using the Virtualization Management command. The number of VI Resources assigned is discoverable in the Secondary Controller List entry for the associated secondary controller.

While a primary controller and/or its associated secondary controllers may concurrently support multiple types of interrupt vectors (e.g., MSI and MSI-X), all the controllers' VI Resources shall contain interrupt resources for interrupt vectors of the same type. In this revision, MSI-X is the only supported type of VI Resource.

For a secondary controller that supports VI Resources with MSI-X vectors, if at least one VI Resource is assigned to that controller, MSIXCAP.MXC.TS (refer to section 2.4.2) indicates the number of VI Resources assigned to the controller. Since MSIXCAP.MXC.TS is read-only, the value shall only be updated when the secondary controller is in the Offline state. MSI-X Table Entries on the secondary controller for newly assigned VI Resources shall be reset to default values.

If a secondary controller that supports VI Resources has no assigned VI Resources, then that controller remains in the Offline state. A secondary controller is not able to transition to the Online state until a VI Resource for interrupt vector 0 has been assigned to that controller. For a secondary controller that supports VI Resources with MSI-X vectors, if no VI Resources are assigned to that controller, then MSIXCAP.MXC.TS is reserved.

A primary controller that supports VI Resources shall have at least one interrupt that is a Private Resource. Interrupt vector 0 is always assigned to the primary controller. A primary controller may be allocated VI Resources using the Primary Controller Flexible Allocation action of the Virtualization Management command. The VI resources allocated take effect after a Controller Level Reset and are persistent across power cycles and resets. The number of VI Resources currently allocated is discoverable in the Primary Controller Capabilities Structure. For a primary controller that supports VI Resources with MSI-X vectors, MSIXCAP.MXC.TS indicates an MSI-X Table size equal to the total number of Private Resources and the Flexible Resources currently allocated following a Controller Level Reset.

When an I/O CQ is created, the controller supports mapping that I/O CQ to any valid interrupt vector, regardless of whether they have the same resource identifier, as long as the I/O CQ and the interrupt vector are attached to the same controller.

8.5.3 Secondary Controller States and Resource Configuration

A secondary controller shall be in one of the following states:

- **Online:** The secondary controller may be in use by a host. Required resources have been assigned. The secondary controller may be enabled in this state (CC.EN may be set to '1' and CSTS.RDY may then transition to '1'); or
- **Offline:** The secondary controller may not be used by a host. CSTS.CFS shall be set to '1'. Controller registers other than CSTS are undefined in this state.

The host may request a transition to the Online or Offline state using the Virtualization Management command. When a secondary controller transitions from the Online state to the Offline state all Flexible Resources are removed from the secondary controller.

To ensure that the host accurately detects capabilities of the secondary controller, the host should complete the following procedure to bring a secondary controller Online:

1. Use the Virtualization Management command to set the secondary controller to the Offline state;
2. Use the Virtualization Management command to assign VQ resources and VI resources;
3. Perform a Controller Level Reset. If the secondary controller is a VF, then this should be a VF Function Level Reset; and
4. Use the Virtualization Management command to set the secondary controller to the Online state.

If VI Resources are supported, then following this process ensures the MSI-X Table size indicated by MSIXCAP.MXC.TS is updated to reflect the appropriate number of VI Resources before the transition to the Online state.

A primary controller or secondary controller is enabled when CC.EN and CSTS.RDY are both set to '1' for that controller. A secondary controller is able to be enabled only when in the Online state. If the primary controller associated with a secondary controller is disabled or undergoes a Controller Level Reset, then the secondary controller shall implicitly transition to the Offline state.

Resources shall only be assigned to a secondary controller when in the Offline state. If the minimum number of resources are not assigned to a secondary controller, then a request to transition to the Online state shall fail for that secondary controller. For implementations that support SR-IOV, if VF Enable is cleared to '0' or NumVFs specifies a value that does not enable the associated secondary controller, then the secondary controller shall implicitly transition to the Offline state.

8.5.4 Single Root I/O Virtualization and Sharing (SR-IOV)

The PCI-SIG® Single Root I/O Virtualization and Sharing Specification (SR-IOV) defines extensions to PCI Express that allow multiple System Images (SIs), such as virtual machines running on a hypervisor, to share PCI hardware resources. The primary benefit of SR-IOV is that it eliminates the hypervisor from participating in I/O operations which may be a significant factor limiting storage performance in some virtualized environments and allows direct SI access to PCI hardware resources.

A Physical Function (PF) is a PCI Express Function that supports the SR-IOV Capability, which in turn allows that PF to support one or more dependent Virtual Functions (VFs). These PFs and VFs may support NVM Express controllers that share an underlying NVM subsystem with multi-path I/O and namespace sharing capabilities (refer to section 1.4.1).

SR-IOV Virtual Functions (VFs) with an NVM Express Class Code (refer to section 2.1.5) shall implement fully compliant NVM Express controllers. This ensures that the same host software developed for non-virtualized environments is capable of running unmodified within an SI.

For hosts where SR-IOV is unsupported or not needed, a controller that is a PF shall support operation as a stand-alone controller.

For a controller that is a PF, the requirements for SR-IOV Capability registers VF BAR0, VF BAR1, VF BAR2, VF BAR4, and VF BAR5 are the same as the requirements for PCI registers BAR0, BAR1, BAR4, and BAR5, respectively, as specified in sections 2.1.10, 2.1.11, 2.1.14, and 2.1.15. For a controller that is a PF, SR-IOV Capability register VF BAR2 shall not support Index/Data Pair (refer to section 2.1.12).

To accommodate SR-IOV address range isolation requirements, VF BAR2 and VF BAR3 may support a 64-bit prefetchable memory register space which shall only be used for MSI-X Tables and MSI-X PBAs of VFs. MSI-X Table BIR = '2' (refer to section 2.4.3) and MSI-X PBA BIR = '2' (refer to section 2.4.4) are valid for controllers that are VFs.

While the controller registers of a controller that is a VF are accessible only if SR-IOV Control.VF MSE is set to '1', clearing VF MSE from '1' to '0' does not cause a reset of that controller. In this case, controller registers are hidden, but their values are not reset.

8.6 Doorbell Stride for Software Emulation

The doorbell stride, specified in CAP.DSTRD, may be used to separate doorbells by a number of bytes in memory space. The doorbell stride is a number of bytes equal to (2 ^ (2 + CAP.DSTRD)). This is useful in software emulation of an NVM Express controller. In this case, a software thread is monitoring doorbell notifications. The software thread may be made more efficient by monitoring one doorbell per discrete cacheline or utilize the monitor/mwait CPU instructions. For hardware implementations of the NVM Express interface, the expected doorbell stride value is 0h.

8.7 Standard Vendor Specific Command Format

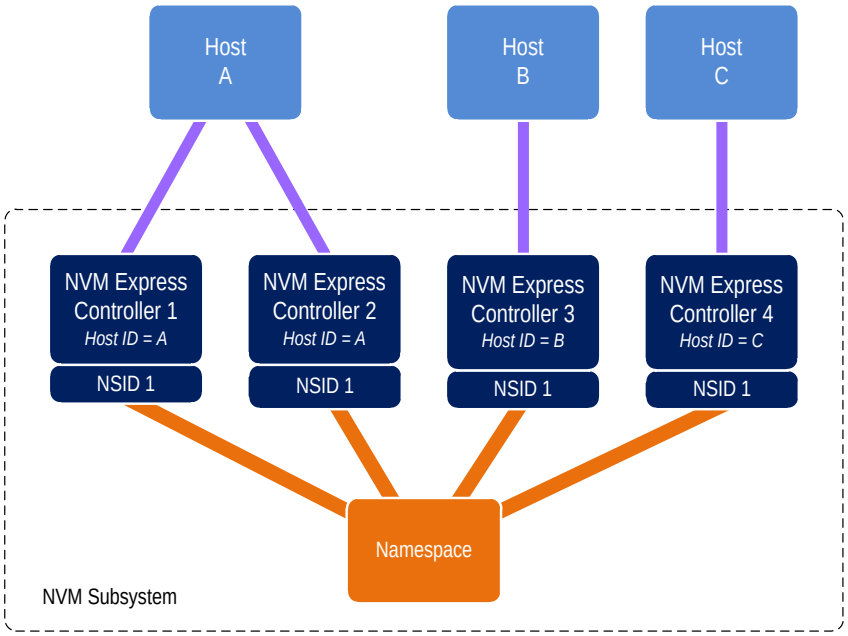
Controllers may support the standard Vendor Specific command format defined in Figure 107. Host storage drivers may use the Number of Dwords fields to ensure that the application is not corrupting physical memory (e.g., overflowing a data buffer). The controller indicates support of this format in the Identify Controller data structure in Figure 251; refer to Admin Vendor Specific Command Configuration and NVM Vendor Specific Command Configuration.

8.8 Reservations (Optional)

NVM Express reservations provide capabilities that may be utilized by two or more hosts to coordinate access to a shared namespace. The protocol and manner in which these capabilities are used is outside the scope of this specification. Incorrect application of these capabilities may corrupt data and/or otherwise impair system operation.

A reservation on a namespace restricts hosts access to that namespace. If a host submits a command to a namespace in the presence of a reservation and lacks sufficient rights, then the command is aborted by the controller with a status of Reservation Conflict. If a host submits a command with the NSID set to FFFFFFFFh in the presence of a reservation on any of the namespaces impacted by that command and that host lacks sufficient rights on all the impacted namespaces, then the command is aborted by the controller with a status of Reservation Conflict. Capabilities are provided that allow recovery from a reservation on a namespace held by a failing or uncooperative host.

Figure 464: Example Multi-Host System



A reservation requires an association between a host and a namespace. As shown in Figure 464, each controller in a multi-path I/O and namespace sharing environment is associated with exactly one host. While it is possible to construct systems where two or more hosts share a single controller, such usage is outside the scope of this specification.

A host may be associated with multiple controllers. In Figure 464 host A is associated with two controllers while hosts B and C are each associated with a single controller. A host registers a Host Identifier (refer to section 5.21.1.26) with each controller with which that host is associated using a Set Features command (refer to section 5.21) prior to performing any operations associated with reservations. The Host Identifier allows the NVM subsystem to identify controllers associated with the same host and preserve reservation properties across these controllers (i.e., a host issued command has the same reservation rights no matter which controller associated with the host processes the command).

Support for reservations by a namespace or controller is optional. A namespace indicates support for reservations by reporting a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure. A controller indicates support for reservations through the Optional NVM Command Support (ONCS) field in the Identify Controller data structure. If a host submits a command associated with reservations (i.e., Reservation Report, Reservation Register, Reservation Acquire, and Reservation Release) to a controller or a namespace that do not both support reservations, then the command is aborted by the controller with status Invalid Command Opcode.

Controllers that make up an NVM subsystem shall all have the same support for reservations. Although strongly encouraged, namespaces that make up an NVM subsystem are not all required to have the same support for reservations. For example, some namespaces within a single controller may support reservations while others do not, or the supported reservation types may differ among namespaces. If a controller supports reservations, then the controller shall:

- Indicate support for reservations by returning a '1' in bit 5 of the Optional NVM Command Support (ONCS) field in the Identify Controller data structure;
- Support the Reservation Report command (refer to section 6.13), Reservation Register command (refer to section 6.11), Reservation Acquire command (refer to section 6.10), and Reservation Release command (refer to section 6.12);
- Support the Reservation Notification log page;
- Support the Reservation Log Page Available asynchronous events;
- Support the Reservation Notification Mask Feature;

- Support the Host Identifier Feature; and
- Support the Reservation Persistence Feature.

If a namespace supports reservations, then the namespace shall:

- Report a non-zero value in the Reservation Capabilities (RESCAP) field in the Identify Namespace data structure;
- Support Persist Through Power Loss (PTPL) state; and
- Support sufficient resources to allow a host to successfully register a reservation key on every controller in the NVM subsystem with access to the shared namespace (i.e., a Reservation Register command shall never fail due to lack of resources).

NOTE: The behavior of Ignore Existing Key has been changed to improve compatibility with SCSI based implementations. Conformance to the modified behavior is indicated in the Reservation Capabilities (RESCAP) field of the Identify Namespace data structure. For the previous definition of Ignore Existing Key behavior, refer to revision 1.2.1.

8.8.1 Reservation Notifications

There are three types of reservation notifications: registration preempted, reservation released, and reservation preempted. Conditions that cause a reservation notification to occur are described in the following sections. A Reservation Notification log page is created whenever an unmasked reservation notification occurs on a namespace associated with the controller (refer to section 5.14.1.16.1). Reservation notifications may be masked from generating a reservation log page on a per reservation notification type and per namespace ID basis through the Reservation Notification Mask feature (refer to section 5.21.1.27). A host may use the Asynchronous Event Request command (refer to section 5.2) to be notified of the presence of one or more available Reservation Notification log pages (refer to section 5.14.1.16.1).

8.8.2 Registering

Prior to establishing a reservation on a namespace, a host shall become a registrant of that namespace by registering a reservation key. This reservation key may be used by the host as a means of identifying the registrant (host), authenticating the registrant, and preempting a failed or uncooperative registrant. The value of the reservation key used by a host and the method used to select its value is outside the scope of this specification.

Registering a reservation key with a namespace creates an association between a host and a namespace. A host that is a registrant of a namespace may use any controller with which that host is associated (i.e., that has the same Host Identifier, refer to section 5.21.1.26) to access that namespace as a registrant. Thus, a host is only required to register on a single controller to become a registrant of the namespace on all controllers in the NVM subsystem that have access to the namespace and are associated with the host.

A host registers a reservation key by executing a Reservation Register command (refer to section 6.11) on the namespace with the Reservation Register Action (RREGA) field cleared to 000b (i.e., Register Reservation Key) and supplying a reservation key in the New Reservation Key (NRKEY) field.

A host that is a registrant of a namespace may register the same reservation key value multiple times with the namespace on the same or different controllers. For a Reservation Register command with the RREGA field cleared to 000b:

a) the IEKEY field shall be ignored; and
b) if a host that is already a registrant of a namespace attempts to register with that namespace using a different registration key value, then the command shall be aborted with status Reservation Conflict.

There are no restrictions on the reservation key value used by hosts with different Host Identifiers. For example, multiple hosts may all register with the same reservation key value.

A host that is a registrant of a namespace may replace the existing reservation key value for that namespace by executing a Reservation Register command on the namespace with the:

a) RREGA field set to 010b (i.e., Replace Reservation Key);
b) current reservation key in the Current Reservation Key (CRKEY) field; and
c) new reservation key in the NRKEY field.

The current reservation key value shall be replaced by the new reservation key value in all controllers to which the namespace is attached that have the same Host Identifier as the Host Identifier of the controller processing the command. If the contents of the CRKEY field do not match the key currently associated with the host, then the command shall be aborted with a status of Reservation Conflict. A host may replace its reservation key without regard to its registration status or current reservation key value by setting the Ignore Existing Key (IEKEY) bit to '1' in the Reservation Register command. Replacing a reservation key has no effect on any reservation that may be held on the namespace.

8.8.3 Reservation Types

The NVM Express interface supports six types of reservations:

- Write Exclusive;
- Exclusive Access;
- Write Exclusive - Registrants Only;
- Exclusive Access - Registrants Only;
- Write Exclusive - All Registrants; and
- Exclusive Access - All Registrants.

Figure 465: Command Behavior in the Presence of a Reservation

Reservation Type	Reservation Holder		Registrant		Non-Registrant		Reservation Holder Definition
	Read	Write	Read	Write	Read	Write	
Write Exclusive	Y	Y	Y	N	Y	N	One Reservation Holder
Exclusive Access	Y	Y	N	N	N	N	One Reservation Holder
Write Exclusive - Registrants Only	Y	Y	Y	Y	Y	N	One Reservation Holder
Exclusive Access - Registrants Only	Y	Y	Y	Y	N	N	One Reservation Holder
Write Exclusive - All Registrants	Y	Y	Y	Y	Y	N	All Registrants are Reservation Holders
Exclusive Access - All Registrants	Y	Y	Y	Y	N	N	All Registrants are Reservation Holders

The differences between these reservation types are: the type of access that is excluded (i.e., writes or all accesses), whether registrants have the same access rights as the reservation holder, and whether registrants are also considered to be reservation holders. These differences are summarized in Figure 465 and the specific behavior for each NVM Express command is shown in Figure 466.

Reservations and registrations persist across all Controller Level Resets and all NVM Subsystem Resets except reset due to power loss. A reservation may be optionally configured to be retained across a reset due to power loss using the Persist Through Power Loss State (PTPLS). A Persist Through Power Loss State (PTPLS) is associated with each namespace that supports reservations and may be modified as a side effect of a Reservation Register command (refer to section 6.11) or a Set Features command (refer to section 5.21).

Figure 466: Command Behavior in the Presence of a Reservation

NVMe Command	Write Exclusive Reservation		Exclusive Access Reservation		Write Exclusive Registrants Only or Write Exclusive All Registrants Reservation		Exclusive Access Registrants Only or Exclusive Access All Registrants Reservation	
	Non-Registrant	Registrant	Non-Registrant	Registrant	Non-Registrant	Registrant	Non-Registrant	Registrant
NVM Read Command Group								
Compare Read Security Receive (Admin) Verify	A	A	C	C	A	A	C	A
NVM Write Command Group								
Dataset Management Flush Format NVM (Admin) Namespace Attachment (Admin) Namespace Management (Admin) Sanitize (Admin) Security Send (Admin) Write Write Uncorrectable Write Zeroes	C	C	C	C	C	A	C	A
Reservation Command Groups								
Reservation Acquire - Acquire	C	C	C	C	C	C	C	C
Reservation Acquire - Preempt Reservation Acquire - Preempt and Abort Reservation Release	C	A	C	A	C	A	C	A
All Other Commands Group								
All other commands[1]	A	A	A	A	A	A	A	A

Key:
A definition: A=Allowed, command processed normally by the controller
C definition: C=Conflict, command aborted by the controller with status Reservation Conflict

Notes:
1. The behavior of a vendor specific command is vendor specific.

8.8.4 Unregistering

A host that is a registrant of a namespace may unregister with the namespace by executing a Reservation Register command (refer to section 6.11) on the namespace with the RREGA field set to 001b (i.e., Unregister Reservation Key) and supplying its current reservation key in the CRKEY field. If the contents of the CRKEY field do not match the key currently associated with the host, then the command is aborted with a status of Reservation Conflict. If the host is not a registrant, then the command is aborted with a status of Reservation Conflict.

Successful completion of an unregister operation causes the host to no longer be a registrant of that namespace. A host may unregister without regard to its current reservation key value by setting the IEKEY bit to '1' in the Reservation Register command.

Unregistering by a host may cause a reservation held by the host to be released. If a host is the last remaining reservation holder (i.e., the reservation type is Write Exclusive - All Registrants or Exclusive Access - All Registrants) or is the only reservation holder, then the reservation is released when the host unregisters.

If a reservation is released and the type of the released reservation was Write Exclusive - Registrants Only or Exclusive Access - Registrants Only, then a reservation released notification occurs on all controllers associated with a registered host other than the host that issued the Reservation Register command.

8.8.5 Acquiring a Reservation

In order for a host to obtain a reservation on a namespace, that host shall be a registrant of that namespace. A registrant obtains a reservation by executing a Reservation Acquire command (refer to section 6.10), clearing the Reservation Acquire Action (RACQA) field to 000b (Acquire), and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field. The CRKEY value shall match that used by the registrant to register with the namespace. If the CRKEY value does not match, then the command is aborted with status Reservation Conflict. If the host is not a registrant, then the command is aborted with a status of Reservation Conflict.

Only one reservation is allowed at a time on a namespace. If a registrant attempts to obtain a reservation on a namespace that already has a reservation holder, then the command is aborted with status Reservation Conflict. If a reservation holder attempts to obtain a reservation of a different type on a namespace for which that host already is the reservation holder, then the command is aborted with status Reservation Conflict. It is not an error if a reservation holder attempts to obtain a reservation of the same type on a namespace for which that host already is the reservation holder. A reservation holder may preempt a reservation to change the reservation type.

8.8.6 Releasing a Reservation

Only a reservation holder may release in an orderly manner a reservation held on a namespace. A host releases a reservation by executing a Reservation Release command (refer to section 6.12), clearing the Reservation Release Action (RRELA) field to 000b (i.e., Release), setting the Reservation Type (RTYPE) field to the type of reservation being released, and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field. The CRKEY value shall match that used by the host to register with the namespace. If the key value doesn't match, then the command is aborted with status Reservation Conflict. If the RTYPE field does not match the type of the current reservation, then the command completes with status Invalid Field in Command.

An attempt by a registrant to release a reservation using the Reservation Release command in the absence of a reservation held on the namespace or when the host is not the reservation holder shall cause the command to complete successfully, but shall have no effect on the controller or namespace.

When a reservation is released as a result of actions described in this section and the reservation type is not Write Exclusive or Exclusive Access, a reservation released notification occurs on all controllers in the NVM subsystem that are associated with hosts that are registrants except for controllers that are associated with the host that issued the Reservation Release command.

8.8.7 Preempting a Reservation or Registration

A host that is a registrant may preempt a reservation and/or registration by executing a Reservation Acquire command (refer to section 6.10), setting the Reservation Acquire Action (RACQA) field to 001b (Preempt), and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field. The CRKEY value shall match that used by the registrant to register with the namespace. If the CRKEY value does not match, then the command is aborted with status Reservation Conflict. The preempt actions that occur are dependent on the type of reservation held on the namespace, if any, and the value of the Preempt Reservation Key (PRKEY) field in the command. If the host is not a registrant, then the

command is aborted with a status of Reservation Conflict. The remainder of this section assumes that the host is a registrant.

If the existing reservation type is not Write Exclusive - All Registrants and not Exclusive Access - All Registrants, then the actions performed by the command depend on the value of the PRKEY field as follows:

a) If the PRKEY field value matches the reservation key of the current reservation holder, then the following occur as an atomic operation:
   - all registrants with a matching registration key other than the host that issued the command are unregistered;
   - the reservation is released; and
   - a new reservation is created of the type specified by the Reservation Type (RTYPE) field in the command for the host that issued the command as the reservation key holder;

   or

b) If the PRKEY field value does not match that of the current reservation holder and is not equal to 0h, then registrants whose reservation key matches the value of the PRKEY field are unregistered. If the PRKEY field value does not match that of the current reservation holder and is equal to 0h, then the command is aborted with status Invalid Field in Command.

If the existing reservation type is Write Exclusive - All Registrants or Exclusive Access - All Registrants, then the actions performed by the command depend on the value of the PRKEY field as follows:

a) If the PRKEY field value is 0h, then the following occurs as an atomic operation:
   - all registrants other than the host that issued the command are unregistered;
   - the reservation is released; and
   - a new reservation is created of the type specified by the Reservation Type (RTYPE) field in the command for the host that issued the command as the reservation key holder;

   or

b) If the PRKEY value is non-zero, then registrants whose reservation key matches the value of the PRKEY field are unregistered. If the PRKEY value is non-zero and there are no registrants whose reservation key matches the value of the PRKEY field, the controller should return an error of Reservation Conflict.

If there is no reservation held on the namespace, then execution of the command causes registrants whose reservation key match the value of the PRKEY field to be unregistered.

If the existing reservation type is not Write Exclusive - All Registrants and not Exclusive Access - All Registrants, then a reservation holder may preempt itself using the above mechanism. When a host preempts itself the following occurs as an atomic operation:

- registration of the host is maintained;
- the reservation is released; and
- a new reservation is created for the host of the type specified by the RTYPE field.

A host may abort commands as a side effect of preempting a reservation by executing a Reservation Acquire command (refer to section 6.10) and setting the RACQA field to 010b (Preempt and Abort). The behavior of such a command is exactly the same as that described above with the RACQA field set to 001b (Preempt), with two exceptions:

- After the atomic operation changes namespace reservation and registration state, all controllers associated with any host whose reservation or registration is preempted by that atomic operation are requested to abort all commands being processed that were addressed to the namespace specified in the Namespace Identifier field (i.e., the NSID field in the Reservation Acquire command) (refer to section 4.13 for the definition of “being processed”); and

- Completion of the Reservation Acquire command shall not occur until all commands that are requested to be aborted are completed, regardless of whether or not each command is actually aborted.

As with the Abort Admin command (refer to section 5.1), abort as a side effect of preempting a reservation is best effort; as a command that is requested to be aborted may currently be at a point in execution where that command is no longer able to be aborted or may have already completed, when a Reservation Acquire or Abort Admin command is submitted. Although prompt execution of abort requests reduces delay in completing the Reservation Acquire command, a command which is requested to be aborted shall either be aborted or otherwise completed before the completion of the Reservation Acquire command.

When a registrant is unregistered as a result of actions described in this section, then a registration preempted notification occurs on all controllers associated with a host that was unregistered other than the host that issued the Reservation Acquire command.

When the type of reservation held on a namespace changes as a result of actions described in this section, then a reservation released notification occurs on all controllers associated with hosts that remain registrants of the namespace except the host that issued the Reservation Acquire command.

8.8.8 Clearing a Reservation

A host that is a registrant may clear a reservation (i.e., force the release of a reservation held on the namespace and unregister all registrants) by executing a Reservation Release command (refer to section 6.12), setting the Reservation Release Action (RRELA) field to 001b (i.e., Clear), and supplying the current reservation key associated with the host in the Current Reservation Key (CRKEY) field. If the value in the CRKEY field does not match the value used by the host to register with the namespace, then the command shall be aborted with status Reservation Conflict. If the host is not a registrant, then the command is aborted with a status of Reservation Conflict. When a command to clear a reservation is executed the following occur as an atomic operation: the reservation held on the namespace, if any, is released, and all registrants are unregistered from the namespace.

A reservation preempted notification occurs on all controllers in the NVM subsystem that are associated with hosts that have their registrations removed as a result of actions taken in this section except those associated with the host that issued the Reservation Release command.

8.8.9 Reporting Reservation Status

A host may determine the current reservation status associated with a namespace by executing a Reservation Report command (refer to section 6.13).

8.9 Host Memory Buffer (Optional)

The Host Memory Buffer (HMB) feature allows the controller to utilize an assigned portion of host memory exclusively. The use of the host memory resources is vendor specific. Host software may not be able to provide any or a limited amount of the host memory resources requested by the controller. The controller shall function properly without host memory resources. Refer to section 5.21.1.13.

The controller may indicate limitations for the minimum usable descriptor entry size and the maximum number of descriptor entries (refer to the HMMINDS and HMMAXD fields in the Identify Controller data structure). If the host does not create the Host Memory Buffer within the indicated limits, then the host memory allocated for use by the controller may not be fully utilized (e.g., descriptor entries beyond the maximum number of entries indicated may be ignored by the controller).

During initialization, host software may provide a descriptor list that describes a set of host memory address ranges for exclusive use by the controller. The host memory resources assigned are for the exclusive use of the controller (host software should not modify the ranges) until host software requests that the controller release the ranges and the controller completes the Set Features command. The controller is responsible

for initializing the host memory resources. Host software should request that the controller release the assigned ranges prior to a shutdown event, a Runtime D3 event, or any other event that requires host software to reclaim the assigned ranges. After the controller acknowledges that the ranges are no longer in use, host software may reclaim the host memory resources. In the case of Runtime D3, host software should provide the host memory resources to the controller again and inform the controller that the ranges were in use prior to the RTD3 event and have not been modified.

The host memory resources are not persistent in the controller across a reset event. Host software should provide the previously allocated host memory resources to the controller after the reset completes. If host software is providing previously allocated host memory resources (with the same contents) to the controller, the Memory Return bit is set to '1' in the Set Features command.

The controller shall ensure that there is no data loss or data corruption in the event of a surprise removal while the Host Memory Buffer feature is being utilized.

8.10 Replay Protected Memory Block (Optional)

The Replay Protected Memory Block (RPMB) provides a means for the system to store data to a specific memory area in an authenticated and replay protected manner. This is provided by first programming authentication key information to the controller that is used as a shared secret. The system is not authenticated in this phase, therefore the authentication key programming should be done in a secure environment (e.g., as part of the manufacturing process). The authentication key is utilized to sign the read and write accesses made to the replay protected memory area with a Message Authentication Code (MAC). Use of random number (nonce) generation and a write count register provide additional protection against replay of messages where messages could be recorded and played back later by an attacker.

The controller may support multiple RPMB targets. RPMB targets are not contained within a namespace. Controllers in the NVM subsystem may share the same RPMB targets. Security Send and Security Receive commands for RPMB do not use the namespace ID field; NSID shall be cleared to 0h. Each RPMB target operates independently – there may be requests outstanding to multiple RPMB targets at once (where the requests may be interleaved between RPMB targets). In order to guarantee ordering the host should issue and wait for completion for one Security Send or Security Receive command at a time. Each RPMB target requires individual authentication and key programming. Each RPMB target may have its own unique Authentication Key.

The message types defined in Figure 468 are used by the host to communicate with an RPMB target. Request Message Types are sent from the host to the controller. Response Message Types are sent to the host from the controller.

Figure 467 defines the RPMB Device Configuration Block data structure – the non-volatile contents stored within the controller for RPMB target 0.

Figure 467: RPMB Device Configuration Block Data Structure

Bytes	Component Name	Description
00	Boot Partition Protection Enable	This field indicates if Boot Partition Protection is enabled. Bits 7:1 are reserved. Bit 0: A value of '1' indicates Boot Partition Protection is enabled. A value of '0' indicates Boot Partition Protection is disabled or not supported. Once enabled, the controller shall prevent disabling Boot Partition Protection

Figure 467: RPMB Device Configuration Block Data Structure

Bytes	Component Name	Description
01	Boot Partition Lock	This field indicates the current status of the Boot Partition Lock. This field shall be cleared to 0h unless Boot Partition Protection is enabled. Refer to section 8.13.3. Bits 7:2 are reserved. Bit 1: A value of '1' indicates Boot Partition 1 (BPID = 1) is locked. A value of '0' indicates Boot Partition 1 (BPID = 1) is unlocked. Bit 0: A value of '1' indicates Boot Partition 0 (BPID = 0) is locked. A value of '0' indicates Boot Partition 0 (BPID = 0) is unlocked.
02	Namespace Write Protection Authentication Control	This field specifies whether the controller processes or aborts Set Features commands which enable certain namespace write protection states (refer to section 8.19 and section 5.21.1.29). If the controller does not support Namespace Write Protection, then this field shall be cleared to 0h. If the controller supports Namespace Write Protection, then bits 1:0 of this field shall be cleared to 00b after a power cycle or a Controller Level Reset. Bits 7:2 are reserved. Bit 1: If cleared to '0', indicates that the controller shall fail a Set Features command which attempts to set the namespace write protection state to Permanent Write Protect, as defined in section 8.19. If set to '1', indicates that the controller shall process a Set Features command which attempts to set the namespace write protection state to Permanent Write Protect. Bit 0: If cleared to '0', indicates that the controller shall fail a Set Features command which attempts to set the namespace write protection state to Write Protect Until Power Cycle, as defined in section 8.19. If set to '1', indicates that the controller shall process a Set Features command which sets the namespace write protection state to Write Protect Until Power Cycle.
511:03		Reserved

Each RPMB Data Frame is 256 bytes in size plus the size of the Data field, and is organized as shown in Figure 471. RPMB uses a sector size of 512 bytes. The RPMB sector size is independent and not related to the logical block size used for the namespace(s).

Figure 468: RPMB Request and Response Message Types

Request Message Types		Description	Requires Data	RPMB Frame Length (bytes)
0001h	Authentication key programming request	The host is attempting to program the Authentication Key for the selected RPMB target to the controller	No	256
0002h	Reading of the Write Counter value request	The host is requesting to read the current Write Counter value from the selected RPMB target	No	256
0003h	Authenticated data write request	The host is attempting to write data to the selected RPMB target	Yes	M + 256
0004h	Authenticated data read request	The host is attempting to read data from the selected RPMB target	No	256
0005h	Result read request	The host is attempting to read the result code for any of the other Message Types	No	256

Figure 468: RPMB Request and Response Message Types

Request Message Types		Description	Requires Data	RPMB Frame Length (bytes)
0006h	Authenticated Device Configuration Block write request	The host is attempting to write Device Configuration Block (DCB) to the selected RPMB target. This request message type is only valid for RPMB target 0.	Yes	512 + 256
0007h	Authenticated Device Configuration Block read request	The host is attempting to read Device Configuration Block (DCB) from the selected RPMB target. This request message type is only valid for RPMB target 0.	No	256
0100h	Authentication key programming response	Returned as a result of the host requesting a Result read request Message Type after programming the Authentication Key	No	256
0200h	Reading of the Write Counter value response	Returned as a result of the host requesting a Result read request Message Type after requesting the Write Counter value	No	256
0300h	Authenticated data write response	Returned as a result of the host requesting a Result read request Message Type after attempting to write data to an RPMB target	No	256
0400h	Authenticated data read response	Returned as a result of the host requesting a Result read request Message Type after attempting to read data from an RPMB target	Yes	M + 256
0600h	Authenticated Device Configuration data write response	Returned as a result of the host requesting a Result read request Message Type after attempting to write a Device Configuration Block to an RPMB target	No	256
0700h	Authenticated Device Configuration data read response	Returned as a result of the host requesting a Result read request Message Type after attempting to read DCB from an RPMB target	Yes	512 + 256

The operation result defined in Figure 469 indicates whether an RPMB request was successful or not.

Figure 469: RPMB Operation Result

<table>
<tr><th>Bits</th><th>Description</th></tr>
<tr><td>15:08</td><td>Reserved</td></tr>
<tr><td>07</td><td>Write Counter Status: Indicates if the Write Counter has expired (i.e., reached its maximum value). A value of ‘1’ indicates that the Write Counter has expired. A value of ‘0’ indicates a valid Write Counter.</td></tr>
<tr><td>06:00</td><td>Operation Status: Indicates the operation status. Valid operation status values are listed below.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>00h</td><td>Operation successful</td></tr>
<tr><td>01h</td><td>General failure</td></tr>
<tr><td>02h</td><td>Authentication failure (MAC comparison not matching, MAC calculation failure)</td></tr>
<tr><td>03h</td><td>Counter failure (counters not matching in comparison, counter incrementing failure)</td></tr>
<tr><td>04h</td><td>Address failure (address out of range, wrong address alignment)</td></tr>
<tr><td>05h</td><td>Write failure (data/counter/result write failure)</td></tr>
<tr><td>06h</td><td>Read failure (data/counter/result read failure)</td></tr>
<tr><td>07h</td><td>Authentication Key not yet programmed. This value is the only valid Result value until the Authentication Key has been programmed. Once the key is programmed, this Result value shall no longer be used.</td></tr>
<tr><td>08h</td><td>Invalid RPMB Device Configuration Block – this may be used when the target is not 0h.</td></tr>
<tr><td>09 to 3Fh</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Figure 470 defines the non-volatile contents stored within the controller for each RPMB target.

Figure 470: RPMB Contents

Content	Type	Size	Description
Authentication Key	Write once, not erasable or readable	Size is dependent on authentication method reported in Identify Controller data structure (e.g., SHA-256 is 32 bytes (refer to RFC 6234))	Authentication key which is used to authenticate accesses when MAC is calculated.
Write Counter	Read only	4 bytes	Counter value for the total amount of successful authenticated data write requests made by the host. The initial value of this register after manufacture is 00000000h. The value is incremented by one automatically by the controller with each successful programming access. The value is not resettable. After the counter has reached the maximum value of FFFFFFFFh, the controller shall no longer increment to prevent overflow.
RPMB Data Area	Readable and writable, not erasable	Size is reported in Identify Controller data structure (128 KiB minimum, 32 MiB maximum)	Data that is able to be read and written only via successfully authenticated read/write access.

Each RPMB Data Frame is 256 bytes in size plus the size of the Data field, and is organized as shown in Figure 471. RPMB uses a sector size of 512 bytes. The RPMB sector size is independent and not related to the logical block size used for the namespace(s).

Figure 471: RPMB Data Frame

Bytes	Component Name	Description
222-*N*:00	Stuff Bytes	Padding for the frame. Values in this field are not part of the MAC calculation. The size is 223 bytes minus the size of the Authentication Key (*N*).
222:222-(N-1)	Authentication Key or Message Authentication Code (MAC)	Size is dependent on authentication method reported in the Identify Controller data structure (e.g., SHA-256 key is 32 bytes (refer to RFC 6234)).
223	RPMB Target	Indicates which RPMB this Request/Response is targeted for. Values 0-6 are supported. If the value in this field is not equal to the NVMe Security Specific Field (NSSF) in the Security Send or Security Receive command, then the controller shall return an error of Invalid Field in Command for the Security Send or Security Receive command.
239:224	Nonce	Random number generated by the host for the requests and copied to the response by the RPMB target.
243:240	Write Counter	Total amount of successfully authenticated data write requests.
247:244	Address	Starting address of data to be programmed to or read from the RPMB.
251:248	Sector Count	Number of sectors (512 bytes) requested to be read or written.
253:252	Result	Defined in Figure 469. Note: The Result field is not needed for Requests.
255:254	Request/Response Message	Defined in Figure 468.
(M-1)+256:256	Data (Optional)	Data to be written or read by signed access where *M* = 512 * Sector Count.

Security Send and Security Receive commands are used to encapsulate and deliver data packets of any security protocol between the host and controller without interpreting, dis-assembling or re-assembling the data packets for delivery. Security Send and Security Receive commands used for RPMB access are populated with the RPMB Data Frame(s) defined in Figure 471. The controller shall not return successful completion of a Security Send or Security Receive command for RPMB access until the requested RPMB Request/Response Message Type indicated is completed. The Security Protocol used for RPMB is defined in section 5.25.3.

8.10.1 Authentication Method

A controller supports one Authentication Method as indicated in the Identify Controller data structure.

If the Authentication Method supported is HMAC SHA-256 (refer to RFC 6234), then the message authentication code (MAC) is calculated using HMAC SHA-256 as defined in RFC 6234. The key used to generate a MAC using HMAC SHA-256 is the 256-bit Authentication Key stored in the controller for the selected RPMB target. The HMAC SHA-256 calculation takes as input a key and a message. Input to the MAC calculation is the concatenation of the fields in the RPMB Data Frame (request or response) excluding stuff bytes and the MAC itself – i.e., bytes [223:255] and Data of the frame in that order.

8.10.2 RPMB Operations

The host sends a Request Message Type to the controller to request an operation by the controller or to deliver data to be written into the RPMB memory block. To deliver a Request Message Type, the host uses the Security Send command. If the data to be delivered to the controller is more than reported in Identify Controller data structure, the host sends multiple Security Send commands to transfer the entire data.

The host sends a Response Message Type to the controller to read the result of a previous operation request, to read the Write Counter, or to read data from the RPMB memory block. To deliver a Response Message Type, the host uses the Security Receive command. If the data to be read from the controller is more than reported in Identify Controller data structure, the host sends multiple Security Receive commands to transfer the entire data.

8.10.2.1 Authentication Key Programming

Authentication Key programming is initiated by a Security Send command to program the Authentication Key to the specified RPMB target, followed by a subsequent Security Send command to request the result, and lastly, the host issues a Security Receive command to retrieve the result.

Figure 472: RPMB – Authentication Key Data Flow

Command	Bytes in Command	Field Name	Value	Objective
Security Send 1	**Data populated by the host and sent to the controller**			Send Authentication Key to be Programmed to the controller
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*Key to be programmed*	
	223	RPMB Target	*RPMB target to access*	
	239:224	Nonce	0…00h	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	0000h	
	255:254	Request/Response	0001h *(Request)*	
Security Send 2	**Data populated by the host and sent to the controller**			Request Result of Key Programming
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	0…00h	
	223	RPMB Target	*RPMB target to access*	
	239:224	Nonce	0…00h	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	0000h	
	255:254	Request/Response	0005h *(Request)*	
Security Receive 1	**Data populated by the controller and returned to the host**			Retrieve the Key Programming Result
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	0…00h	
	223	RPMB Target	*RPMB target response was sent from*	
	239:224	Nonce	0…00h	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	*Result Code*	
	255:254	Request/Response	0100h *(Response)*	

8.10.2.2 Read Write Counter Value

The Read Write Counter Value sequence is initiated by a Security Send command to request the Write Counter value, followed by a Security Receive command to retrieve the Write Counter result.

Figure 473: RPMB – Read Write Counter Value Flow

Command	Bytes in Command	Field Name	Value	Objective
Security Send 1	**Data populated by the host and sent to the controller**			Request Write Counter Read
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	0…00h	
	223	RPMB Target	*RPMB target to access*	
	239:224	Nonce	*Nonce generated by the host*	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	0000h	
	255:254	Request/Response	0002h *(Request)*	
Security Receive 1	**Data populated by the controller and returned to the host**			Retrieve Write Counter Read Result
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*MAC generated by the controller*	
	223	RPMB Target	*RPMB target response was sent from*	
	239:224	Nonce	*Copy of the Nonce generated by the host*	
	243:240	Write Counter	*Current Write Counter value*	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	*Result Code*	
	255:254	Request/Response	0200h *(Response)*	

8.10.2.3 Authenticated Data Write

The Authenticated Data Write is initiated by a Security Send command. The RPMB Data Frame delivered from the host to the controller includes the Request Message Type = 0003h, Block Count, Address, Write Counter, Data and MAC.

When the controller receives this RPMB Data Frame, that controller first checks whether the Write Counter has expired. If the Write Counter has expired, then that controller sets the result to 0005h (write failure, write counter expired) and no data is written to the RPMB data area.

After checking the Write Counter is not expired, the Address is checked. If there is an error in the Address (e.g., out of range), then the result is set to 0004h (address failure) and no data is written to the RPMB data area.

After checking the Address is valid, the controller calculates the MAC (refer to section 8.10.1) and compares this with the MAC in the request. If the MAC in the request and the calculated MAC are different, then the controller sets the result to 0002h (authentication failure) and no data is written to the RPMB data area.

If the MAC in the request and the calculated MAC are equal, then the controller compares the Write Counter in the request with the Write Counter stored in the controller. If the counters are different, then the controller sets the result to 0003h (counter failure) and no data is written to the RPMB data area.

If the MAC and Write Counter comparisons are successful, then the write request is authenticated. The Data from the request is written to the Address indicated in the request and the Write Counter is incremented by one.

If the write fails, then the returned result is 0005h (write failure). If another error occurs during the write procedure, then the returned result is 0001h (general failure).

The controller returns a successful completion for the Security Send command when the Authenticated Data Write operation is completed regardless of whether the Authenticated Data Write was successful or not.

The success of programming the data should be checked by the host by reading the result register of the RPMB:

1) The host initiates the Authenticated Data Write verification process by issuing a Security Send command with delivery of a RPMB data frame containing the Request Message Type = 0005h;
2) The controller returns a successful completion of the Security Send command when the verification result is ready for retrieval;
3) The host should then retrieve the verification result by issuing a Security Receive command; and
4) The controller returns a successful completion of the Security Receive command and returns the RPMB data frame containing the Response Message Type = 0300h, the incremented counter value, the data address, the MAC and result of the data programming operation.

Figure 474: RPMB – Authenticated Data Write Flow

Command	Bytes in Command	Field Name	Value	Objective
Security Send 1	**Data populated by the host and sent to the controller**			Program data request
	222-N:00	Stuff Bytes	0…00h	
	222:222-(N-1)	MAC/Key	MAC generated by the host	
	223	RPMB Target	RPMB target to access	
	239:224	Nonce	0…00h	
	243:240	Write Counter	Current Write Counter value	
	247:244	Address	Address in the RPMB	
	251:248	Sector Count	Number of 512B blocks	
	253:252	Result	0000h	
	255:254	Request/Response	0003h (Request)	
	(M-1)+256:256	Data	Data to be written	
Security Send 2	**Data populated by the host and sent to the controller**			Request Result of data programming
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	0…00h	
	223	RPMB Target	*RPMB target to access*	
	239:224	Nonce	0…00h	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	0000h	
	255:254	Request/Response	0005h *(Request)*	
Security Receive 1	**Data populated by the controller and returned to the host**			Retrieve Result from data programming
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*MAC generated by the controller*	
	223	RPMB Target	*RPMB target response was sent from*	
	239:224	Nonce	0…00h	
	243:240	Write Counter	*Incremented Write Counter value*	
	247:244	Address	*Address in RPMB*	
	251:248	Sector Count	00000000h	
	253:252	Result	*Result Code*	
	255:254	Request/Response	0300h *(Response)*	

8.10.2.4 Authenticated Data Read

The Authenticated Data Read sequence is initiated by a Security Send command. The RPMB data frame delivered from the host to the controller includes the Request Message Type = 0004h, Nonce, Address, and the Sector Count.

When the controller receives this RPMB Data Frame, that controller first checks the Address. If there is an error in the Address, then the result is set to 0004h (address failure) and the data read is not valid.

When the host receives a successful completion of the Security Send command from the controller, that host should send a Security Receive command to the controller to retrieve the data. The controller returns

an RPMB Data Frame with Response Message Type (0400h), the Sector Count, a copy of the Nonce received in the request, the Address, the Data, the controller calculated MAC, and the Result. Note: It is the responsibility of the host to verify the MAC returned on an Authenticated Data Read Request.

If the data transfer from the addressed location in the controller fails, the returned Result is 0006h (read failure). If the Address provided in the Security Send command is not valid, then the returned Result is 0004h (address failure). If another error occurs during the read procedure, then the returned Result is 0001h (general failure).

Figure 475: RPMB – Authenticated Data Read Flow

Command	Bytes in Command	Field Name	Value	Objective
Security Send 1	**Data populated by the host and sent to the controller**			Read Data request
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	0..00h	
	223	RPMB Target	*RPMB target to access*	
	239:224	Nonce	*Nonce generated by the host*	
	243:240	Write Counter	00000000h	
	247:244	Address	*Address in RPMB*	
	251:248	Sector Count	*Number of 512B blocks*	
	253:252	Result	0000h	
	255:254	Request/Response	0004h *(Request)*	
Security Receive 1	**Data populated by the controller and returned to the host**			Retrieve result and data from read request
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*MAC generated by the controller*	
	223	RPMB Target	*RPMB target response was sent from*	
	239:224	Nonce	*Copy of the Nonce generated by the host*	
	243:240	Write Counter	0000h	
	247:244	Address	*Address in RPMB*	
	251:248	Sector Count	*Number of 512B blocks*	
	253:252	Result	*Result Code*	
	255:254	Request/Response	0400h *(Response)*	
	(*M*-1)+256:256	Data	*Data read from RPMB target*	

8.10.3 Authenticated Device Configuration Block Write

The Authenticated Device Configuration Block Write is initiated by a Security Send command. The RPMB Data Frame delivered from the host to the controller includes the Request Message Type = 0006h, Sector Count = 01h, MAC, Write Counter set to the current Write Counter value, and the RPMB Device Configuration Block data structure (refer to Figure 476). All other fields are cleared to 0h.

If the Write Counter has expired, then that controller sets the result to 0005h (write failure, write counter expired) and no data is written to the Device Configuration Block.

The controller calculates the MAC of Request Type, Block Count, Write Counter, Address and Data, and compares this with the MAC in the request. If the MAC in the request and the calculated MAC are different, then the controller sets the result to 0002h (authentication failure) and no data is written to the RPMB Device Configuration Block.

If the Data from the RPMB Device Configuration Block attempts to disable Boot Partition Protection, then the controller sets the result to 0008h (Invalid RPMB Device Configuration Block) and no data is written to the RPMB Device Configuration Block.

If the MAC in the request and the calculated MAC are equal, then the write request is authenticated. The Data from the request is written to the RPMB Device Configuration Block.

If any other error occurs during the write procedure, then the returned result is 0001h (general failure).

The controller returns a successful completion for the Security Send command when the Authenticated Data Write operation is completed regardless of whether the Authenticated Device Configuration Block Write was successful or not.

When the host receives a successful completion of the Security Send command from the controller, that host should send a Security Receive command to the controller to retrieve the data. The controller returns an RPMB Data Frame with Response Message Type (0600h), the incremented counter value, the MAC, and the Result. All other fields are cleared to 0h.

The Write Counter for the Device Configuration Block is independent of the Write Counter for RPMB target 0. Authenticated Device Configuration Block Writes do not affect the Write Counter for RPMB target 0 since the data is not part of the RPMB data area. The current value of the Write Counter for the Device Configuration Block may be read using an Authenticated Device Configuration Block Read (refer to section 8.10.4).

Figure 476: RPMB – Authenticated Device Configuration Block Write Flow

Command	Bytes in Command	Field Name	Value	Objective
Security Send 1	**Data populated by the host and sent to the controller**			Request Device Configuration Block Write
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*MAC generated by the host*	
	223	RPMB Target	00h	
	239:224	Nonce	0…00h	
	243:240	Write Counter	*Current Write Counter value*	
	247:244	Address	00000000h	
	251:248	Sector Count	00000001h	
	253:252	Result	0000h	
	255:254	Request/Response	0006h *(Request)*	
	767:256	Data	*RPMB Device Configuration Block data structure*	
Security Send 2	**Data populated by the host and sent to the controller**			Request Result of data programming
	222-N:00	Stuff Bytes	0…00h	
	222:222-(N-1)	MAC/Key	0…00h	
	223	RPMB Target	*RPMB target to access*	
	239:224	Nonce	0…00h	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	0000h	
	255:254	Request/Response	0005h *(Request)*	
Security Receive 1	**Data populated by the controller and returned to the host**			Retrieve Device Configuration Block Write Result
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*MAC generated by the controller*	
	223	RPMB Target	00h	
	239:224	Nonce	0…00h	
	243:240	Write Counter	*Incremented Write Counter value*	
	247:244	Address	00000000h	
	251:248	Sector Count	00000000h	
	253:252	Result	*Result Code*	
	255:254	Request/Response	0600h *(Response)*	

8.10.4 Authenticated Device Configuration Block Read

The Authenticated Device Configuration Block Read sequence is initiated by a Security Send command. The RPMB data frame delivered from the host to the controller includes the Nonce, Request Message Type = 0007h and the Sector Count = 01h. All other fields are cleared to 0h.

When the host receives a successful completion of the Security Send command from the controller, that host should send a Security Receive command to the controller to retrieve the data. The controller returns an RPMB Data Frame with Response Message Type (0700h), the Sector Count = 01h, a copy of the Nonce received in the request, the RPMB Device Configuration Block Data Structure (refer to Figure 467), the MAC, the Write Counter set to the current Write Counter value, and the Result. All other fields are cleared to 0h.

The Write Counter for the Device Configuration Block is independent of the Write Counter for RPMB target 0. The controller returns the Device Configuration Block Write Counter as shown in Figure 477.

The MAC is calculated from Response Type, Nonce, Address, Data and Result fields. If the MAC calculation fails, then the returned result is 0002h (authentication failure). If another error occurs during the read procedure, then the returned Result is 0001h (general failure).

Figure 477: RPMB – Authenticated Device Configuration Block Read Flow

Command	Bytes in Command	Field Name	Value	Objective
Security Send 1	**Data populated by the host and sent to the controller**			Request Device Configuration Block Read
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	0..00h	
	223	RPMB Target	00h	
	239:224	Nonce	*Nonce generated by the host*	
	243:240	Write Counter	00000000h	
	247:244	Address	00000000h	
	251:248	Sector Count	00000001h	
	253:252	Result	0000h	
	255:254	Request/Response	0007h *(Request)*	
Security Receive 1	**Data populated by the controller and returned to the host**			Retrieve Device Configuration Block Read Result
	222-*N*:00	Stuff Bytes	0…00h	
	222:222-(*N*-1)	MAC/Key	*MAC generated by the controller*	
	223	RPMB Target	00h	
	239:224	Nonce	*Copy of the Nonce generated by the host*	
	243:240	Write Counter	*Current Write Counter value*	
	247:244	Address	00000000h	
	251:248	Sector Count	00000001h	
	253:252	Result	*Result Code*	
	255:254	Request/Response	0700h *(Response)*	
	767:256	Data	*RPMB Device Configuration Block data structure*	

8.11 Device Self-test Operations (Optional)

A device self-test operation is a diagnostic testing sequence that tests the integrity and functionality of the controller and may include testing of the media associated with namespaces. The operation is broken down in to a series of segments, where each segment is a set of vendor specific tests. The segment number in the Self-test Result Data Structure (refer to section 5.14.1.6) is used for reporting purposes to indicate where a test failed, if any. The test performed in each segment may be the same for the short device self-test operation and the extended device self-test operation.

A device self-test operation is performed in the background allowing concurrent processing of some commands and requiring suspension of the device self-test operation to process other commands. Which commands may be processed concurrently versus require suspension of the device self-test operation is vendor specific.

If the controller receives any command that requires suspension of the device self-test operation to process and complete, then the controller shall:

1) suspend the device self-test operation;
2) process and complete that command; and
3) resume the device self-test operation.

During a device self-test operation, the performance of the NVM subsystem may be degraded (e.g., controllers not performing the device self-test operation may also experience degraded performance).

The following device self-test operations are defined:

a) short device self-test operation (refer to section 8.11.1); and
b) extended device self-test operation (refer to section 8.11.2).

Figure 478 is an informative example of a device self-test operation with the associated segments and tests performed in each segment.

Figure 478: Example Device Self-test Operation (Informative)

Segment		Test Performed	Failure Criteria
1 – RAM Check		Write a test pattern to RAM, followed by a read and compare of the original data.	Any uncorrectable error or data miscompare
2 – SMART Check		Check SMART or health status for Critical Warning bits set to '1' in SMART / Health Information Log.	Any Critical Warning bit set to '1' fails this segment
3 – Volatile memory backup		Validate volatile memory backup solution health (e.g., measure backup power source charge and/or discharge time).	Significant degradation in backup capability
4 – Metadata validation		Confirm/validate all copies of metadata.	Metadata is corrupt and is not recoverable
5 – NVM integrity		Write/read/compare to reserved areas of each NVM. Ensure also that every read/write channel of the controller is exercised.	Data miscompare
Extended only	6 – Data Integrity	Perform background housekeeping tasks, prioritizing actions that enhance the integrity of stored data. Exit this segment in time to complete the remaining segments and meet the timing requirements for extended device self-test operation indicated in the Identify Controller data structure.	Metadata is corrupt and is not recoverable
7 – Media Check		Perform random reads from every available good physical block. Exit this segment in time to complete the remaining segments. The time to complete is dependent on the type of device self-test operation.	Inability to access a physical block
8 – Drive Life		End-of-life condition: Assess the drive's suitability for continuing write operations.	The Percentage Used is set to 255 in the SMART / Health Information Log or an analysis of internal key operating parameters indicates that data is at risk if writing continues
9 – SMART Check		Same as 2 – SMART Check	

8.11.1 Short Device Self-Test Operation

A short device self-test operation should complete in two minutes or less. The percentage complete of the short device self-test operation is indicated in the Current Percentage Complete field in the Device Self-test Log (refer to section 5.14.1.6).

A short device self-test operation:

a) shall be aborted by any Controller Level Reset that affects the controller on which the device self-test is being performed;
b) shall be aborted by a Format NVM command as described in Figure 479;

c) shall be aborted when a sanitize operation is started (refer to section 5.24);
d) shall be aborted if a Device Self-test command with the Self-Test Code field set to Fh is processed; and
e) may be aborted if the specified namespace is removed from the namespace inventory.

Figure 479: Format NVM command Aborting a Device Self-Test Operation

FNA bit [1]	NSID in Format NVM command	NSID in Device Self-test command	Abort Device Self-Test operation?
0	Any allocated NSID value (refer to section 6.1.3)	Any active NSID value (refer to section 6.1)	Yes, if the NSID values are the same
0	FFFFFFFFh	Any active NSID value (refer to section 6.1)	Yes
0	Any allocated NSID value (refer to section 6.1.3)	FFFFFFFFh	Optional
0	FFFFFFFFh	FFFFFFFFh	Yes
1	Ignored	Ignored	Yes

Key:
Optional = The device self-test operation is not required to be aborted but may be aborted.

NOTES:
1. For a Format NVM command with Secure Erase, this column refers to Bit 1 in the FNA field in the Identify Controller data structure (refer to Figure 251) and bit 0 in the FNA field is ignored. For a Format NVM command without Secure Erase, this column refers to bit 0 in the FNA field, and bit 1 in the FNA field is ignored.

8.11.2 Extended Device Self-Test Operation

An extended device self-test operation should complete in the time indicated in the Extended Device Self-test Time field in the Identify Controller data structure or less. The percentage complete of the extended device self-test operation is indicated in the Current Percentage Complete field in the Device Self-test Log (refer to section 5.14.1.6).

An extended device self-test operation shall persist across any Controller Level Reset, and shall resume after completion of the reset or any restoration of power, if any. The segment where the extended device self-test operation resumes is vendor specific, but implementations should only have to perform tests again within the last segment that was being tested prior to the reset.

An extended device self-test operation:

a) shall be aborted by a Format NVM command as described in Figure 479;
b) shall be aborted when a sanitize operation is started (refer to section 5.24);
c) shall be aborted if a Device Self-test command with the Self-Test Code field set to Fh is processed; and
d) may be aborted if the specified namespace is removed from the namespace inventory.

8.12 Namespace Management (Optional)

The Namespace Management capability consist of the Namespace Management command (refer to section 5.20) and the Namespace Attachment command (refer to section 5.19). The Namespace Management command is used to create a namespace or delete a namespace. The Namespace Attachment command is used to attach and detach controllers from a namespace. The Namespace Management capability is intended for use during manufacturing or by a system administrator.

If the Namespace Management capability is supported, then the controller:

a) shall support the Namespace Management command and the Namespace Attachment command;
b) shall set bit 3 to ‘1’ in the OACS field (refer to Figure 251);

c) should support the Namespace Attribute Changed asynchronous event (refer to Figure 149 and section 5.21.1.11); and
d) may support Namespace Granularity (refer to section 8.12.1).

If a namespace is detached from a controller, then the NSID that referred to that namespace becomes an inactive NSID (refer to section 6.1.4) on that controller. If a namespace is deleted from the NVM subsystem, then the NSID that referred to that namespace becomes an unallocated NSID (refer to section 6.1.3) in the NVM subsystem. Previously submitted but uncompleted or subsequently submitted commands to the affected NSID are handled by the controller as if they were issued to an inactive NSID (refer to Figure 106).

The size of a namespace is based on the number of logical blocks requested in a create operation, the format of the namespace, and any characteristics (e.g., endurance). The controller determines the NVM capacity allocated for that namespace. Namespaces may be created with different usage characteristics (e.g., endurance) that utilize differing amounts of NVM capacity. Namespace characteristics and the mapping of these characteristics to NVM capacity usage are outside the scope of this specification.

The total and unallocated NVM capacity for the NVM subsystem is reported in the Identify Controller data structure (refer to Figure 251). For controllers that support NVM Sets, the total and unallocated NVM capacity for each NVM Set is reported as part of the NVM Set Attributes Entry (refer to Figure 255). For each namespace, the NVM Set in which the namespace is allocated is reported in the Identify Namespace data structure. The NVM Set to be used for a namespace is based on the value in the NVM Set Identifier field in a create operation. If the NVM Set Identifier field is cleared to 0h in a create operation, then the controller shall choose the NVM Set from which to allocate the namespace.

For each namespace, the NVM capacity used for that namespace is reported in the Identify Namespace data structure (refer to Figure 249). The controller may allocate NVM capacity in units such that the requested size for a namespace may be rounded up to the next unit boundary. The units in which NVM capacity is allocated are reported in the Namespace Granularity List (refer to Figure 259), if supported. For example, if host software requests a namespace of 32 logical blocks with a logical block size of 4 KiB for a total size of 128 KiB and the allocation unit for the implementation is 1 MiB, then the NVM capacity consumed may be rounded up to 1 MiB. The NVM capacity fields may not correspond to the logical block size multiplied by the total number of logical blocks.

The method of allocating ANA Group identifiers is outside the scope of this specification. If the ANA Group Identifier (refer to Figure 266) is cleared to 0h, then the controller shall determine the ANAGRPID that is assigned to that namespace.

To create a namespace, host software performs the following actions:

1. Host software requests the Identify Namespace data structure that specifies common namespace capabilities (i.e., using an Identify command with the NSID field set to FFFFFFFFh and the CNS field cleared to 0h);
2. If the controller supports reporting of Namespace Granularity, host software optionally requests the Namespace Granularity List defined in Figure 259 (Identify command with CNS set to 16h).
3. Host software creates the data structure defined in Figure 269. Host software sets the host software specified fields defined in Figure 266 (taking into account the common namespace capabilities);
4. Host software issues the Namespace Management command specifying the Create operation and the data structure. On successful completion of the command, the Namespace Identifier of the new namespace is returned in Dword 0 of the completion queue entry. At this point, the new namespace is not attached to any controller; and
5. Host software requests the Identify Namespace data structure for the new namespace to determine all attributes of the namespace.

To attach a namespace, host software performs the following actions:

1. Host software issues the Namespace Attachment command specifying the Controller Attach operation to attach the specified namespace to one or more controllers; and
2. If Namespace Attribute Notices are enabled, the controller(s) newly attached to the namespace report a Namespace Attribute Changed asynchronous event to the host.

To detach a namespace, host software performs the following actions:

1. Host software issues the Namespace Attachment command specifying the Controller Detach operation to detach the specified namespace from one or more controllers; and
2. If Namespace Attribute Notices are enabled, the controllers that were detached from the namespace report a Namespace Attribute Changed asynchronous event to the host.

To delete a namespace, host software performs the following actions:

1. Host software should detach the namespace from all controllers;
2. Host software issues the Namespace Management command specifying the Delete operation for the specified namespace. On successful completion of the command, the namespace has been deleted; and
3. If Namespace Attribute Notices are enabled, any controller(s) not processing the Namespace Management command that was attached to the namespace reports a Namespace Attribute Changed asynchronous event to the host.

8.12.1 Namespace Granularity

If the controller supports reporting of Namespace Granularity, then the Namespace Granularity Descriptor List (refer to Figure 259) contains one or more Namespace Granularity Descriptors (refer to Figure 260) indicating the size granularity and the capacity granularity at which the controller allocates namespaces.

The size granularity and the capacity granularity are hints which may be used by the host to minimize the capacity that is allocated for a namespace and that is not able to be addressed by logical block addresses. The granularities are used in specifying values for the Namespace Size (NSZE) and Namespace Capacity (NCAP) fields of the data structure used for the create operation of the Namespace Management command (refer to section 5.20).

If a Namespace Management command create operation specifies values such that:

a) the product of NSZE and the Formatted LBA Size value is an integral multiple of the Namespace Size Granularity;
b) the product of NCAP and the Formatted LBA Size value is an integral multiple of the Namespace Capacity Granularity; and
c) NSZE is equal to NCAP,

then the namespace is fully provisioned and all of the capacity allocated for the namespace is able to be addressed by logical block addresses, otherwise:

a) not all of the capacity allocated for the namespace is able to be addressed by logical block addresses; and
b) if the Namespace Management command is otherwise valid, then the controller shall not abort the command (i.e., the granularity values are hints).

8.13 Boot Partitions (Optional)

Boot Partitions provide an optional area of NVM storage that may be read by the host without the host initializing queues or enabling the controller. The simplified interface to access Boot Partitions may be used for platform initialization code (e.g., a bootloader that is executed from host ROM) to boot to a pre-OS environment (e.g., UEFI) instead of storing the image on another storage medium (e.g., SPI flash). Refer to section 8.13.1 for the procedure to read the contents of a Boot Partition.

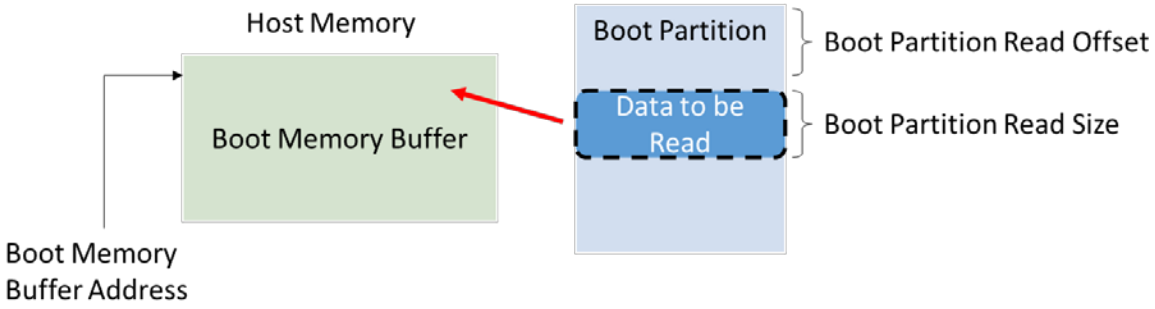
An NVMe controller that supports Boot Partitions has two Boot Partitions of equal size using Boot Partition identifiers 0h and 1h. The two Boot Partitions allow the host to update one and verify the contents before marking the Boot Partition active. Controllers in the NVM subsystem may share the same Boot Partitions.

The contents of Boot Partitions are only modified using the Firmware Image Download and Firmware Commit commands (refer to section 8.13.2) and may be secured using Replay Protected Memory Block to prevent unauthorized modifications (refer to section 8.13.3).

8.13.1 Reading from a Boot Partition

A Boot Partition is a continuous block of data as shown in Figure 480, that the host may read.

Figure 480: Boot Partition Overview



To read the contents of a Boot Partition, the host allocates a Boot Partition Memory Buffer in host memory for the controller to copy contents from a Boot Partition. The host initializes the Boot Partition Memory Buffer Base Address. The host sets the Boot Partition ID, Boot Partition Read Size, and Boot Partition Read Offset to initiate the Boot Partition read operation. The host may continue reading from the Boot Partition until the entire Boot Partition has been read.

A portion of the Boot Partition may be read by the host any time the NVM subsystem is powered (i.e., whether or not CC.EN is set to '1'). The host shall not modify the PCI Express registers (described in section 2), reset, or shutdown the controller while a Boot Partition read is in progress.

To read data from a Boot Partition, the host follows these steps:

1. Initialize the transport (e.g., PCIe link), if necessary;
2. Determine if Boot Partitions are supported by the controller (CAP.BPS);
3. Determine which Boot Partition is active (BPINFO.ABPID) and the size of the Boot Partition (BPINFO.BPSZ);
4. Allocate a physically contiguous memory buffer in the host to store the contents of a Boot Partition;
5. Initialize the address (BPMBL.BMBBA) into the memory buffer where the contents should be copied;
6. Initiate the transfer of data from a Boot Partition by writing to the Boot Partition Read Select (BPRSEL) register. This includes setting the Boot Partition identifier (BPRSEL.BPID), size of Boot Partition Read Size (BPRSEL.BPRSZ) and Boot Partition Read Offset (BPRSEL.BPROF). The controller sets the Boot Read Status (BPINFO.BRS) field while transferring the Boot Partition contents to indicate a Boot Partition read operation is in progress; and
7. Wait for the controller to completely transfer the requested portion of the Boot Partition, indicated in the status field (BPINFO.BRS). If BPINFO.BRS is set to 10b, the requested Boot Partition data has been transferred to the Boot Partition Memory Buffer. If BPINFO.BRS is set to 11b, there was an error transferring the requested Boot Partition data and the host may request the Boot Partition data again.

In constrained memory environments, the host may read the contents of a Boot Partition with a small Boot Partition Memory Buffer by reading a small portion of a Boot Partition, moving the data out of the Boot Memory Buffer to another memory location, and then reading another portion of the Boot Partition until the entire Boot Partition has been read.

8.13.2 Writing to a Boot Partition

Boot Partition contents may be modified by the host using the Firmware Image Download and Firmware Commit commands while the controller is enabled (CC.EN set to '1').

The process for updating a Boot Partition is:

1. The host issues a Firmware Image Download command to download the contents of the Boot Partition to the controller. There may be multiple portions of the Boot Partition to download, thus the offset for each portion of the Boot Partition being downloaded is specified in the Firmware Image Download command. Host software shall send the Boot Partition image in order starting with the beginning of the Boot Partition;
2. Unlock Boot Partitions for writing (refer to section 8.13.3);
3. The host submits a Firmware Commit command with a Commit Action of 110b which specifies that the downloaded image replaces the contents of the Boot Partition specified in the Boot Partition ID field;
4. The controller completes the Firmware Commit command. The following actions are taken in certain error scenarios:
   a. If the firmware activation was not successful because the Boot Partition could not be written, then the controller reports an error of Boot Partition Write Prohibited;
5. (Optional) The host reads the contents of the Boot Partition to verify they are correct (refer to section 8.13.1). Host software updates the active Boot Partition ID by issuing a Firmware Commit command with a Commit Action of 111b; and
6. The host locks Boot Partition access to prevent further modification (refer to section 8.13.3).

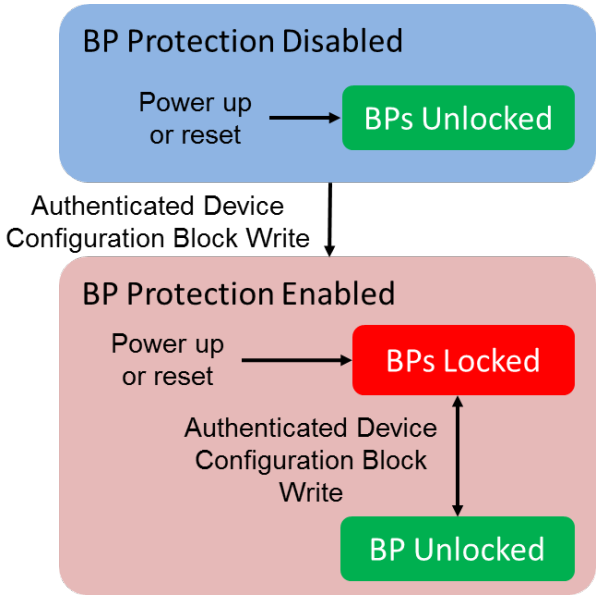
If an internal error, reset, or power loss condition occurs while committing the downloaded image to a Boot Partition, the contents of the Boot Partition may contain the old contents, new contents, or a mixture of both. Host software should verify the contents of a Boot Partition before marking that Boot Partition active to ensure the active Boot Partition is stable.

Host software should not read the contents of a Boot Partition while writing to the Boot Partition. The controller may return a combination of new and old data if the host attempts to perform a Boot Partition read operation while overwriting the contents.

8.13.3 Boot Partition Protection

A controller that supports Boot Partitions and RPMB shall support Boot Partition Protection. Boot Partition Protection may be configured using RPMB (refer to section 8.10). Figure 481 shows an overview of Boot Partition Protection.

Figure 481: Boot Partition Protection Overview



The default state for all Boot Partitions is the “Unlocked” state. In this state, host software may read and write a Boot Partition.

All Boot Partitions remain unlocked until Boot Partition Protection is enabled by host software. Host software enables Boot Partition Protection by setting the Boot Partition Protection Enable bit in the RPMB Device Configuration Block data structure (refer to section 8.10). Once Boot Partition Protection is enabled, the controller shall reject Authenticated Device Configuration Block Writes that disable Boot Partition Protection (i.e., enabling Boot Partition Protection is permanent). Once Boot Partition Protection is enabled, Boot Partitions are able to be modified only after unlocking the Boot Partition using RPMB.

After activating Boot Partition Protection, the default state for all Boot Partitions is the “Locked” state. In this state, host software may read a Boot Partition. In this state, the controller rejects attempts to write to a Boot Partition using the Firmware Commit command.

Each Boot Partition may be locked or unlocked independently using the corresponding bit in the Device Configuration Block data structure.

8.14 Telemetry (Optional)

Telemetry enables manufacturers to collect internal data logs to improve the functionality and reliability of products. The telemetry data collection may be initiated by the host or by the controller. The data is returned in the Telemetry Host-Initiated log page or the Telemetry Controller-Initiated log page (refer to section 5.14.1.7 and 5.14.1.8). The data captured is vendor specific. The telemetry feature defines the mechanism to collect the vendor specific data. The controller indicates support for the telemetry log pages in the Log Page Attributes field in the Identify Controller data structure.

An important aspect to discovering issues by collecting telemetry data is the ability to qualify distinct issues that are being collected. The ability to create a one to one mapping of issues to data collections is essential. If a one to one mapping is not established, there is the risk that several payload collections appear distinct but are actually all caused by the same issue. Conversely, a single payload collection may have payloads caused by several issues mixed together creating additional complexity in determining the root cause. As a result, flexibility in size is provided in the collection of telemetry payloads and a three phase process is typically used.

The first phase establishes that an issue exists and is best accomplished by collecting a minimum set of data to identify the issue as being distinct from other issues. Once the number of instances of an issue establish an investigation, another phase may be necessary to collect actionable information. In the second phase, a targeted collection of more in depth medium size payloads are gathered and analyzed to identify the source of the problem. For rare issues that are not root caused by a small or medium sized telemetry data collection, a third phase may be employed to collect the largest and most complete payload to diagnose the issue.

There are two telemetry data logs (i.e., Host-Initiated log and Controller-Initiated log) defined. Each telemetry data log is made up of a single set of Telemetry Data Blocks. Each Telemetry Data Block is 512 bytes in size. Telemetry data is returned (refer to section 5.14.1.7 and section 5.14.1.8) in units of Telemetry Data Blocks. Each telemetry data log is segmented into three Telemetry Data Areas (i.e., small, medium, and large). All telemetry data areas start at Telemetry Data Block 1. Each Telemetry Data Area shall represent the controller's internal state at the time the telemetry data was captured.

Each Telemetry Data Area is intended to capture a richer set of data to aid in resolution of issues. Telemetry Data Area 1 is intended to have a small size payload (i.e., the first phase), Telemetry Data Area 2 is intended to have a medium size payload (i.e., the second phase), and Telemetry Data Area 3 is intended to have a large size payload (i.e., the third phase). The size of each Telemetry Data Area is vendor specific and may change on each data collection. When possible, the host should retrieve the payload for all three Telemetry Data Areas to enable the best diagnosis of the issue(s).

The preparation, collection, and submission of telemetry data is similar for host-initiated and controller-initiated data; the primary difference is the trigger for the collection. The operational model for telemetry is:

1. The host identifies controller support for Telemetry log pages in the Identify Controller data structure;
2. The host prepares an area to store telemetry data if needed;
3. To receive notification that controller-initiated telemetry data is available, the host enables Telemetry Log Notices using the Asynchronous Event Configuration feature (refer to section 5.21.1.11); and
4. If the host decides to collect host-initiated telemetry data or the controller signals that controller-initiated telemetry data is available:
    a. The host reads the appropriate blocks of the Telemetry Data Area from the host-initiated log (refer to section 5.14.1.7) or the controller-initiated log (refer to section 5.14.1.8). If possible, the host should collect Telemetry Data Area 1, 2, and 3. The host reads the log in 512 byte Telemetry Data Block units. As part of the last read for a controller-initiated log, the host clears the Retain Asynchronous Event bit to '0';
    b. If it is a controller-initiated log, the host re-reads the header of the log page and ensures that the Telemetry Controller-Initiated Data Generation Number matches the original value read. If these values do not match, then the data captured is not consistent and needs to be re-read; and
    c. When all telemetry data has been saved, the data should be forwarded to the manufacturer of the controller.

The trigger for the collection for host-initiated data is typically a system crash, but may also be initiated during normal operation. The host proceeds with a host-initiated data collection by submitting the Get Log Page command for the Telemetry Host-Initiated log page with the Create Telemetry Host-Initiated Data bit set to '1'. The controller should complete the command quickly (e.g., in less than one second) to avoid a user rebooting the system prior to completion of the data collection.

The controller notifies the host to collect controller-initiated data through the completion of an Asynchronous Event Request command with an Asynchronous Event Type of Notice that indicates a Telemetry Log Changed event. The host may also determine controller-initiated data is available via the Telemetry Controller-Initiated Data Available field in the Telemetry Host-Initiated or the Telemetry Controller-Initiated log pages. The host proceeds with a controller-initiated data collection by submitting the Get Log Page command for the Telemetry Controller-Initiated log page. Once the host has started reading the Telemetry

Controller-Initiated log page, the controller should avoid modifying the controller-initiated data until the host has finished reading all controller-initiated data.

Since there is only one set of controller-initiated data, the controller is responsible for prioritizing the version of the controller-initiated data that is available for the host to collect. When the controller replaces the controller-initiated data with new controller-initiated data, the controller shall increment the Telemetry Controller-Initiated Data Generation Number field. The host needs to ensure that the Telemetry Controller-Initiated Data Generation Number field has not changed between the start and completion of the controller-initiated data collection to ensure the data captured is consistent.

8.14.1 Telemetry Data Collection Examples (Informative)

This section includes several examples of Telemetry Host-Initiated Data Areas for illustration. The same concepts apply to the Telemetry Controller-Initiated Data Areas.

If a Telemetry Host-Initiated log page has no data for collection, then the following fields are all cleared to 0h:

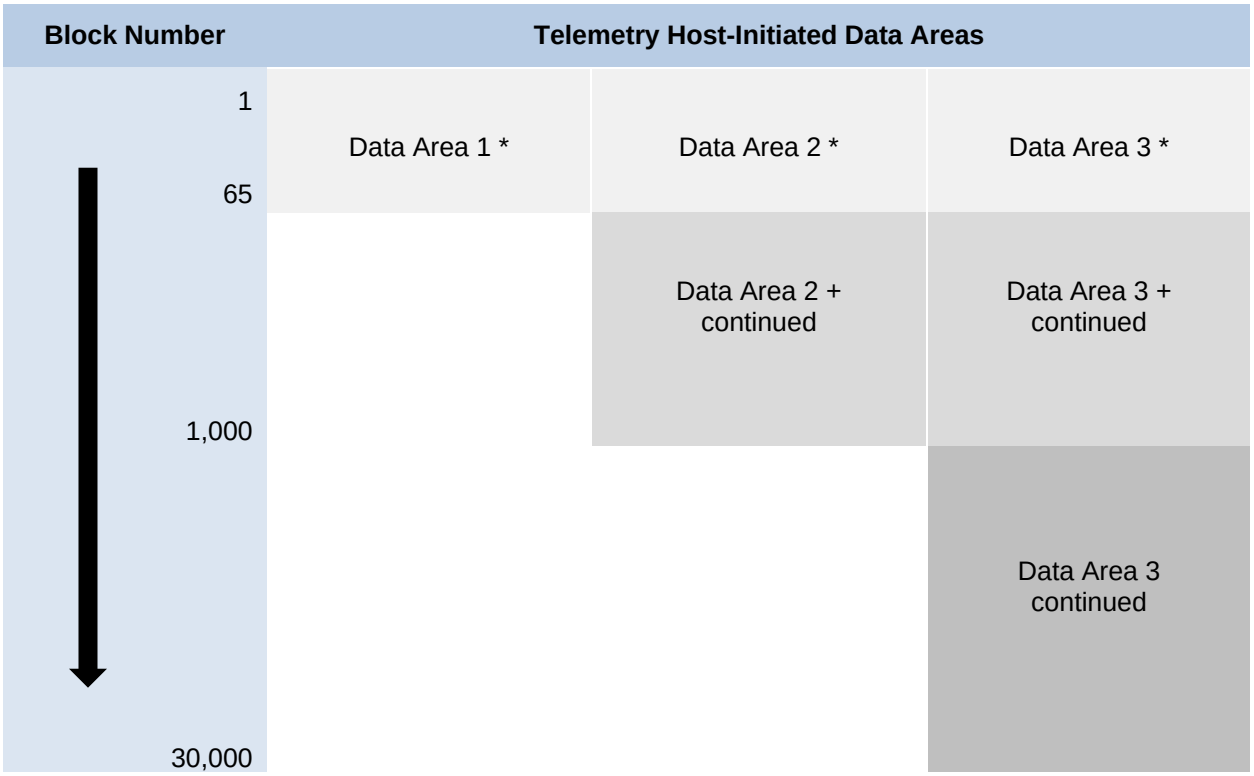
- Telemetry Host-Initiated Data Area 1 Last Block = 0;
- Telemetry Host-Initiated Data Area 2 Last Block = 0; and
- Telemetry Host-Initiated Data Area 3 Last Block = 0.

When all three telemetry data areas are populated, then the Telemetry Host-Initiated log page has different values in each of the Telemetry Host-Initiated Data Area n Last Block fields. For example, the following values correspond to the layout shown in Figure 482:

- Telemetry Host-Initiated Data Area 1 Last Block = 65;
- Telemetry Host-Initiated Data Area 2 Last Block = 1,000; and
- Telemetry Host-Initiated Data Area 3 Last Block = 30,000.

As a result of telemetry data areas being made up of a single set of Telemetry Data Blocks starting at Telemetry Data Block 1, the telemetry data contained in Telemetry Data Block 1 through Telemetry Data Block 65 of data area 1, data area 2, and data area 3 is the same. In addition, the telemetry data contained in Telemetry Data Block 66 through Telemetry Data Block 1,000 of data area 2 and data area 3 is the same.

Figure 482: Telemetry Log Example – All Data Areas Populated



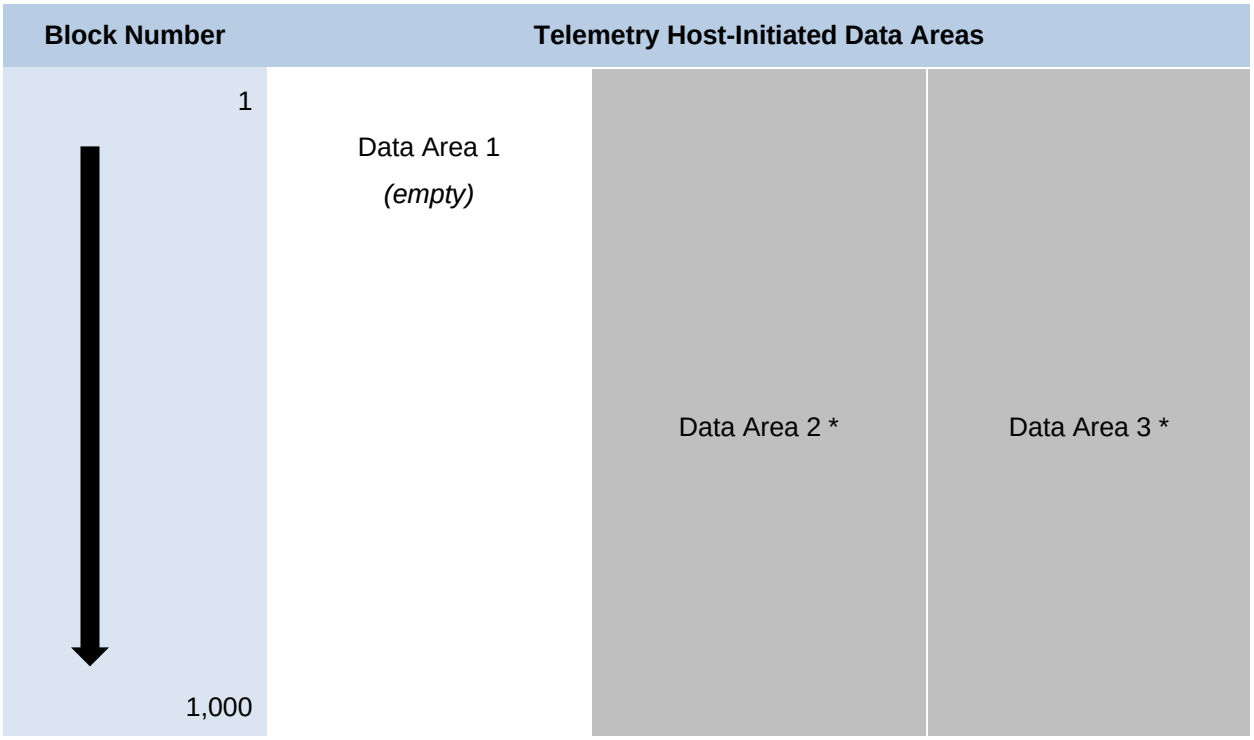
* Data Area 1, Data Area 2, and Data Area 3 contain the same telemetry data in blocks 1 through 65.
\+ Data Area 2 and Data Area 3 contain the same telemetry data in blocks 66 through 1,000.

When only the second data areas is populated, then the Telemetry Host-Initiated log page has no data in Telemetry Data Area 1 shown by having its corresponding last block value cleared to 0h, and no additional data in Telemetry Data Area 3 shown by having its corresponding last block value set to the same value as the last block value for Telemetry Data Area 2. For example, the following values correspond to the layout shown in Figure 483:

- Telemetry Host-Initiated Data Area 1 Last Block = 0;
- Telemetry Host-Initiated Data Area 2 Last Block = 1,000; and
- Telemetry Host-Initiated Data Area 3 Last Block = 1,000.

As a result of telemetry data areas being made up of a single set of Telemetry Data Blocks starting at Telemetry Data Block 1, the telemetry data contained in Telemetry Data Block 1 through Telemetry Data Block 1,000 of data area of data area 2 and data area 3 is the same.

Figure 483: Telemetry Log Example – Data Area 2 Populated



* Data Area 2, and Data Area 3 contain the same telemetry data in blocks 1 through 1,000.

8.15 Sanitize Operations (Optional)

A sanitize operation alters all user data in the NVM subsystem such that recovery of any previous user data from any cache, the non-volatile media, or any Controller Memory Buffer is not possible. It is implementation specific whether Submission Queues and Completion Queues within a Controller Memory Buffer are altered by a sanitize operation; all other data stored in all Controller Memory Buffers is altered by a sanitize operation. If a portion of the user data was not altered and the sanitize operation completed successfully, then the NVM subsystem shall ensure permanent inaccessibility of that portion of the user data for any future use within the NVM subsystem (e.g., retrieval from NVM media, caches, or any Controller Memory Buffer) and permanent inaccessibility of that portion of the user data via any interface to the NVM subsystem, including management interfaces such as NVMe-MI implementation.

The scope of a sanitize operation is all locations in the NVM subsystem that are able to contain user data, including caches, Persistent Memory Regions, and unallocated or deallocated areas of the media. Sanitize operations do not affect the Replay Protected Memory Block, boot partitions, or other media and caches that do not contain user data. A sanitize operation also may alter log pages as necessary (e.g., to prevent derivation of user data from log page information). Once started, a sanitize operation is not able to be aborted and continues after a Controller Level Reset including across power cycles. Refer to Annex A for further information about sanitize operations.

The Sanitize command (refer to section 5.24) is used to start a sanitize operation or to recover from a previously failed sanitize operation. All sanitize operations are performed in the background (i.e., completion of the Sanitize command does not indicate completion of the sanitize operation). The completion of a sanitize operation is indicated in the Sanitize Status log page, and with either the Sanitize Operation Completed asynchronous event or the Sanitize Operation Completed With Unexpected Deallocation asynchronous event (if an Asynchronous Event Request Command is outstanding).

The Sanitize Capabilities field of the Identify Controller data structure indicates the sanitize operation types supported and controller attributes specific to sanitize operations.

The sanitize operation types are:

- The Block Erase sanitize operation alters user data with a low-level block erase method that is specific to the media for all locations on the media within the NVM subsystem in which user data may be stored;
- The Crypto Erase sanitize operation alters user data by changing the media encryption keys for all locations on the media within the NVM subsystem in which user data may be stored; and
- The Overwrite sanitize operation alters user data by writing a fixed data pattern or related patterns to all locations on the media within the NVM subsystem in which user data may be stored one or more times. Figure 484 defines the data pattern or patterns that are written.

Controller attributes specific to sanitize operations include:

- The No-Deallocate Modifies Media After Sanitize (NODMMAS) field which indicates if media is modified by the controller after a sanitize operation successfully completes that had been requested with No-Deallocate After Sanitize set to '1' in the Sanitize command that started the sanitize operation; and
- No-Deallocate Inhibited (NDI) bit which indicates if the controller supports the No-Deallocate After Sanitize bit in the Sanitize Command.

The NODMMAS field in the Identify Controller data structure (refer to Figure 251), specifies that if a Sanitize command includes No-Deallocate After Sanitize set to '1' and NODMMAS is set to 10b, then a sanitize operation has an associated additional media modification operation. This additional media modification operation acts upon the results of the requested sanitize operation with the purpose of making all LBA contents readable. Refer to Annex A for further information about sanitize operations and interactions with integrity circuits.

This additional media modification shall complete before the NVM subsystem:

a) reports sanitize completion by Asynchronous Event (refer to section 5.2); and
b) reports sanitize completion in the Sanitize Status log (refer to section 5.14.1.16.2).

The Overwrite sanitize operation is media specific and may not be appropriate for all media types. For example, if the media is NAND, multiple pass overwrite operations may have an adverse effect on media endurance.

Figure 484: Sanitize Operations – Overwrite Mechanism

OIPBP[1]	Overwrite Pass Count[1]	Overwrite Pass Number	User Data except PI Metadata	Protection Information[2]
'0'	All	All	Overwrite Pattern[1]	FFFFFFFF_FFFFFFFFh
'1'	Even	First	Inversion of Overwrite Pattern[1]	00000000_00000000h
		Subsequent	Inversion of Overwrite Pattern[1] from previous pass (i.e., each bit XORed with '1')	
'1'	Odd	First	Overwrite Pattern[1]	FFFFFFFF_FFFFFFFFh
		Subsequent	Inversion of Overwrite Pattern[1] from previous pass (i.e., each bit XORed with '1')	

NOTES:
1. Parameters are specified in Command Dword 10 and Command Dword 11 of the corresponding Sanitize command that started the Overwrite operation. The Overwrite Invert Pattern Between Passes (OIPBP) field is defined in Command Dword 10. The Overwrite Pass Count is defined in Command Dword 10. The Overwrite Pattern is defined in Command Dword 11. Refer to section 5.24.
2. If Protection Information is present within the metadata.

To start a sanitize operation, the host submits a Sanitize command specifying one of the sanitize operation types (i.e., Block Erase, Overwrite, or Crypto Erase). The host sets command parameters, including the Allow Unrestricted Sanitize Exit bit and the No-Deallocate After Sanitize bit. After validating the Sanitize command parameters, the controller starts the sanitize operation in the background, updates the Sanitize Status log page and then completes the Sanitize command with Successful Completion status. If the sanitize operation is to be followed by an associated additional media modification operation (refer to NODMMAS in Figure 251), then the associated additional media modification operation shall be completed before the controller reports sanitize operation complete. If a Sanitize command is completed with any status other than Successful Completion, then the controller shall not start the sanitize operation and shall not update the Sanitize Status log page. The controller ignores Critical Warning(s) in the SMART / Health Information log page (e.g., read only mode) and attempts to complete the sanitize operation requested. While a sanitize operation is in progress, all controllers shall abort any commands not listed in Figure 486 with a status of Sanitize In Progress (refer to section 8.15.1).

The user data values that result from a successful sanitize operation are specified in Figure 485. If the controller deallocates user data after successful completion of a sanitize operation, then values read from deallocated logical blocks are described in section 6.7.1.1. The host may specify that sanitized logical blocks not be deallocated by setting the No-Deallocate After Sanitize bit to '1' in the Sanitize command.

Figure 485: Sanitize Operations – User Data Values

Sanitize Operation	Logical Blocks
Block Erase	Vendor specific value
Crypto Erase	Indeterminate
Overwrite	Refer to Figure 484

The Sanitize Status log page (refer to section 5.14.1.16.2) contains estimated times for sanitize operations and a consistent snapshot of information about the most recently started sanitize operation, including whether a sanitize operation is in progress, the sanitize operation parameters and the status of the most recent sanitize operation. The controller shall report sanitize operation in progress if either a sanitize operation is in progress or an associated additional media modification operation is in progress. If a sanitize operation is not in progress, then the Global Data Erased bit in the log page indicates whether the NVM subsystem may contain any user data (i.e., has not been written to since the most recent successful sanitize operation).

The Sanitize Status log page shall be updated as described:

- Initialize before any controller in the NVM subsystem is ready;
- Update before a Sanitize command that starts a sanitize operation is completed (i.e., prior to the completion queue entry being posted for the Sanitize command); and
- Update when a sanitize operation is complete (e.g., immediately prior to the completion queue entry being posted for the Sanitize Operation Completed asynchronous event or for the Sanitize Operation Completed With Unexpected Deallocation asynchronous event).

The Sanitize Status log page should be updated periodically during a sanitize operation to make progress information available to hosts.

During a sanitize operation, the host may periodically examine the Sanitize Status log page to check for progress, however, the host should limit this polling (e.g., to at most once every several minutes) to avoid interfering with the progress of the sanitize operation itself.

On completion of a sanitize operation:

- If the sanitize operation is successful, then the Global Data Erased bit shall be set to '1';
- The Sanitize Status log page is updated;
- The controller to which the Sanitize command was submitted completes an Asynchronous Event Request command (if one is outstanding) with the following information:
    - The Log Page Identifier field is set to 81h (i.e., Sanitize Status);

  - The Asynchronous Event Information field is set to Sanitize Operation Completed or to Sanitize Operation Completed With Unexpected Deallocation asynchronous event (refer to section 5.2); and
  - The Asynchronous Event Type field is set to 110b (i.e., I/O Command Set specific status); and
- All controllers in the NVM subsystem may resume any power management that was suspended when the sanitize operation started.

The host should read the Sanitize Status log page upon completion of a sanitize operation (which clears the asynchronous event, if one was generated).

If a sanitize operation fails, all controllers in the NVM subsystem shall abort any command not allowed during a sanitize operation with a status of Sanitize Failed (refer to section 8.15.1) until a subsequent sanitize operation is started or successful recovery from the failed sanitize operation occurs. A subsequent successful sanitize operation or the Exit Failure Mode action may be used to recover from a failed sanitize operation. Refer to section 5.24 for recovery details.

If the Sanitize command is supported, then the NVM subsystem and all controllers shall:

- Support the Sanitize Status log page;
- Support the Sanitize Operation Completed asynchronous event;
- Support the Sanitize Operation Completed With Unexpected Deallocation asynchronous event, if the Sanitize Config feature is supported;
- Support the Exit Failure Mode action for a Sanitize command;
- Support at least one of the following sanitize operation types: Block Erase, Overwrite, or Crypto Erase;
- Support the same set of sanitize operation types; and
- Indicate the supported sanitize operation types in the Sanitize Capabilities field in the Identify Controller data structure.

The Sanitize Config Feature Identifier (refer to section 5.21.1.23) contains the No-Deallocate Response Mode bit that specifies the response of the controller to a Sanitize command processed with the No-Deallocate After Sanitize bit (refer to Figure 334) set to ‘1’ if the No-Deallocate Inhibited bit in the Sanitize Capabilities field of the Identify Controller data structure (refer to Figure 251) is set to ‘1’. In the No-Deallocate Error Response Mode, the controller aborts such Sanitize commands with a status of Invalid Field in Command. In the No-Deallocate Warning Response Mode, the controller processes such Sanitize commands, and if a resulting sanitize operation is completed successfully, then bits 2:0 of the Sanitize Status field in the Sanitize Status log page are set to 100b (refer to Figure 242).

8.15.1 Sanitize Command Restrictions

While performing a sanitize operation and while a failed sanitize operation has occurred but successful recovery from that failure has not occurred, all enabled controllers and namespaces in the NVM subsystem are restricted to performing only a limited set of actions.

While a sanitize operation is in progress:

- All controllers in the NVM subsystem shall only process the Admin commands listed in Figure 486 subject to the additional restrictions stated in that figure;
- All I/O Commands other than a Flush command shall be aborted with a status of Sanitize In Progress;
- Processing of a Flush command is specified in section 6.8;
- Any command or command option that is not explicitly permitted in Figure 486 shall be aborted with a status of Sanitize In Progress if fetched by any controller in the NVM subsystem; and
- The Persistent Memory Region shall be prevented from being enabled (i.e., setting PMRCTL.EN to ‘1’ does not result in PMRSTS.NRDY being cleared to ‘0’).

While a failed sanitize operation has occurred, a subsequent sanitize operation has not started and successful recovery from the failed sanitize operation has not occurred:

- All controllers in the NVM subsystem shall only process the Sanitize command (refer to section 5.24) and the Admin commands listed in Figure 486 subject to the additional restrictions noted in that figure;
- All I/O Commands shall be aborted with a status of Sanitize Failed;
- The Sanitize command is permitted with action restrictions (refer to section 5.24);
- Aside from the Sanitize command, any other command or command option that is not explicitly permitted in Figure 486 shall be aborted with a status of Sanitize Failed if fetched by any controller in the NVM subsystem; and
- The Persistent Memory Region shall be prevented from being enabled (i.e., setting PMRCTL.EN to '1' does not result in PMRSTS.NRDY being cleared to '0').

Figure 486: Sanitize Operations – Admin Commands Allowed

<table>
<tr><th>Admin Command</th><th>Additional Restrictions</th></tr>
<tr><td>Abort</td><td></td></tr>
<tr><td>Asynchronous Event Request</td><td></td></tr>
<tr><td>Create I/O Completion Queue</td><td></td></tr>
<tr><td>Create I/O Submission Queue</td><td></td></tr>
<tr><td>Delete I/O Completion Queue</td><td></td></tr>
<tr><td>Delete I/O Submission Queue</td><td></td></tr>
<tr><td>Get Features</td><td></td></tr>
<tr><td>Get Log Page</td><td>The log pages allowed are listed below.
<table>
<tr><th>Log Pages</th><th>Additional Restrictions</th></tr>
<tr><td>Error Information</td><td>Return zeroes in the LBA field.</td></tr>
<tr><td>SMART / Health Information</td><td></td></tr>
<tr><td>Changed Namespace List</td><td></td></tr>
<tr><td>Reservation Notification</td><td></td></tr>
<tr><td>Sanitize Status</td><td></td></tr>
<tr><td>Asymmetric Namespace Access</td><td></td></tr>
</table></td></tr>
<tr><td>Identify</td><td></td></tr>
<tr><td>Keep Alive</td><td></td></tr>
<tr><td>NVMe-MI Receive</td><td rowspan="2">Prohibited unless explicitly allowed in the NVM Express Management Interface Specification.</td></tr>
<tr><td>NVMe-MI Send</td></tr>
<tr><td>Set Features</td><td>Namespace Write Protection Config Feature is not allowed.</td></tr>
<tr><td>Opcode 7Fh</td><td>The Fabric Commands allowed are listed below. Refer to the NVMe over Fabrics specification.
<table>
<tr><th>Fabrics Commands</th><th>Additional Restrictions</th></tr>
<tr><td>Property Set</td><td></td></tr>
<tr><td>Connect</td><td></td></tr>
<tr><td>Disconnect</td><td></td></tr>
<tr><td>Property Get</td><td></td></tr>
<tr><td>Authentication Send</td><td></td></tr>
<tr><td>Authentication Receive</td><td></td></tr>
<tr><td>Vendor Specific</td><td>Commands are allowed that do not affect or retrieve user data.</td></tr>
</table></td></tr>
<tr><td>Vendor Specific</td><td>Commands are allowed that do not affect or retrieve user data.</td></tr>
</table>

8.16 Read Recovery Level (Optional)

The Read Recovery Level (RRL) is a NVM Set configurable attribute that balances the completion time for read commands and the amount of error recovery applied to those read commands. The Read Recovery Level applies to an NVM Set with which the Read Recovery Level is associated. A namespace created within an NVM Set inherits the Read Recovery Level of that NVM Set. If NVM Sets are not supported, all namespaces in the NVM subsystem use an identical Read Recovery Level.

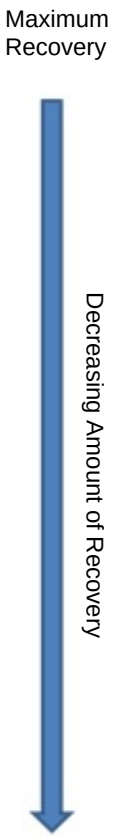
The controller indicates support for Read Recovery Levels in the Controller Attributes field in the Identify Controller data structure (refer to Figure 251). If Read Recovery Levels are supported, then the specific levels supported are indicated in the Read Recovery Levels Supported field in the Identify Controller data structure. There are 16 levels that may be supported. Level 0, if supported, provides the maximum amount of recovery. Level 4 is a mandatory level that provides a nominal amount of recovery and is the default level. Level 15 is a mandatory level that provides the minimum amount of recovery and is referred to as the 'Fast Fail' level. The levels are organized based on the amount of recovery supported, such that a higher numbered level provides less recovery than the preceding lower level.

Interactions between the Read Recovery Level and the Limited Retry (LR) field in I/O commands are implementation specific.

The Read Recovery Level may be configured using a Set Features command for the Read Recovery Level Config Feature. The Read Recovery Level may be determined using a Get Features command for the Read Recovery Level Config Feature.

Figure 487: Read Recovery Level Overview

Level	O/M	Description
0	O	
1	O	
2	O	
3	O	
4	M	Default
5	O	
6	O	
7	O	
8	O	
9	O	
10	O	
11	O	
12	O	
13	O	
14	O	
15	M	Fast Fail



If Read Recovery Levels are supported, then the NVM subsystem and all controllers shall:

- Support at least Level 4 and Level 15;
- Indicate support for Read Recovery Levels in the Controller Attributes field in the Identify Controller data structure;
- Support the Read Recovery Levels Supported field in the Identify Controller data structure; and

- Support the Read Recovery Level Config Feature.

8.17 Endurance Groups (Optional)

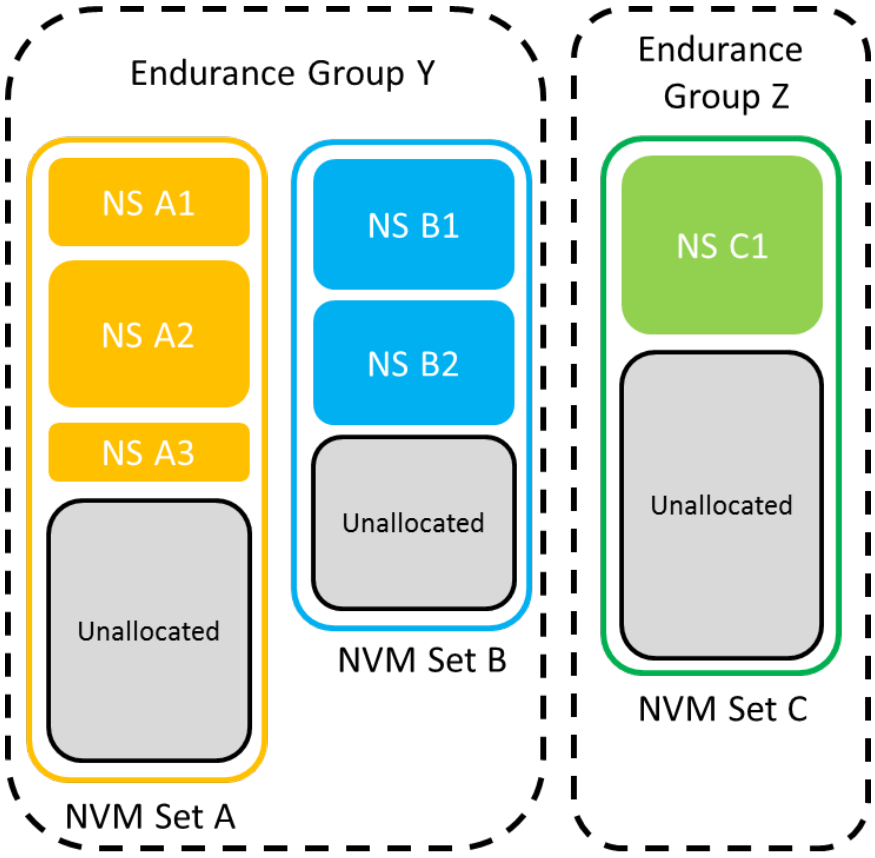
Endurance may be managed within a single NVM Set (refer to section 4.9) or across a collection of NVM Sets. Each NVM Set is associated with an Endurance Group (refer to Figure 254). If two or more NVM Sets have the same Endurance Group Identifier, then endurance is managed by the NVM subsystem across that collection of NVM Sets. If only one NVM Set is associated with a specific Endurance Group Identifier, then endurance is managed locally to that NVM Set.

An Endurance Group Identifier is a 16-bit value that specifies the Endurance Group with which an action is associated. An Endurance Group Identifier value of 0h is reserved and is not a valid Endurance Group Identifier. Unless otherwise specified, if the host specifies an Endurance Group Identifier cleared to 0h for a command that requires an Endurance Group Identifier, then that command shall abort with a status code of Invalid Field in Command.

The endurance information for an Endurance Group is specified in the Endurance Group Information log page (refer to section 5.14.1.9).

Figure 488 shows Endurance Groups added to the example in Figure 135. In this example, the endurance of NVM Set A and NVM Set B are managed together as part of Endurance Group Y, while the endurance of NVM Set C is managed only within NVM Set C which is the only NVM Set that is part of Endurance Group Z.

Figure 488: NVM Sets and Associated Namespaces



If Endurance Groups are supported, then the NVM subsystem and all controllers shall:

- Indicate support for Endurance Groups in the Controller Attributes field in the Identify Controller data structure;
- Indicate the Endurance Group Identifier with which the namespace is associated in the Identify Namespace data structure; and
- Support the Endurance Group Information log page.

8.17.1 Configuring and Managing Events

The host may configure asynchronous events to be triggered when certain events occur for an Endurance Group. The host submits a Set Features command specifying the Endurance Group Event Configuration feature (refer to section 5.21.1.24), the Endurance Group, and the specific event(s) that shall trigger adding an entry to the Endurance Group Event Aggregate log page (refer to section 5.14.1.15).

The host configures events using a Set Features command for each Endurance Group.

The host submits a Set Features command specifying the Asynchronous Event Configuration feature (refer to section 5.21.1.11) with the Endurance Group Event Aggregate Log Change Notices bit set to '1' to specify that adding an entry to the Endurance Group Event Aggregate log page shall trigger an Endurance Group Event Aggregate Log Page Change Notice event to the host (refer to Figure 319).

The host determines the Endurance Groups that have outstanding events by reading the Endurance Group Event Aggregate log page. An entry is returned for each Endurance Group that has an event outstanding. The host may use the Endurance Group Identifier Maximum value reported in the Identify Controller data structure to determine the maximum size of this log page.

To determine the specific event(s) that have occurred for a reported Endurance Group, the host reads the Endurance Group log page for that Endurance Group. The Critical Warning field indicates the event(s) that have occurred (e.g., that all namespaces in the Endurance Group have been placed in read-only mode). All events for an Endurance Group are cleared if the controller successfully processes a read for the Endurance Group Information log page for that Endurance Group, where the Get Log Page command has the Retain Asynchronous Event bit cleared to '0'. If the Critical Warning field in the Endurance Group Information log page is cleared to 0h, then events for that Endurance Group are not reported in the Endurance Group Event Aggregate log page.

8.18 Predictable Latency Mode (Optional)

Predictable Latency Mode is used to achieve predictable latency for read and write operations. When configured to operate in this mode using the Predictable Latency Mode Config Feature, the namespaces in an NVM Set (refer to section 4.9) provide windows of operation for deterministic operation or non-deterministic operation.

When Predictable Latency Mode is enabled:

- NVM Sets and their associated namespaces have vendor specific quality of service attributes;
- I/O commands that access NVM in the same NVM Set have the same quality of service attributes; and
- I/O commands that access NVM in one NVM Set do not impact the quality of service of I/O commands that access NVM in a different NVM Set.

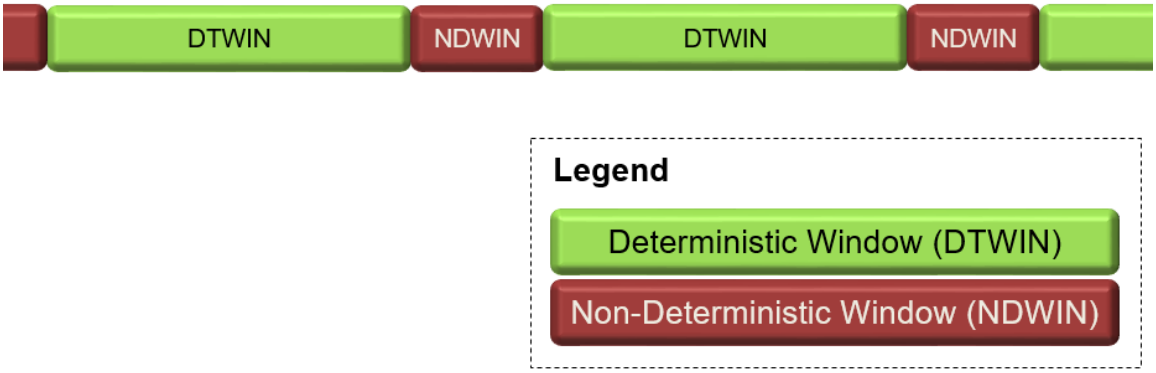
The quality of service attributes apply within the NVM subsystem and do not include the PCIe or fabric connection. To enhance isolation, the host should submit I/O commands for different NVM Sets to different I/O Submission Queues.

Read Recovery Levels (refer to section 8.16) shall be supported when Predictable Latency Mode is supported. The host configures the Read Recovery Level to specify the tradeoff between the quality of service versus the amount of error recovery to apply for a particular NVM Set.

The Deterministic Window (DTWIN) is the window of operation during which the NVM Set is able to provide deterministic latency for read and write operations. The Non-Deterministic Window (NDWIN) is the window of operation during which the NVM Set is not able to provide deterministic latency for read and write

operations as a result of preparing for a subsequent Deterministic Window. Examples of actions that may be performed in the Non-Deterministic Window include background operations on the non-volatile media. The current window that an NVM Set is operating in is configured by the host using the Predictable Latency Mode Window Feature or by the controller as a result of an autonomous action.

Figure 489: Deterministic and Non-Deterministic Windows



To remain in the Deterministic Window, the host is required to follow operating rules (refer to section 8.18.1) ensuring that certain attributes do not exceed the typical or maximum values indicated in the Predictable Latency Per NVM Set log page. If the attributes exceed any of the typical or maximum values indicated in the Predictable Latency Per NVM Set log page or a Deterministic Excursion occurs, then the associated NVM Set may autonomously transition to the Non-Deterministic Window. A Deterministic Excursion is a rare occurrence in the NVM subsystem that requires immediate action by the controller.

The host configures Predictable Latency Events to report using the Predictable Latency Mode Config feature. The host may configure a Predictable Latency Event to be triggered when that value exceeds a specific value in order to manage window changes and avoid autonomous transitions by the controller. Refer to section 8.18.3.

If Predictable Latency Mode is supported, then all controllers in the NVM subsystem shall:

- Support one or more NVM Sets;
- Support Read Recovery Levels;
- Support the Predictable Latency Mode log page for each NVM Set;
- Support the Predictable Latency Event Aggregate log page;
- Support the Predictable Latency Mode Config Feature;
- Support the Predictable Latency Mode Window Feature;
- Support Predictable Latency Event Aggregate Log Change Notices; and
- Indicate support for Predictable Latency Mode in the Controller Attributes field in the Identify Controller data structure.

8.18.1 Host Operating Rules to Achieve Determinism

In order to achieve deterministic operation, the host is required to follow operating rules.

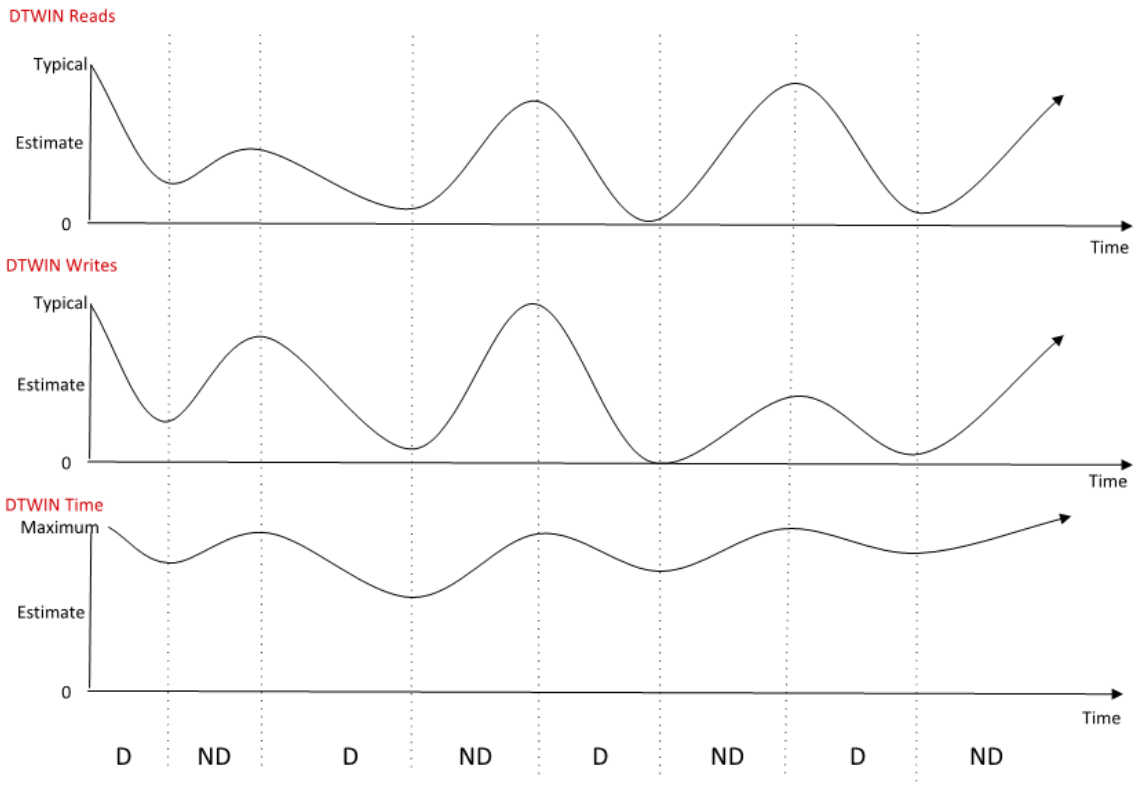
An NVM Set remains in the Deterministic Window while attributes do not exceed any of the typical or maximum values indicated in the Predictable Latency Per NVM Set log page, there is not a Deterministic Excursion, and the host does not request a transition to the Non-Deterministic Window. The attributes specified in this specification are the number of random 4 KiB reads, the number of writes in Optimal Write Size, and time in the Deterministic Window. Additional attributes are vendor specific.

For reads, writes, and time in the Deterministic Window, two values are provided in the Predictable Latency Per NVM Set log page (refer to section 5.14.1.10):

- A typical or maximum amount of that attribute that the host may consume during any given DTWIN; and
- A reliable estimate of the amount of that attribute that remains to be consumed during the current DTWIN.

Figure 490 shows how the Typical, Maximum, and Reliable Estimates for the DTWIN attributes increase or decrease when the associated NVM Set is in the Deterministic Window or Non-Deterministic Window.

Figure 490: DTWIN Attributes and Estimates

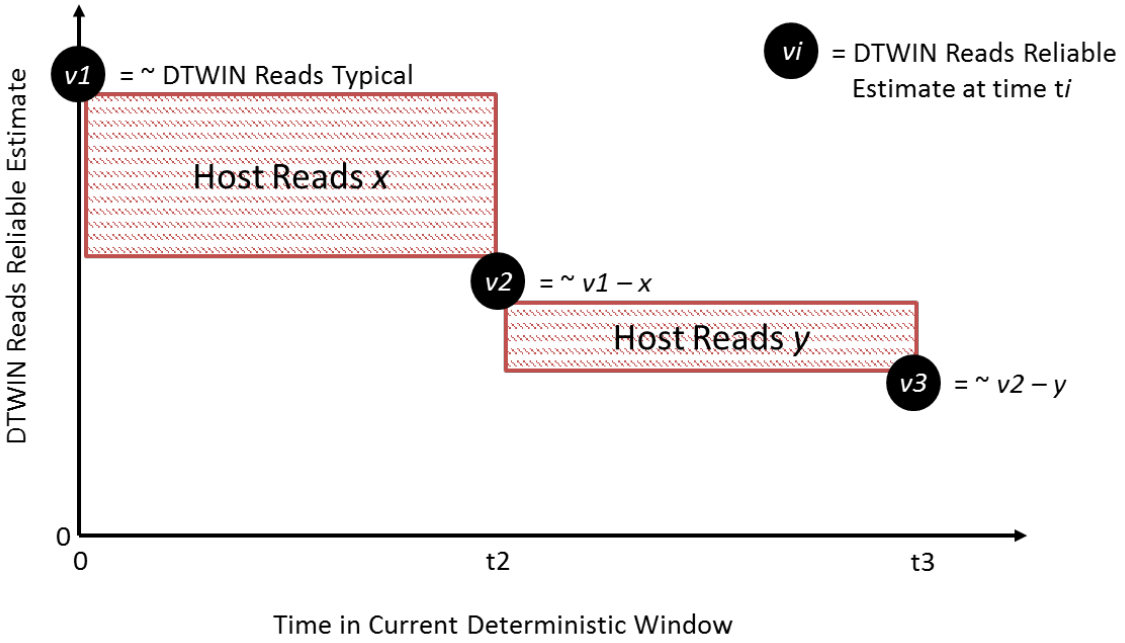


An NVM Set may transition autonomously to the NDWIN if, since entry to the current DTWIN:

a) the number of reads is greater than the value indicated in the DTWIN Reads Typical field;
b) the number of writes is greater than the value indicated in the DTWIN Writes Typical field;
c) the amount of time indicated in the DTWIN Time Maximum field has passed; or
d) a Deterministic Excursion occurs.

Figure 491 is an example that shows the relationship between the typical and reliable estimate values for DTWIN Reads. DTWIN Reads Reliable Estimate begins near the DTWIN Reads Typical value at the start of the current DTWIN at time 0. During the first time increment, the host reads *x* units, and the value of the reliable estimate at time t2 is decremented by approximately *x*. During the second time increment, the host reads a smaller amount consisting of *y* units and thus the reliable estimate at t3 is decremented by approximately *y*.

Figure 491: Typical and Reliable Estimate Example



The host configures the current window to be either DTWIN or NDWIN using a Set Features command with the Predictable Latency Mode Window Feature. The host may use the reliable estimates provided in the Predictable Latency Mode log page to ensure that the host transitions the NVM Set to the NDWIN prior to any reliable estimates exceeding one of the typical or maximum values (e.g., DTWIN Reads Estimate = 0).

The reliable estimates provided shall have the following properties when in the Deterministic Window:

- The estimates shall be monotonically decreasing towards 0h for the entirety of the DTWIN, depending on the attribute. For example, DTWIN Reads Reliable Estimate is monotonically decreasing and thus does not increase without transitioning from the DTWIN to the NDWIN; and
- The estimates shall not change abruptly unless operating conditions have changed abruptly. The estimate should be based on averaging or smoothing of data collected over some period of time.

8.18.2 Configuring Periodic Windows

When using the NVM Set in Predictable Latency Mode, the host should transition the controller to NDWIN for periodic maintenance. The maintenance is required in order for the NVM subsystem to reliably provide the amount of time indicated for Deterministic Windows.

There are three static time based parameters reported in the Predictable Latency Per NVM Set log page (refer to section 5.14.1.10) that may be used by the host to configure periodic windows. The values provided are worst case for the life of the NVM subsystem:

- NDWIN Time Minimum Low is the minimum time that the NVM Set remains in the Non-Deterministic Window. The controller may delay completion of a Set Features command requesting a transition to the Deterministic Window until this time is completed. This time does not account for additional host activity in the Non-Deterministic Window;
- NDWIN Time Minimum High is the minimum time that the host should allow the NVM Set to remain in the Non-Deterministic Window after the NVM Set remained in the previous Deterministic Window

for DTWIN Time Maximum. This time does not account for additional host activity in the Non-Deterministic Window; and

- DTWIN Time Maximum is the maximum time that the NVM Set is able to stay in a Deterministic Window.

The DTWIN Time Maximum and NDWIN Time Minimum High may provide a ratio of the amount of maintenance that needs to be performed based on the time that the NVM Set remains in the DTWIN, assuming no threshold is exceeded. Any scaling of the time in the Non-Deterministic Window based on the read, write, and time behavior in the previous Deterministic Window is implementation dependent.

The DTWIN Time Estimate may be used by the host when a Deterministic Excursion has occurred. This estimate allows the host to re-synchronize an NVM Set with other NVM Sets operating in Predictable Latency Mode, if applicable.

8.18.3 Configuring and Managing Events

The host may configure events to be triggered when thresholds do not exceed certain levels or when autonomous transitions occur using the Predictable Latency Mode Feature. The host submits a Set Feature for the particular NVM Set and configures the specific event(s) and threshold(s) values that shall trigger a Predictable Latency Event Aggregate Log Change Notice event for that particular NVM Set to the host. Refer to Figure 313.

The host determines the NVM Sets that have outstanding events by reading the Predictable Latency Event Aggregate log page (refer to section 5.14.1.11). An entry is returned for each NVM Set that has an event outstanding. The host may use the NVM Set Identifier Maximum value reported in the Identify Controller data structure in order to determine the maximum size of this log page.

To determine the specific event(s) that have occurred for a reported NVM Sets, the host reads the Predictable Latency Per NVM Set log page (refer to section 5.14.1.10) for that NVM Set. The Event Type field indicates the event(s) that have occurred (e.g., an autonomous transition to the NDWIN). An event(s) for a particular NVM Set is cleared if the controller successfully processes a read for the Predictable Latency Per NVM Set log page for the affected NVM Set where the Get Log Page command has the Retain Asynchronous Event parameter cleared to ‘0’. If the Event Type field in the Predictable Latency Per NVM Set log page is cleared to 0h, then events for that particular NVM Set are not reported in the Predictable Latency Event Aggregate log page.

8.19 Namespace Write Protection (Optional)

Namespace Write Protection is an optional configurable controller capability that enables the host to control the write protection state of a namespace or to determine the write protection state of a namespace. Support for this capability is reported in the Namespace Write Protection Capabilities (NWPC) field in the Identify Controller data structure (refer to Figure 251 and section 5.15).

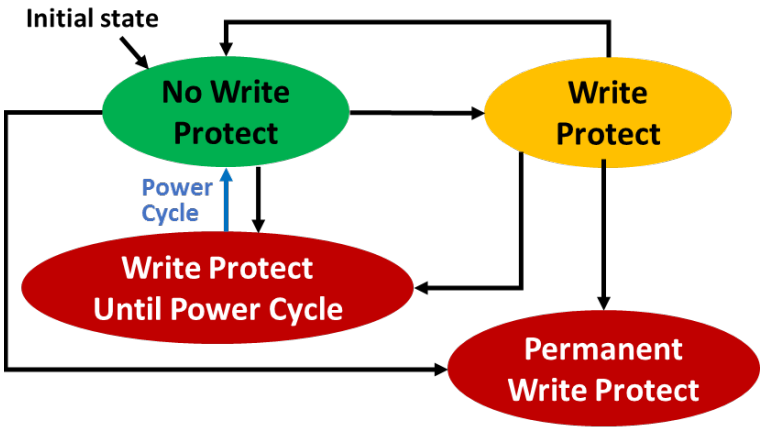
Figure 492 defines the write protection states that may be supported for a namespace. All states persist across power cycles and NVMe Controller Level Resets (refer to section 7.3) except Write Protect Until Power Cycle state, which transitions to the No Write Protect state on the occurrence of a power cycle.

Figure 492: Namespace Write Protection State Definitions

State	Definition	Persistent Across	
		Power Cycles	Controller Level Resets
No Write Protect	The namespace is not write protected.	Yes	Yes
Write Protect	The namespace is write protected.	Yes	Yes
Write Protect Until Power Cycle	The namespace is write protected until the next power cycle.	No	Yes
Permanent Write Protect	The namespace is permanently write protected.	Yes	Yes

Figure 493 defines the transition between write protection states. All state transitions are based on Set Features commands unless otherwise specified. The initial state of a namespace at the time of its creation is the No Write Protect state.

Figure 493: Namespace Write Protection State Machine Model



The Write Protect Until Power Cycle and Permanent Write Protect states are subject to the Namespace Write Protection Authentication Control mechanism, which determines whether the controller processes or aborts Set Features commands which cause a transition into either of these two states (refer to section 8.10).

The results of using Namespace Write Protection in combination with an external write protection system (e.g., TCG Storage Interface Interactions Specification) are outside the scope of this specification.

8.19.1 Namespace Write Protection – Theory of Operation

If Namespace Write Protection is supported by the controller, then the controller shall:

- Indicate the level of support for Namespace Write Protection capabilities in the Namespace Write Protection Capabilities (NWPC) field in the Identify Controller data structure; and
- Support the Namespace Write Protection Config Feature (refer to section 5.21.1.29).

If the Write Protect Until Power Cycle or the Permanent Write Protect states are supported by the controller, then the controller shall support the Namespace Write Protection Authentication Control field in the RPMB Device Configuration Block data structure (refer to section 8.10).

The controller shall not set the Critical Warning field, bit 3 (refer to Figure 198) to '1' if the read-only condition on the media is a result of a change in the namespace write protection state as defined by the Namespace Write Protection State Machine (refer to Figure 493), or due to any autonomous namespace write protection state transitions (e.g., power cycle). Host software may check the current namespace write protection state of a namespace using the Get Features command with the Namespace Write Protection Config Feature Identifier.

If any controller in the NVM subsystem supports Namespace Write Protection, then the write protection state of a namespace shall be enforced by any controller to which that namespace is attached.

8.19.1.1 Namespace Write Protection – Command Interactions

Unless otherwise noted, the commands listed in Figure 494 are processed normally when specifying an NSID for a namespace that is write protected.

Figure 494: Commands Allowed when Specifying a Write Protected NSID

Admin Command Set	NVM Command Set
Device Self–test	Compare
Directive Send [1]	Dataset Management [1]
Directive Receive [3]	Read
Get Features	Reservation Register
Get Log Page	Reservation Report
Identify	Reservation Acquire
Namespace Attachment	Reservation Release
Security Receive [1]	Vendor Specific [1]
Security Send [1]	Flush [2]
Set Features [1]	Verify
Vendor Specific [1]	

NOTES:
1. The controller shall fail commands if the specified action attempts to modify the medium of the specified namespace.
2. A Flush command shall complete successfully with no effect. All volatile write cache data and metadata associated with the specified namespace is written to non-volatile media as part of transitioning to the write protected state (refer to section 5.21.1.29).
3. A Directive Receive command which attempts to allocate streams resources shall be aborted with a status code of Namespace is Write Protected.

Commands not listed in Figure 494, and which meet the following conditions, shall be aborted with a status code of Namespace Is Write Protected (refer to Figure 128):

a) Commands that specify an NSID for a namespace that is write protected;
b) Commands that specify an NSID for a namespace that is not write protected and the execution of which would modify another namespace that is write protected (e.g., a Format NVM command); and
c) Commands that do not specify an NSID, and the execution of which would modify a namespace that is write protected (e.g., Sanitize command).

8.20 Asymmetric Namespace Access Reporting (Optional)

8.20.1 Asymmetric Namespace Access Reporting Overview

Asymmetric Namespace Access (ANA) occurs in environments where namespace access characteristics (e.g., performance or ability to access the media) may vary based on the controller used to access the namespace (e.g., Fabrics) and the internal configuration of the NVM subsystem. Asymmetric Namespace Access Reporting is used to indicate to the host information about those access characteristics.

Shared namespaces may be accessed through controllers via multiple PCIe ports (refer to section 1.4.1) or fabric ports (refer to the NVMe over Fabrics specification). The controllers that provide access to a shared namespace may provide identical access characteristics through all controllers (i.e., symmetric access), or may provide different access characteristics through some controllers (i.e., asymmetric access).

Private namespaces are accessed by only one controller at a time. The access characteristics of the namespace through that controller may be impacted as a result of changes to the internal configuration of the NVM subsystem. If the access characteristics of the namespace through that controller are impacted by the internal configuration of the NVM subsystem, then asymmetric access occurs.

Symmetric access to a namespace occurs when:

- the access characteristics using one controller are identical to the access characteristics when using a different controller; and
- changes to the internal configuration of the NVM subsystem do not impact the access characteristics.

Asymmetric access to a namespace occurs when:

- the access characteristics using one controller may differ from the access characteristics when using a different controller; or
- changes to the internal configuration of the NVM subsystem may impact the access characteristics.

While commands may be sent to a shared namespace through any attached controller with asymmetric access, the characteristics (e.g., performance or ability to access the media) may differ based on which controller is used; as a result, the host should consider those characteristics when selecting which controller to use for each command that accesses the namespace. The NVM subsystem may perform autonomous internal reconfiguration that results in a change to the access characteristics.

If an NVM subsystem supports Asymmetric Namespace Access Reporting, then all controllers in that NVM subsystem shall:

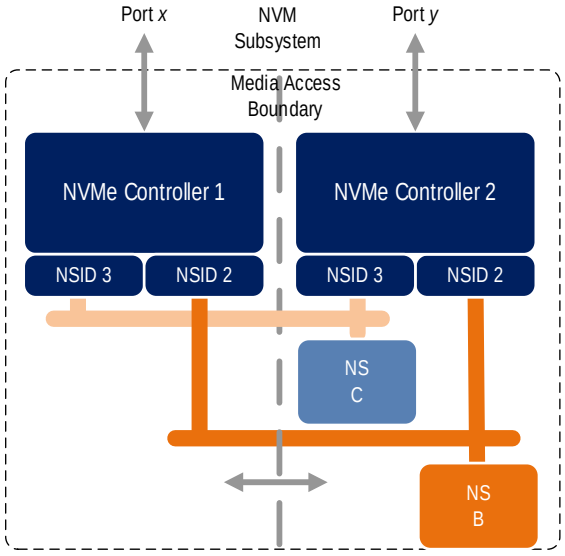
- set bit 3 to ‘1’ in the Controller Multi-path I/O and Namespace Sharing Capabilities (CMIC) field in the Identify Controller data structure (refer to Figure 251) to indicate support for Asymmetric Namespace Access Reporting;
- set bit 0 to ‘1’ in the Asymmetric Namespace Access Capabilities (ANACAP) field in the Identify Controller data structure to indicate that the ANA Optimized state is able to be reported;
- set bit 1 to ‘1’ in the ANACAP field in the Identify Controller data structure if ANA Non-Optimized state is able to be reported;
- set bit 2 to ‘1’ in the ANACAP field in the Identify Controller data structure if ANA Inaccessible state is able to be reported;
- set bit 3 to ‘1’ in the ANACAP field in the Identify Controller data structure if ANA Persistent Loss state is able to be reported;
- set bit 4 to ‘1’ in the ANACAP field in the Identify Controller data structure if ANA Change state is able to be reported;
- support Asymmetric Namespace Access Change Notices (refer to section 5.21.1.11); and
- support the Asymmetric Namespace Access log page (refer to section 5.14.1.12).

Namespaces attached to a controller that supports Asymmetric Namespace Access Reporting shall:

- be members of an ANA Group; and
- supply a valid ANA Group Identifier in the ANA Group Identifier (ANAGRPID) field in the Identify Namespace data structure (refer to Figure 249).

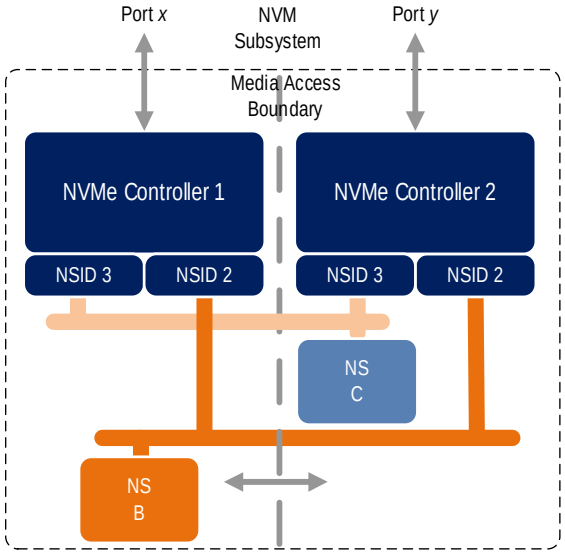
Figure 495 shows an example of an NVM subsystem where access characteristics vary as a result of the presence of two independent domains. In this example, the non-volatile media for namespace B and for namespace C are contained within the same domain that contains controller 2. As a result, controller 2 provides optimized access to namespace B and to namespace C while controller 1 does not provide optimized access to namespace B or to namespace C.

Figure 495: Namespace B and C optimized through Controller 2



To provide optimized access to namespace B through controller 1, the NVM subsystem may be administratively reconfigured, or may perform autonomous internal reconfiguration actions that change the access characteristics of namespace B when accessed through controller 1 and controller 2 as shown in Figure 496. Controller 2 provides optimized access to namespace C while controller 1 provides optimized access to namespace B.

Figure 496: Namespace B optimized through Controller 1



8.20.2 ANA Groups

Namespaces that are members of the same ANA Group perform identical asymmetric namespace access state transitions. The ANA Group maintains the same asymmetric namespace access state for all namespaces that are members of that ANA Group (i.e., a change in the asymmetric namespace access state of one namespace only occurs as part of a change in the asymmetric namespace access state of all

namespaces that are members of that ANA Group). The method for assigning namespaces to ANA Groups is outside the scope of this specification.

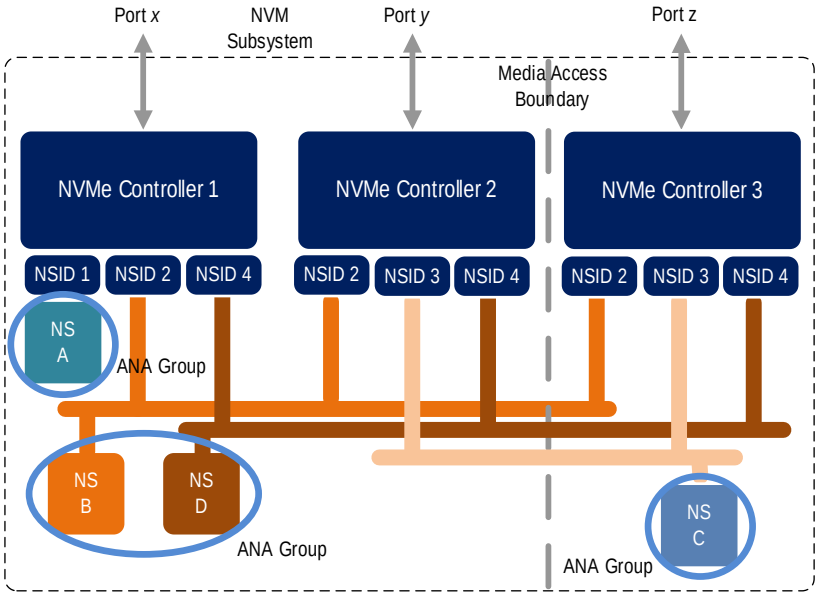
A valid ANA Group Identifier is a non-zero value that is less than or equal to ANAGRPMAX (refer to Figure 251).

The ANA Group Identifier (ANAGRPID) for each ANA Group shall be unique within the NVM subsystem. If bit 6 in the ANACAP field in the Identify Controller data structure is set to '1', then the ANA Group Identifier shall not change while the namespace is attached to any controller in the NVM subsystem. If bit 6 in the ANACAP field is cleared to '0', then the ANA Group Identifier may change while the namespace is attached to any controller in the NVM subsystem. If the ANA Group Identifier changes, the controller shall issue the Asymmetric Namespace Access Change Notice as described in 8.20.3.6.

Figure 497 shows the following four namespaces:

- the private namespace A in a first ANA Group;
- namespace B and namespace D, that are in the same second ANA Group; and
- namespace C that is in a third ANA Group.

Figure 497: Multiple Namespace groups



8.20.3 Asymmetric Namespace Access states

The Asymmetric Namespace Access State indicates information about the characteristics of the relationship between a controller and an ANA Group. The following asymmetric namespace access states are defined:

- ANA Optimized (refer to section 8.20.3.1);
- ANA Non-Optimized (refer to section 8.20.3.2);
- ANA Inaccessible (refer to section 8.20.3.3);
- ANA Persistent Loss (refer to section 8.20.3.4); and
- ANA Change (refer to section 8.20.3.5).

8.20.3.1 ANA Optimized state

While the relationship between the controller and an ANA group is in this state, the characteristic of that relationship to each namespace in that group is optimized. Commands processed by a controller that reports this state for an ANA Group provide optimized access characteristics to any namespace in that ANA Group. A controller that supports ANA Reporting shall support reporting this state.

While in this state, all commands, functions, and operations supported by the namespace shall perform as described in this specification.

8.20.3.2 ANA Non-Optimized state

While the relationship between the controller and an ANA group is in this state, the characteristic of that relationship to each namespace in that group is non-optimized. Commands processed by a controller that reports this state for an ANA Group provide non-optimized access characteristics (e.g., the processing of some commands, especially those involving data transfer, may operate with lower performance or may use NVM subsystem resources less effectively than if a controller is used that reports the optimized state) to any namespace in that ANA Group. Support for reporting this state is optional.

While in this state, all commands, functions, and operations supported by the namespace shall perform as described in this specification.

8.20.3.3 ANA Inaccessible state

While the relationship between the controller and an ANA group is in this state, the characteristic of that relationship to each namespace in that group is inaccessible. Commands processed by a controller that reports this state for an ANA Group are not able to access user data of namespaces in that ANA Group. The namespaces may become accessible through the controller reporting this state at a future time (i.e., a subsequent ANA state transition may occur). Support for reporting this state is optional.

While in this state, accurate namespace related capacity information may not be available. As a result, some namespace capacity information returned in the Identify namespace data (i.e., the NUSE field and the NVMCAP field), are cleared to 0h. For that namespace capacity information, hosts should use the Identify namespace data returned from a controller that reports the relationship between the controller and the namespace to be in the ANA Optimized state or in the ANA Non-Optimized state.

A controller shall fail commands, other than those described in 8.20.4, with a status code of Asymmetric Access Inaccessible if those commands are submitted while the relationship between the namespace specified by the command and the controller processing the command is in this state.

While ANA Inaccessible state is reported by a controller for the namespace, the host should retry the command on a different controller that is reporting ANA Optimized state or ANA Non-Optimized state. If no controllers are reporting ANA Optimized state or ANA Non-Optimized state, then a transition may be occurring such that a controller reporting the Inaccessible state may become accessible and the host should retry the command on the controller reporting Inaccessible state for at least ANATT seconds (refer to Figure 251). Refer to section 8.21.2.

8.20.3.4 ANA Persistent Loss state

While the relationship between the controller and an ANA group is in this state, the characteristic of that relationship to each namespace in that group is persistently inaccessible. Commands processed by a controller that reports this state for an ANA Group are persistently not able to access user data of namespaces in that ANA Group. The relationship between a controller and an ANA Group in this state shall not transition to any other ANA state. Support for reporting this state is optional.

While in this state, accurate namespace related capacity information may not be available. As a result, some namespace capacity information returned in the Identify namespace data (i.e., the NUSE field and the NVMCAP field), are cleared to 0h. For that namespace capacity information, hosts should use the Identify namespace data returned from a controller that reports the relationship between the controller and the namespace to be in the ANA Optimized state or in the ANA Non-Optimized state.

A controller shall fail commands, other than those described in 8.20.4, with a status code of Asymmetric Access Persistent Loss if those commands are submitted while the relationship between the namespace specified by the command and the controller processing the command is in this state.

While ANA Persistent Loss state is reported by a controller for the namespace, the host should retry the command on a different controller that is reporting ANA Optimized state or ANA Non-Optimized state. If no controllers are reporting ANA Optimized state or ANA Non-Optimized state, then a transition may be occurring such that a controller reporting the Inaccessible state may become accessible and the host should retry the command on the controller reporting Inaccessible state for at least ANATT seconds (refer to Figure 251).

8.20.3.5 ANA Change state

The change from one asymmetric namespace access state to another asymmetric namespace access state is called a transition. Transitions may occur in such a way that the ANA Change state is not visible to the host (i.e., the ANA Change state may or may not be reported in the Asymmetric Namespace Access State field in the Asymmetric Namespace Access log (refer to section 5.14.1.12)). Support for reporting this state is optional.

A controller shall fail commands, other than those described in 8.20.4, with a status code of Asymmetric Access Transition if those commands are submitted while the relationship between the namespace specified by the command and the controller processing the command is in this state.

While ANA Change state is reported by a controller for the namespace, the host should:

a) after a short delay, retry the command on the same controller for at least ANATT (refer to Figure 251) seconds (e.g., if ANATT is 30, perform 3 retries at 10 s intervals, or 10 retries at 3 s intervals); or
b) retry the command on a different controller that is reporting ANA Optimized state or ANA Non-Optimized state.

8.20.3.6 Asymmetric Namespace Access Change Notifications

If Asymmetric Namespace Access Change Notices are enabled (refer to section 5.21.1.11) on a controller, then an Asymmetric Namespace Access Change Notice shall be sent as described in Figure 149 by the controllers where the change occurred:

a) if an ANA Group Identifier (refer to Figure 251) changes;
b) if an asymmetric namespace access state transition fails (e.g., a transition begins, but does not complete and the controller returns to the state that existed before the transition began); or
c) upon entry to the following ANA states, unless the state entry is a result of a namespace attachment:

- ANA Optimized State;
- ANA Non-Optimized State;
- ANA Inaccessible State; and
- ANA Persistent Loss State.

8.20.4 Asymmetric Namespace Access States Command Processing Effects

Processing of Admin commands that:

- are not NVM Command Set Specific commands; and
- do not use the Namespace Identifier (i.e., Figure 141 – "Namespace Identifier Used" column indicates "No"),

are not affected by ANA states, except as specified in Figure 498.

Figure 498 describes Asymmetric Namespace Access effects on command processing.

Figure 498: ANA effects on Command Processing

Command	ANA State	Effects on command processing
Get Features	ANA Inaccessible, ANA Persistent Loss, or ANA Change	The following feature identifiers are not available[1]: a) LBA Range Type (i.e., 03h); b) Error Recovery (i.e., 05h); c) Write Atomicity Normal (i.e., 0Ah); d) Reservation Notification Mask (i.e., 82h); and e) Reservation Persistence (i.e., 83h).
Get Log Page	ANA Inaccessible, ANA Persistent Loss, or ANA Change	The following log pages are affected: a) Error Information (i.e., 01h): The log page is not required to contain entries for namespaces whose relationship to the controller processing the command is in the ANA Inaccessible state (refer to section 8.20.3.3), the ANA Persistent Loss state (refer to section 8.20.3.4), or the ANA Change state (refer to section 8.20.3.5).
Identify	ANA Inaccessible or ANA Persistent Loss	Capacity fields in the Identify namespace data structure (refer to Figure 249) information is cleared to 0h.

Figure 498: ANA effects on Command Processing

Command	ANA State	Effects on command processing
Set Features	ANA Inaccessible	The saving of features shall not be supported and the following feature identifiers are not available[1]: a) LBA Range Type (i.e., 03h); b) Error Recovery (i.e., 05h); c) Write Atomicity Normal (i.e., 0Ah); d) Reservation Notification Mask (i.e., 82h); and e) Reservation Persistence (i.e., 83h). If the NSID is set to FFFFFFFFh, then the command shall abort with a status code of Asymmetric Access Inaccessible (refer to section 8.20.3.3).
	ANA Change	The saving of features shall not be supported and the following feature identifiers are not available[1]: a) LBA Range Type (i.e., 03h); b) Error Recovery (i.e., 05h); c) Write Atomicity Normal (i.e., 0Ah); d) Reservation Notification Mask (i.e., 82h); and e) Reservation Persistence (i.e., 83h). If the NSID is set to FFFFFFFFh, then the command shall abort with a status code of Asymmetric Access Transition (refer to section 8.20.3.5).
	ANA Persistent Loss	The command shall abort with a status code of Asymmetric Access Persistent Loss (refer to section 8.20.3.4).

NOTES:
1. If the ANA state is ANA Inaccessible State, then commands that use feature identifiers that are not available shall abort with a status code of Asymmetric Access Inaccessible. If the ANA state is ANA Persistent Loss State, then commands that use feature identifiers that are not available shall abort with a status code of Asymmetric Access Persistent Loss. If the ANA state is ANA Change State, then commands that use feature identifiers that are not available shall abort with a status code of Asymmetric Access Transition.

8.21 Host Operation with Asymmetric Namespace Access Reporting (Informative)

8.21.1 Host ANA Normal Operation

The host determines if ANA is supported by examining bit 3 in the CMIC field in the Identify Controller data structure (refer to Figure 251). The NSID or Identifier (refer to section 7.10) is used to determine when multiple paths to the same namespace are available. The host examines the ANA Log page (refer to section 5.14.1.12) for each controller to determine the ANA state of each group of namespaces attached to that controller.

To send a command to a namespace, the host should select a controller that reports the ANA Optimized State (refer to section 8.20.3.1) and send the command to that controller. If more than one controller that reports the ANA Optimized state for a namespace are found, then the host may use all of those controllers to send commands.

If there are no controllers that report the ANA Optimized state for a namespace, then the host should select a controller that reports ANA Non-Optimized State (refer to section 8.20.3.2) for that namespace and send the command to that controller. If more than one controller that reports ANA Non-Optimized state for a namespace are found, then the host may use all of those controllers to send commands.

If multiple controllers are being used, then the algorithm for determining which controller to use next is outside the scope of this specification (e.g., the host may select a simple round robin algorithm, a queue depth weighted algorithm, a transfer length weighted algorithm, or any other algorithm).

If there are no controllers that report the ANA Optimized state for a namespace and there are no controllers that report the ANA Non-Optimized state for that namespace, then the host should examine controllers that report the ANA Inaccessible state as described in section 8.21.2.

8.21.2 Host ANA Inaccessible Operation

If the ANA Log page reports an ANA state of ANA Inaccessible State for an ANA Group or a command returns a status code of Asymmetric Access Inaccessible, then the host should:

- not use that controller to send commands to any namespace in that ANA Group; and
- select a different controller for sending commands to all namespaces in that ANA Group.

If there are no controllers that report the ANA Optimized state for a namespace and there are no controllers that report the ANA Non-Optimized state, then a transition may be occurring that also impacts controllers that are reporting the ANA Inaccessible state. As a result, the host should use the methods described for Host ANA Transition operation (refer to section 8.21.4) to determine if the controller reporting ANA Inaccessible state transitions during the ANATT time interval to an ANA state that enables commands to be processed by that controller.

8.21.3 Host ANA Persistent Loss Operation

If the ANA Log page reports an ANA state of ANA Persistent Loss State for an ANA Group or a command returns a status code of Asymmetric Access Persistent Loss, then the host should not use that controller to send commands to any namespace in that ANA Group, and select a different controller for sending commands to any namespace in that ANA Group. If the controller supports the Namespace Management capability (refer to section 8.12), then the namespaces in an ANA Group reporting this state should be detached.

8.21.4 Host ANA Transition Operation

If the ANA Log page reports an ANA state of ANA Change State for an ANA Group or a command returns a status code of Asymmetric Access Transition, then the host should temporarily not use that controller to send commands to any namespace in that ANA Group. If only controllers reporting ANA Inaccessible State are available, then the host should follow these procedures to determine which controller to use. To use a controller, the host may:

a) if Asymmetric Namespace Access Change Notices are enabled (refer to section 5.21.1.11) on the controller, wait for an Asymmetric Namespace Access Change Notice from that controller. Upon receipt of that notice, the host should examine the ANA Log page to determine the new ANA state and resume sending commands based on the new ANA state. Such notice should occur within the ANATT time (refer to Figure 251); or
b) delay and retry the command during the ANATT time interval. The host should not immediately retry, but rather, divide the ANATT time into equal intervals for command retry purposes (e.g., if ANATT is 30, perform 3 retries at 10 s intervals, or 10 retries at 3 s intervals). During or upon completion of the ANATT time interval, the new ANA state of the ANA Group should be known (e.g., one of the command retries returned a different status that indicates completion of the transition to a new ANA state). If the retried command did not complete without error, the ANA Log page should be examined on each controller that provides access to the namespace and the host should resume sending commands based on the new ANA state.

If the ANATT time interval expires, then the host should use a different controller for sending commands to the namespaces in that ANA Group. The ANATT interval reported by the controller should prevent this type of timer expiration from occurring.

8.21.5 Host ANA Change Notice Operation

Receipt of an Asymmetric Namespace Access Change Notice from a controller may indicate:

a) that the ANA state reported in one or more ANA Group Descriptors has changed;
b) a new NSID has been added to one or more of the ANA Group Descriptors;
c) an NSID has been removed from one or more of the ANA Group Descriptors; and/or
d) the NSID of a namespace has moved from one ANA Group Descriptor to a different ANA Group Descriptor (i.e., the ANAGRPID field in the Identify Namespace data structure for that namespace has changed), if bit 6 in the ANACAP field is cleared to '0' in the Identify Controller data structure (refer to Figure 251).

As a result of receiving an Asymmetric Namespace Access Change Notice, the host should read the ANA Log page (refer to section 5.14.1.12) to check for each of those possible changes.

8.21.6 All Paths Down Condition

An all paths down condition occurs when there are no paths available on the host to access the namespaces in an ANA Group (i.e., the NVM media). To determine whether an all paths down condition has occurred, the host may examine the ANA Log page on each controller that provides access to the namespaces in a particular ANA Group. All paths that are not in the ANA Persistent Loss state should be checked. If no paths to the namespaces in that ANA Group become available (i.e., transition to the ANA Optimized state or the ANA Non-Optimized state) for the duration of an ANATT time interval, then an all paths down condition has occurred for the namespaces in that ANA Group.

8.22 Get LBA Status (Optional)

Potentially Unrecoverable LBAs are LBAs that, when read, may result in the command that caused the media to be read being aborted with Unrecovered Read Error status. The Get LBA Status capability provides the host with the ability to identify Potentially Unrecoverable LBAs. The logical block data is able to be recovered from another location and re-written.

To support the Get LBA Status capability, the NVM subsystem shall:

- indicate support for the Get LBA Status capability in the Optional Admin Command Support (OACS) field in the Identify Controller data structure;
- indicate support for LBA Status Information Notices in the Optional Asynchronous Events Supported field in the Identify Controller data structure;
- support the LBA Status Information log page;
- indicate support for the Log Page Offset and extended Number of Dwords (i.e., 32 bits rather than 12 bits) in the Log Page Attributes field of the Identify Controller data structure;
- support the LBA Status Attributes Feature;
- support the Get LBA Status command; and
- support the LBA Status Information Alert Notices event.

Prior to using the Get LBA Status capability:

- The host should use the Get Features and Set Features commands with the LBA Status Information Attributes Feature (refer to section 5.21.1.21) to retrieve and optionally configure the LBA Status Information Report Interval; and
- If the host wishes to receive LBA Status Information Alert asynchronous events, the host should enable LBA Status Information Notices (refer to Figure 291).

If LBA Status Information Notices are enabled, the controller shall send an LBA Status Information Alert asynchronous event if:

a) there are Tracked LBAs and:

   a) the LBA Status Information Report Interval condition has been exceeded; or
   b) an implementation specific aggregate threshold, if any exists, of Tracked LBAs has been exceeded;

   or

b) a component (e.g., die or channel) failure has occurred that may result in the controller aborting commands with Unrecovered Read Error status.

Upon receiving an LBA Status Information Alert asynchronous event, the host should send one or more Get Log Page commands for Log Identifier 0Eh with the Retain Asynchronous Event bit set to '1' in order to read the entire LBA Status Information log page (refer to section 5.14.1.14).

Once the host has started reading the LBA Status Information log page with the Retain Asynchronous Event bit set to '1', the controller shall not modify the contents of that log page until the host re-reads the LBA Status Information log page with the Retain Asynchronous Event bit cleared to '0'.

The LBA Status Information log page returns zero or more sets of per-namespace LBA Range Descriptors. Each LBA Range Descriptor specifies a range of LBAs that should be examined by the host in a subsequent Get LBA Status command (refer to section 5.27).

The Get LBA Status command requests information about Potentially Unrecoverable LBAs in a specified range.

The LBA Status Information Report Interval is restarted by the controller when the host issues a Get Log Page for Log Identifier 0Eh with the Retain Asynchronous Event bit cleared to '0'. Reading the Get Log Page for Log Identifier 0Eh with the Retain Asynchronous Event bit cleared to '0' causes an outstanding LBA Status Information asynchronous event to be cleared, if there is one outstanding on the controller.

When the host re-reads the header of the LBA Status Information log page with the Retain Asynchronous Event bit cleared to '0', the host should ensure that the LBA Status Generation Counter matches the original value read. If these values do not match, there is newer LBA Status Log Page data available than that which was returned to the host the last time the host read the LBA Status Information log. In this case, the host is not required to wait for the LBA Status Information Poll Interval (LSIPI) to pass before re-reading the LBA Status Information log page.

The host decides when to send Get LBA Status commands and when to recover the LBAs identified by the Get LBA Status commands, relative to when the host reads the Get Log Page for Log Identifier 0Eh with the Retain Asynchronous Event bit cleared to '0'. Section 8.22.1 describes some example host implementations.

The Get LBA Status command may return zero or more LBA Status Descriptors (refer to Figure 348) for each LBA Range Descriptor (refer to Figure 239) returned by the LBA Status Information log page.

Figure 499: Example LBA Range Identifiers returned by LBA Status Information Log Page

Bytes	Description	Value
03:00	Namespace Element Identifier	1
07:04	Number of LBA Range Descriptors	2
15:08	Reserved	
31:16	**LBA Range Descriptor 0:** This field contains the first LBA Range Descriptor in this LBA Status Log Namespace Element.	**Description** / **Value** Range Starting LBA / 10 Range Number of Logical Blocks / 1,000
47:32	**LBA Range Descriptor 1:** This field contains the second LBA Range Descriptor in this LBA Status Log Namespace Element.	**Description** / **Value** Range Starting LBA / 15,000 Range Number of Logical Blocks / 15,010

Figure 500: Example LBA Status Descriptors for Get LBA Status Command issued for LBA Range Descriptor 0 in Figure 499 (Starting LBA set to 10, Range Length set to 1,000)

Bytes	Description	Value
03:00	Number of LBA Status Descriptors	3
04	Completion Condition	2
07:05	Reserved	
23:08	**LBA Range Descriptor 0:** This field contains the first LBA Range Descriptor in this LBA Status Log Namespace Element.	**Description** / **Value**: Descriptor Starting LBA = 10; Number of Logical Blocks = 30
39:24	**LBA Range Descriptor 1:** This field contains the second LBA Range Descriptor in this LBA Status Log Namespace Element.	**Description** / **Value**: Descriptor Starting LBA = 550; Number of Logical Blocks = 75
55:40	**LBA Range Descriptor 2:** This field contains the third LBA Range Descriptor in this LBA Status Log Namespace Element.	**Description** / **Value**: Descriptor Starting LBA = 1,000; Number of Logical Blocks = 10

Figure 501: Example LBA Status Descriptors for Get LBA Status Command issued for LBA Range Descriptor 1 in Figure 499 (Starting LBA set to 15,000, Range Length set to 15,010)

Bytes	Description	Value
03:00	**Number of LBA Status Descriptors**	1
04	**Completion Condition**	2
07:05	Reserved	
23:08	**LBA Range Descriptor 0:** This field contains the LBA Range Descriptor in this LBA Status Log Namespace Element.	**Description** / **Value**: Descriptor Starting LBA = 15,000; Number of Logical Blocks = 15,010

8.22.1 Sample Get LBA Status Host Software Implementations (Informative)

8.22.1.1 Example Flow #1

1) Read all the LBA Status Information log page data with RAE bit set to ‘1’;
2) Complete all necessary Get LBA Status commands;
3) Complete all necessary recovery of the affected user data by rewriting that data; and
4) Read the LBA Status Information log page data with RAE bit cleared to ‘0’.

8.22.1.2 Example Flow #2

1) Read all the LBA Status Information log page data with RAE bit set to ‘1’;
2) Read the LBA Status Information log page data with RAE bit cleared to ‘0’;
3) Issue some host-determined subset of the Get LBA Status commands indicated by the log page data;
4) Complete the recovery of the affected user data returned by the Get LBA Status commands issued so far;
5) Re-issue the Get LBA Status commands over the ranges associated with the re-written (i.e., recovered) user data;
6) Confirm that the re-written LBAs are no longer in the Tracked LBA List (if any are still there, they are there because they have been detected as newly bad again);
7) Add any new LBA ranges returned in the Get LBA Status commands to the list of LBAs still outstanding the host needs to recover; and
8) If the host has not processed all LBA ranges returned by:
    - the LBA Status Information log page in step 1); and
    - the Get LBA Status command(s) in step 7),

then go back to step 3).

8.23 SQ Associations (Optional)

When Predictable Latency Mode is enabled, all I/O commands for namespaces in a given NVM Set have the same quality of service attributes and shall exhibit predictable latencies as described in section 8.18.

The SQ Associations capability provides hints to the controller as to which specific I/O Queues are associated with a given NVM Set. The controller uses this information to further enhance performance when Predictable Latency Mode is enabled.

The SQ Associations capability is an optional capability. Predictable Latency Mode (refer to section 8.18) is not dependent on the use of the SQ Associations capability.

If a controller supports SQ Associations, then the controller shall:

- indicate support for the SQ Associations capability in the Controller Attributes (CTRATT) field in the Identify Controller data structure;
- indicate support for NVM Sets in the Controller Attributes (CTRATT) field in the Identify Controller data structure; and
- indicate support for Predictable Latency Mode in the Controller Attributes (CTRATT) field in the Identify Controller data structure.

The host enables the SQ Associations capability by creating an association between an NVM Set and a Submission Queue.

In order for the SQ Associations capability to yield benefits, the host is required to:

a) create an association between each Submission Queue and some NVM Set; and
b) only issue I/O commands to Submission Queues that have an association with the NVM Set that contains the namespace associated with the Namespace Identifier specified in that I/O command.

While this capability is enabled, failure to follow the specified operating rules may impact Predictable Latency (refer to section 8.18).

8.24 UUIDs for Vendor Specific Information (Optional)

8.24.1 UUIDs for VS Information Introduction

Several commands send or receive information that contains fields described as Vendor Specific or that is specified by a command field containing a value in a vendor specific range. Examples include the Set Features command, which may specify a vendor specific feature identifier, and the Identify command, which may retrieve a data structure having a vendor specific area.

The vendor specific information may have different definitions (e.g., a vendor specific log page identifier with the contents of the page defined differently by different entities, such as an NVM subsystem vendor and an NVM subsystem customer). By associating each definition of the information with a UUID specified by the defining entity, a command is able to specify the particular definition of the information.

A command specifies a particular definition of the information by specifying an index into a list of UUIDs supported by the controller. The NVMe Invalid UUID is defined for use to replace a previously valid UUID without reorganizing the list of UUIDs, as such reorganizations could change the UUID values specified by indexes into the UUID list.

NVM subsystem vendors and customers communicate (by means outside the scope of this specification) the UUID used for each definition of the information.

8.24.2 UUIDs for VS Information Requirements

A UUID list is a list of non-zero UUID values, terminated by a 0h UUID value. Each non-zero UUID value may be either a valid UUID or the NVMe Invalid UUID. The NVMe Invalid UUID is the hexadecimal value FFFFFFFF_FFFFFFFF_7FFFFFFF_FFFFFFFFh. A valid UUID is any non-zero value other than the NVMe Invalid UUID.

If a command supports selection of a UUID, then the UUID Selection Supported bit in the Commands Supported and Effects data structure for that command (refer to Figure 202) shall be set to '1'. If a command does not support selection of a UUID, then the UUID Selection Supported bit shall be cleared to '0'.

If the UUID Selection Supported bit is set to '1' for one or more commands, then the UUID List bit in the Controller Attributes field shall be set to '1' (refer to Figure 251), and the controller shall support reporting of a UUID List (refer to Figure 261).

If a command supports selection of a UUID, then that command contains a UUID Index field (refer to Figure 502).

Figure 502: UUID Index Field

Bits	Description
6:0	**UUID Index:** If this field is set to a non-zero value, then the value of this field is the index of a UUID in the UUID List (refer to Figure 261) that is used by the command. If this field is cleared to 0h, then no UUID index is specified.

If the UUID Index field specifies a valid UUID (i.e., the UUID Index field is set to a non-zero value and the UUID at that index indicates a valid UUID) (refer to section 5.15.2.13), then the controller shall process the command using the vendor specific information specified by that UUID. If the UUID Index field is cleared to 0h, then the command does not specify a UUID.

If no UUID is specified by the command, then the controller shall process the command, returning vendor specific information.

The controller shall abort the command with Invalid Field in Command status if:

a) The controller does not support the UUID specified by the UUID Index for the specified information;
b) The UUID specified by the UUID Index is cleared to 0h; or
c) The UUID specified by the UUID Index is the NVMe Invalid UUID.

If a firmware image is activated that has a UUID List in which an entry is different from that of the previously-active firmware image, then a host that is unaware of the change may issue a command with the UUID index value for that entry. Such a command may produce unexpected results because the UUID specified by that UUID Index has changed. To avoid this, vendors should follow the following revision guidelines for UUID lists when constructing firmware images that support UUID selection:

a) Add UUIDs that are not supported in prior firmware image revisions to the end of the UUID List in subsequent firmware image revisions;
b) Remove UUIDs that are supported in prior firmware image revisions by replacing the UUID with the NVMe Invalid UUID in the same entry in the UUID list in subsequent firmware image revisions;
c) Do not replace the NVMe Invalid UUID with a valid UUID in the same UUID list entry in subsequent firmware image revisions; and
d) Do not shorten or remove the UUID list in subsequent firmware image revisions.

In these guidelines, the terms "prior" and "subsequent" refer to a linear sequence of firmware versions (e.g., based on the date and time of the construction of the downloadable firmware image).

Following these guidelines prevents the host from inadvertently specifying the wrong UUID because there is at most one valid UUID for each entry in the UUID list. Hence a command that specifies a UUID Index either specifies the intended UUID or is aborted because that entry in the UUID list is empty or contains the NVMe Invalid UUID.

The controller shall require a reset to activate a downloaded firmware image (refer to section 5.11) if the downloaded image reports a UUID list with at least one slot in which a valid UUID replaces the NVMe Invalid UUID or a different valid UUID in the existing image. All controllers that are affected by the UUID list change caused by activation of a downloaded firmware image shall be reset as part of activating that downloaded firmware image.

The above requirements for a reset to activate a downloaded firmware image do not require the controller to directly compare the UUID lists in the current and downloaded firmware images. For example, a vendor could use a vendor-specific major.minor firmware image revision numbering system (e.g., 3.5, 4.1) where all downloadable firmware images with the same major revision number follow the above guidelines. In that scenario, the controller is able to meet these reset requirements by requiring a reset if the downloaded firmware image and the currently executing firmware have different major revision numbers.

8.24.3 UUIDs for VS Information Examples

This section includes examples of the use of UUIDs to select vendor specific information.

8.24.3.1 Vendor Specific Log Page Example

If entity C and entity V create different definitions for a vendor specific log page having the same log page identifier (e.g., D0h), then each assigns a UUID to distinguish their definition (e.g., entity V assigns UUID V and entity C assigns UUID C).

A controller supporting both definitions of the log page:

a) Sets the UUID List bit to ‘1’ in the CTRATT field of the Identify Controller data structure (refer to Figure 251);
b) Sets the UUID Selection Supported bit to ‘1’ in the Commands Supported and Effects data structure (refer to Figure 202) corresponding to the Get Log Page command; and
c) Reports both UUID V and UUID C in the UUID list (refer to Figure 261).

A host requesting the log page defined by entity C:

1) Determines the index of UUID C in the UUID list;
2) Sets the Log Page Identifier field of the Get Log Page command to D0h; and
3) Sets the UUID Index field of the Get Log Page command to the index of UUID C.

A host requesting the log page defined by entity V:

1) Determines the index of UUID V in the UUID list;
2) Sets the Log Page Identifier field of the Get Log Page command to D0h; and
3) Sets the UUID Index field of the Get Log Page command to the index of UUID V.

A host not specifying the definition of the log page clears the UUID Index field to 0h. The selection of the log page definition returned by the controller is vendor specific (e.g., the controller may select any definition for the returned data).

8.24.3.2 Vendor Specific Feature Example

If entity C and entity V create different definitions for a vendor specific feature having the same Feature Identifier (e.g., F1h), then each assigns a UUID to distinguish their definitions (e.g., entity V assigns UUID V and entity C assigns UUID C).

A controller supporting both definitions of the feature for the Get Features command:

a) Sets the UUID List bit to ‘1’ in the CTRATT field of the Identify Controller data structure (refer to Figure 251);

b) Sets the UUID Selection Supported bit to '1' in the Commands Supported and Effects data structure (refer to Figure 202) corresponding to the Get Features command; and
c) Reports both UUID V and UUID C in the UUID list (refer to Figure 261).

A host retrieving the attributes of the feature defined by entity C:

1) Determines the index of UUID C in the UUID list;
2) Sets the Feature Identifier field of the Get Features command to F1h; and
3) Sets the UUID Index field of the Get Features command to the index of UUID C.

A host retrieving the attributes of the feature defined by entity V:

1) Determines the index of UUID V in the UUID list;
2) Sets the Feature Identifier field of the Get Features command to F1h; and
3) Sets the UUID Index field of the Get Features command to the index of UUID V.

8.25 Improving Performance through I/O Size and Alignment Adherence

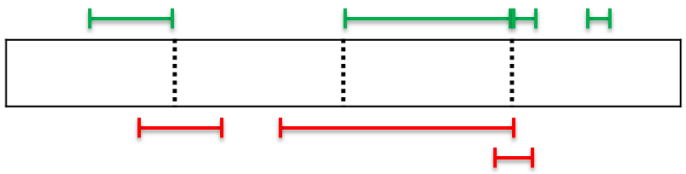
NVMe controllers may require constrained I/O sizes and alignments to achieve the full performance potential. There are a number of optional attributes that the controller uses to indicate these recommendations. If hosts do not follow these constraints, then the controller shall function correctly, but performance may be limited.

Each Write, Write Uncorrectable, or Write Zeroes commands should address a multiple of Namespace Preferred Write Granularity (NPWG) (refer to Figure 249) and Stream Write Size (SWS) (refer to Figure 519) logical blocks (as expressed in the NLB field), and the SLBA field of the command should be aligned to Namespace Preferred Write Alignment (NPWA) (refer to Figure 249) for best performance. Each range in a Dataset Management command with the Attribute - Deallocate (AD) bit set to '1' should contain a multiple of Namespace Preferred Deallocate Granularity (NPDG) (refer to Figure 249) logical blocks and the start of each range should be aligned to Namespace Preferred Deallocate Alignment (NPDA) (refer to Figure 249) and Stream Granularity Size (SGS) logical blocks.

8.25.1 Improved I/O examples (non-normative)

It is recommended that the host utilize the I/O attributes as reported by the controller to receive optimal performance from the NVM subsystem. This section summarizes performance related attributes from namespaces, streams, NVM Sets and the NVM command set. The I/O commands discussed throughout this section include those that interact with non-volatile storage in either a Read, Compare, Verify, Write, Write Uncorrectable, Write Zeroes operation, or Dataset Management operation with the Attribute - Deallocate bit set to '1'. The I/O command properties of length and alignment are discussed throughout this section.

Figure 503: An example namespace with four NOIOBs

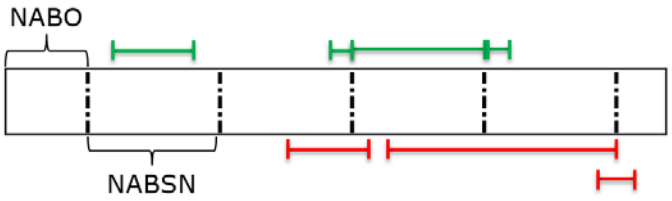


Legend	
☐	Namespace
.....	Namespace Optimal IO Boundary (NOIOB)
⊢⊣	Conformant I/O
⊢⊣	Non-Conformant I/O

In Figure 503 an example namespace is diagrammed with three Namespace I/O Boundaries (NOIOB) (refer to Figure 249). The NOIOB attribute should be applied to Read, Compare, Verify, Write, Write Uncorrectable, and Write Zeroes I/O commands. The four green lines are example I/O commands from the host that adhere to the recommendations of NOIOB settings for this namespace. None of the four I/O

commands shown in green on the top of Figure 503 cross an NOIOB. The three I/O commands shown in red on the bottom of Figure 503 violate the recommendations for improved performance. The longest I/O command shown in red crosses one NOIOB and ends aligned with a different NOIOB. The remaining two I/O commands shown in red also cross an NOIOB. All three of these example I/O commands shown in red could be split into two I/O commands that adhere to the recommendations provided by the namespace for NOIOB.

Figure 504: Example namespace illustrating a potential NABO and NABSN

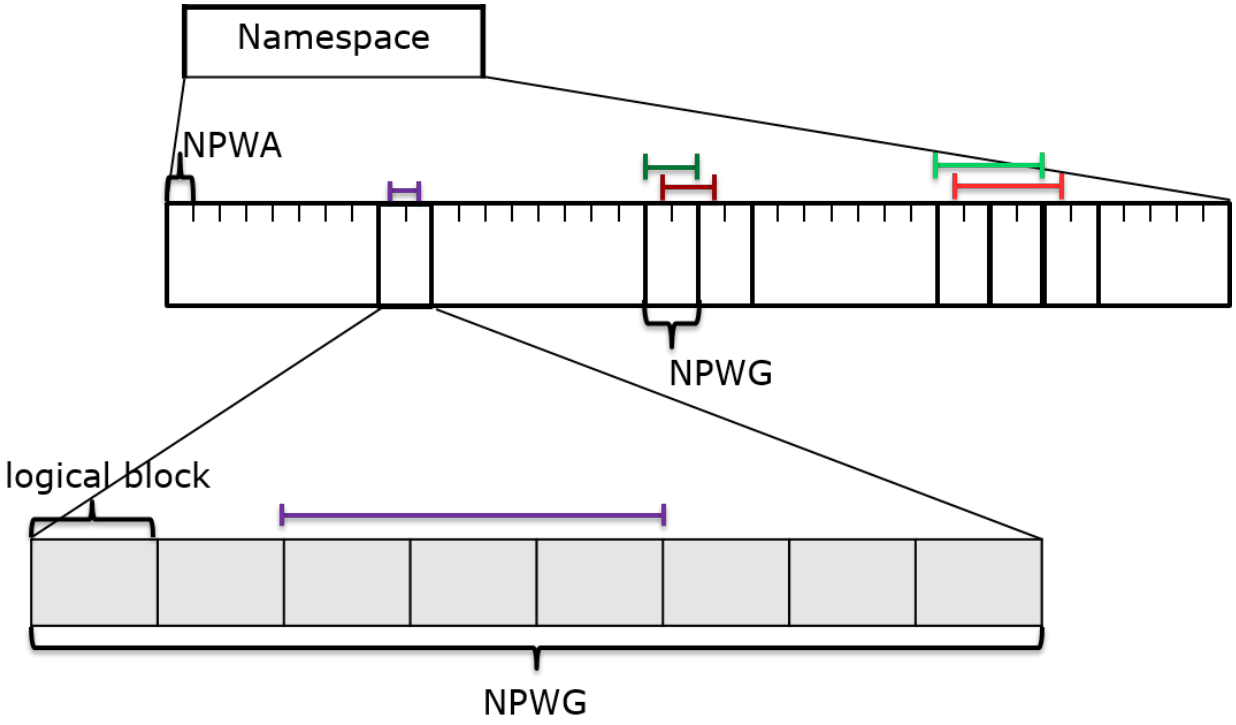


Legend	
	Namespace
	Namespace Atomic Boundary Size Normal (NABSN)
	Conformant I/O
	Non-Conformant I/O
Namespace Atomic Boundary Offset (NABO)	

Continuing with the same namespace example from Figure 503, an illustration of Namespace Atomic Boundary Offset (NABO) (refer to Figure 249) and Namespace Atomic Boundary Size Normal (NABSN) (refer to Figure 249) is shown in Figure 504. NABSN and NABO attributes apply to Write, Write Uncorrectable, and Write Zeroes commands. NABSN and NOIOB may not be related to each other, and there may be an offset of NABO to locate the first NABSN starting. The NOIOBs are not shown in Figure 504. The I/O commands shown in green on the top of Figure 504 illustrate I/O commands that adhere to the namespace's guidance for optimal performance. The I/O commands shown in red on the bottom illustrate I/O commands that do not follow the optimal performance guidelines.

The I/O command examples shown in red in Figure 503 and Figure 504 both illustrate commands that could be restructured to conform to the namespace attributes for Optimal I/O relative to NOIOB, NABO, and NABSN. Each of these example I/O commands shown in red in Figure 503 and Figure 504 could be split into two different I/O commands that adhere to the recommendations. While this increases the number of commands sent to the controller, the expectation is that adherence to the boundary recommendations improves the performance for the controller. Avoiding host traffic that demands non-optimal I/O commands is the most recommendable solution for a host.

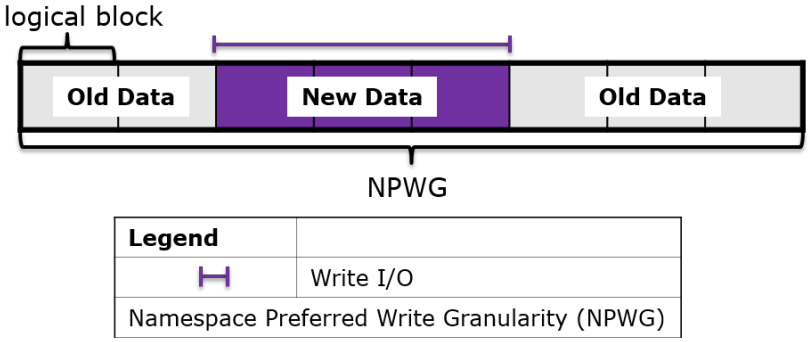
Figure 505: Example namespace broken down to illustrate potential NPWA and NPWG settings



Legend	
	Conformant I/O
	Non-Conformant I/O
Namespace Preferred Write Alignment (NPWA)	
Namespace Preferred Write Granularity (NPWG)	

NPWG and NPWA are namespace internal constructs, and they are illustrated in Figure 505. The box at the top of Figure 505 is the namespace. The series of boxes in the middle layer indicate many namespace optimal write units described by NPWA (refer to Figure 249) and NPWG (refer to Figure 249), and the bottom layer is a series of eight logical blocks that in aggregate form the NPWG for this example. Sometimes NPWG are useful because several sequential logical blocks (refer to Figure 249) may be placed and tracked together on the media, or the NPWG may be related to NVM subsystem data reliability implementation constraints. NPWG and NPWA attributes apply to Write, Write Uncorrectable, and Write Zeroes commands.

Figure 506: Non-conformant Write Impact



Shown in Figure 506 is an I/O command that covers three of eight logical blocks within an NPWG. In this example namespace, NPWG is set to eight logical blocks, and the write of only three logical blocks requires a read of the preceding two logical blocks and trailing three logical blocks. The host write that completes to the non-volatile storage would consist of five logical blocks of older data and three new logical blocks with the data provided by the write I/O command. The resulting read-modify-write may have non-optimal performance in comparison to a host write adhering to the NPWG attribute due to the extra read operation executed internally in the NVM subsystem. Aligning the beginning of the write I/O command with the NPWA attribute would remove the requirement to read the preceding existing data. Host writes with a length that is a multiple of NPWG would remove the requirement for reading the trailing data.

Following the NPWG recommendation alone is insufficient for optimal performance. If a write I/O command specifies the number of LBAs that is an integer multiple of NPWG and is offset in alignment from the recommended NPWA, then a read-modify-write may occur on the logical blocks at the beginning and ending of the command. The I/O commands shown in red in Figure 505 specify numbers of LBAs that are integer multiples of NPWG, but their alignment is triggering a read-modify-write at both the beginning and ending of the write I/O command. The write I/O commands shown in green adhere to the alignment and granularity requirements of the NPWA and NPWG. Figure 507 illustrates the shorter dark green write I/O command that adheres to both NPWG and NPWA attributes. This dark green write I/O command has a length equaling the NPWG attribute which adheres to the NPWG attribute recommendations. Figure 508 illustrates the dark red write I/O command that follows the NPWG attribute with a length of one NPWG, but that command does not adhere to the NPWA attribute recommendations. The dark red write I/O command requires a read of the old data at the beginning and the ending of the write I/O command to fill both NPWG units illustrated here. Longer write I/O commands that fail to adhere to the NPWA recommendation may trigger a read-modify-write of the leading and trailing NPWG segments inside of the NVM subsystem.

Figure 507: Host write I/O command following NPWA and NPWG

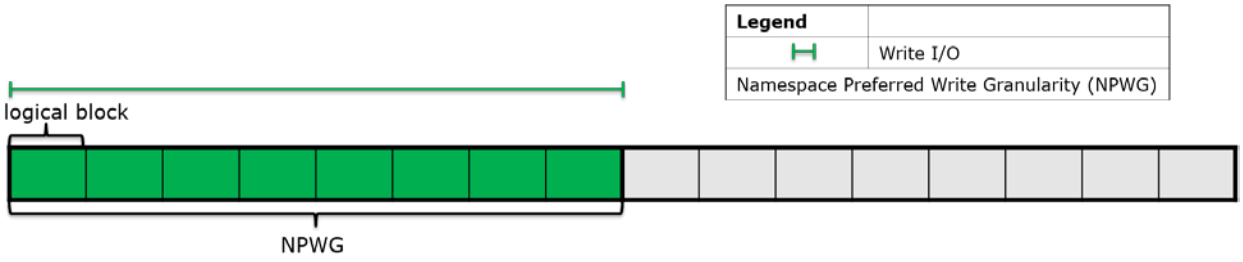
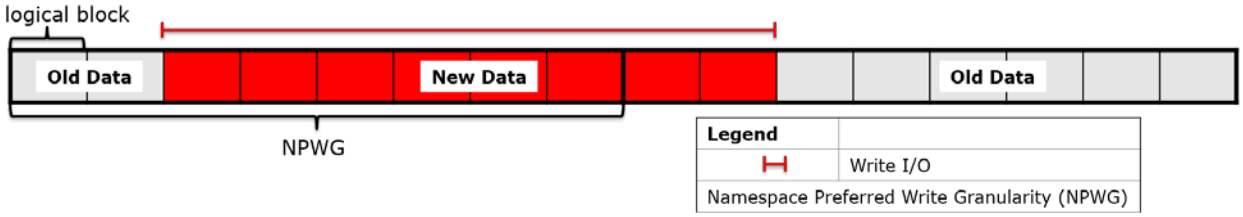
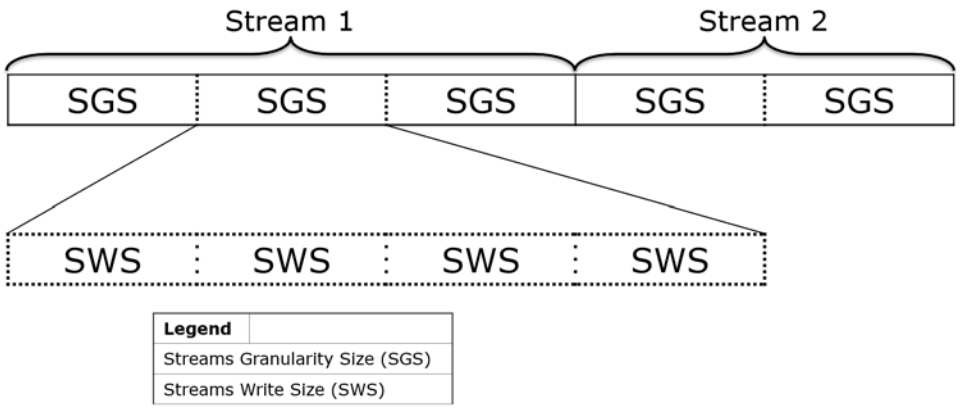


Figure 508: Host write I/O command following NPWG but not NPWA attributes



NPDG and NPDA (refer to Figure 249) are constructs in the namespace intended to improve performance for Dataset Management deallocate operations within a namespace. NPDG and NPDA may be impacted by multiple factors including but not limited to the boundaries described in Figure 505, device hardware limits, or non-volatile storage erase block sizes. Deallocating at multiples of NPDG size and aligned to NPDA ((Starting LBA modulo NPDA) == 0) may enable improved deallocate performance for the namespace.

Figure 509: Two streams composed of SGS and SWS



Streams (refer to section 9.3) may or may not be utilized with different namespace attributes. Figure 509 shows the streams attributes of Stream Granularity Size (SGS) (refer to Figure 519) and Stream Write Size (SWS) (refer to Figure 519). The first stream is constructed by the host to be composed of three SGS units, and each SGS unit in this example is equal to four SWS units. The host streams are optimized for performance of the Dataset Management deallocate operations by extending the stream in units of SGS. The streams receive optimal host write performance if write I/O command lengths are integer multiples of SWS.

Streams are sometimes handled by separate I/O paths in the device. This may entail such things as different device hardware, media mapping, or reliability protections. SWS should be a multiple of the NPWG. SGS and NPDG may be equivalent to or multiples of each other. A namespace utilizing integer multiple relationships between the streams attributes (SWS and SGS) and the namespace attributes (NPWG and NPDG) may provide optimal performance by adhering to the largest attribute for write I/O commands or deallocations.

Not all namespaces describe both their Streams and namespace attributes in multiples as described above. The recommended order of priority for a host to adhere to conflicting namespace and Streams attributes is to conform to SGS and SWS while utilizing the Streams directives. When not utilizing the Streams directives, the namespace attributes for each namespace should provide improved performance.

If the Streams Directive is enabled on a namespace, and a deallocate operations specifies logical blocks that are associated with a stream, then the host should use the SGS based alignment and size preferences in favor of the Namespace and NVM Set preferences. If the Streams Directive is not enabled on a

namespace, or the logical blocks are not associated with a stream, then the host should construct deallocate operations that conform to NPDG and NPDA.

Namespace Optimal Write Size (NOWS) (refer to Figure 249) is intended to supplement NVM Sets Optimal Write Size as NOWS provides a mechanism to report the optimal write size that scales to a multiple namespace per NVM Set use case, but also covers the use case where there is a single namespace allocated in an NVM Set. Namespaces should report NOWS as a multiple of NPWG. When constructing write operations, the host should minimally construct writes that meet the recommendations of NPWG and NPWA, but may achieve optimal write performance by constructing writes that meet the recommendation of NOWS.

If NVM Sets are supported as described in Figure 251, the value in the NOWS field for the namespace indicates the value the host should use to achieve optimal performance. If an NVM Set does not specify an Optimal Write Size, the host should use the value in the NOWS field for the namespace for I/O optimization purposes. Similarly, if NOWS is not defined for a namespace, the host should use the value in the Optimal Write Size field for the NVM Set associated with that namespace to achieve optimal performance.

9 Directives

Directives is a mechanism to enable host and NVM subsystem or controller information exchange. The Directive Receive command is used to transfer data related to a specific Directive Type from the controller to the host. The Directive Send command is used to transfer data related to a specific Directive Type from the host to the controller. Other commands may include a Directive Specific value specific for a given Directive Type (e.g., the Write command in the NVM command set).

Support for Directives is optional and is indicated in the Optional Admin Command Support (OACS) field in the Identify Controller data structure.

If a controller supports Directives, then the controller shall:

- Indicate support for Directives in the Optional Admin Command Support (OACS) field in the Identify Controller data structure;
- Support the Directive Receive command;
- Support the Directive Send command; and
- Support the Identify Directive (i.e., Type 00h).

The Directive Types that may be supported by a controller (refer to Figure 510) are the Identify Directive (refer to section 9.2), and the Streams Directive (refer to section 9.3). The Directive Specific field and Directive Operation field are dependent on the Directive Type specified in the command (e.g., Directive Send, Directive Receive, or I/O command).

Figure 510: Directive Types

Directive	Directive Type Value	Definition	I/O Command Directive
Identify	00h	Section 9.2	No
Streams	01h	Section 9.3	Yes

If a Directive is not supported or is supported and disabled, then all Directive Send commands and Directive Receive commands with that Directive Type shall be aborted with a status of Invalid Field in Command.

Support for a specific directive type is indicated using the Return Parameters operation of the Identify Directive. A specific directive may be enabled or disabled using the Enable operation of the Identify Directive. Before using a specific directive, the host should determine if that directive is supported and should enable that directive using the Identify Directive.

9.1 Directive Use in I/O Commands

I/O Command Directives are the subset of Directive Types that may be used as part of I/O commands. For example, a Write command in the NVM command set may specify a Directive Type and an associated Directive Specific value. I/O Command Directives shall have a Directive Type value that is less than or equal to 0Fh due to the size of the Directive Type field in I/O commands. When a Directive Type is specified in an I/O command, the upper four bits are assumed to be 0h. A Directive Type of 00h in an I/O command specifies that the I/O command is not using Directives.

The only I/O command that supports use of directives in this version of this specification is the Write command.

In an I/O command, if the Directive Type (DTYPE) field is set to an I/O Command Directive, then the Directive Specific (DSPEC) field includes additional information for the associated I/O command (refer to Figure 511).

Figure 511: Directive Specific Field Interpretation

Directive Type Value	Directive Specific Field Definition
00h (Directives not in use)	Field not used.
01h (Streams)	Specifies the identifier of the stream associated with the data.

Figure 511: Directive Specific Field Interpretation

Directive Type Value	Directive Specific Field Definition
02h to 0Fh	Reserved

In an I/O command:

- if no I/O Command Directive is enabled or the DTYPE field is cleared to 00h, then the DTYPE field and the DSPEC field are ignored; and
- if one or more I/O Command Directives is enabled and the DTYPE field is set to a value that is not supported or not enabled, then the controller shall abort the command with a status of Invalid Field in Command**.**

For the Streams Directive (i.e., DTYPE field set to 01h), if the DSPEC field is cleared to 0h in a Write command, then that Write command shall be processed as a normal write operation (i.e., as if DTYPE field is cleared to 00h).

9.2 Identify (Directive Type 00h)

The Identify Directive is used to determine the Directive Types that the controller supports and to enable use of the supported Directives. If Directives are supported, then this Directive Type shall be supported.

The Directive operations that shall be supported for the Identify Directive are listed in Figure 512.

Figure 512: Identify Directive – Directive Operations

Directive Command	Directive Operation Name	Directive Operation Value	Definition
Directive Receive	Return Parameters	01h	Section 9.2.1.1
	Reserved	All others	
Directive Send	Enable Directive	01h	Section 9.2.2.1
	Reserved	All others	

9.2.1 Directive Receive

This section defines operations used with the Directive Receive command for the Identify Directive.

9.2.1.1 Return Parameters (Directive Operation 01h)

This operation returns a data structure that contains a bit vector specifying the Directive Types supported by the controller and a bit vector specifying the Directive Types enabled for the namespace. The data structure returned is defined in Figure 513. If an NSID value of FFFFFFFFh is specified, then the controller shall abort the command with a status of Invalid Field in Command. The DSPEC field in command Dword 11 is not used for this operation.

Figure 513: Identify Directive – Return Parameters Data Structure

Bytes	Bits	Description
		Directives Supported
31:00	255:02	Reserved
	01	**Streams Directive:** This bit is set to '1' if the Streams Directive is supported. This bit is cleared to '0' if the Streams Directive is not supported.
	00	**Identify Directive:** This bit shall be set to '1' to indicate that the Identify Directive is supported.
		Directives Enabled
63:32	255:02	Reserved
	01	**Streams Directive:** This bit is set to '1' if the Streams Directive is enabled. This bit is cleared to '0' if the Streams Directive is not enabled.
	00	**Identify Directive:** This bit shall be set to '1' to indicate that the Identify Directive is enabled.
4095:64	n/a	Reserved

9.2.2 Directive Send

This section defines operations used with the Directive Send command for the Identify Directive.

9.2.2.1 Enable Directive (Directive Operation 01h)

The Enable Directive operation is used to enable a specific Directive for use within a namespace by all controllers that are associated with the same Host Identifier. The DSPEC field in command Dword 11 is not used for this operation. The Identify Directive is always enabled. The enable state of each Directive on each shared namespace attached to enabled controllers associated with the same non-zero Host Identifier is the same. If an NSID value of FFFFFFFFh is specified, then the Enable Directive operation applies to the NVM subsystem (i.e., all namespaces and all controllers associated with the NVM subsystem). On an NVM Subsystem Reset, all Directives other than the Identify Directive are disabled for the entire NVM subsystem.

On a Controller Level Reset:

- all Directives other than the Identify Directive are disabled for that controller; and
- if there is an enabled controller associated with the Host Identifier for the controller that was reset, then for namespaces attached to enabled controllers associated with that Host Identifier, Directives are not disabled.

If a host sets the Host Identifier of a controller to the same non-zero Host Identifier as one or more other controllers in the NVM subsystem, then setting that Host Identifier shall result in each shared namespace attached to that controller having the same enable state for each Directive as the enable state for each Directive for that namespace attached to other controllers associated with that Host Identifier.

If a host enables a controller that has the same non-zero Host Identifier as one or more other controllers in the NVM subsystem, then enabling that controller shall result in each shared namespace attached to that controller having the same enable state for each Directive as the enable state for each Directive for that namespace attached to other controllers associated with that Host Identifier.

For all controllers in an NVM subsystem that have the same non-zero Host Identifier, if a host changes the enable state of any Directive for a shared namespace attached to a controller by a means other than a Controller Level Reset, then that change shall be made to the enable state of that Directive for that namespace attached to any other controller associated with that Host Identifier.

Figure 514: Enable Directive – Command Dword 12

Bits	Description
31:16	Reserved
15:08	**Directive Type (DTYPE):** This field specifies the Directive Type to enable or disable. If this field specifies the Identify Directive (i.e., 00h), then a status of Invalid Field in Command shall be returned.
07:01	Reserved
00	**Enable Directive (ENDIR):** If set to '1' and the Directive Type is supported, then the Directive is enabled. If cleared to '0', then the Directive is disabled. If this bit is set to '1' for a Directive that is not supported, then a status of Invalid Field in Command shall be returned.

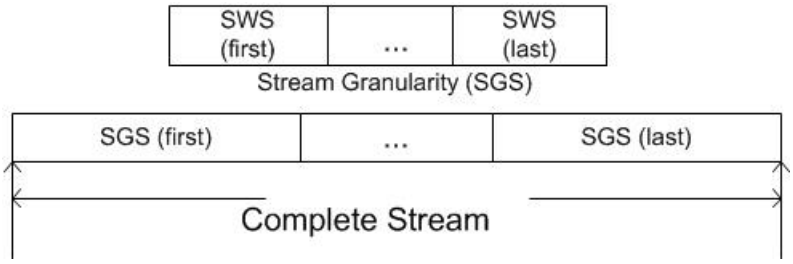
9.3 Streams (Directive Type 01h, Optional)

The Streams Directive enables the host to indicate (i.e., by using the stream identifier) to the controller that the specified logical blocks in a write command are part of one group of associated data. This information may be used by the controller to store related data in associated locations or for other performance enhancements.

The controller provides information in response to the Return Parameters operation about the configuration of the controller that indicates Stream Write Size, Stream Granularity Size, and stream resources at the NVM subsystem and namespace levels.

Data that is aligned to and in multiples of the Stream Write Size (SWS) provides optimal performance of the write commands to the controller. The Stream Granularity Size indicates the size of the media that is prepared as a unit for future allocation for write commands and is a multiple of the Stream Write Size. The controller may allocate and group together a stream in Stream Granularity Size (SGS) units. Refer to Figure 515.

Figure 515: Directive Streams – Stream Alignment and Granularity



If the host issues a Dataset Management command to deallocate logical blocks that are associated with a stream, that host should specify a starting LBA and length that is aligned to and in multiples of the Stream Granularity Size. This provides optimal performance and endurance of the media.

Stream resources are the resources in the NVM subsystem that are necessary to track operations associated with a specified stream identifier. There are a maximum number of stream resources that are available in an NVM subsystem as indicated by the Max Stream Limit (MSL) field in the Return Parameters data structure.

Available NVM subsystem stream resources are stream resources that are not allocated for exclusive use in any namespace. Available NVM subsystem stream resources are reported in the NVM Subsystem Streams Available (NSSA) field and may be used by any host in any namespace that:

- has the Streams Directive enabled;
- has not been allocated exclusive stream resources by that host if bit 0 of the NSSC field is cleared to '0'; and

- has not been allocated exclusive stream resources by any host if bit 0 of the NSSC field is set to '1'.

Each time stream resources are allocated for exclusive use in a specified namespace, the available NVM subsystem stream resources reported in the NSSA field are reduced.

For a given namespace:

a) a host allocates stream resources to that namespace for the exclusive use of that host(s) by issuing the Allocate Resources operation;
b) other hosts may concurrently allocate stream resources to that namespace for their exclusive use; and
c) hosts which have not allocated stream resources to that namespace may use available NVM subsystem stream resources for access to that namespace.

The Directive operations that shall be supported if the Streams Directive is supported are listed in Figure 516. The Directive Specific field in a command is referred to as the stream identifier when the Directive Type field is set to the Streams Directive.

Figure 516: Streams – Directive Operations

Directive Command	Directive Operation Name	Directive Operation Value	Definition
Directive Receive	Return Parameters	01h	Section 9.3.1.1
	Get Status	02h	Section 9.3.1.2
	Allocate Resources	03h	Section 9.3.1.3
	Reserved	All others	
Directive Send	Release Identifier	01h	Section 9.3.2.1
	Release Resources	02h	Section 9.3.2.2
	Reserved	All others	

Stream identifiers are assigned by the host and may be in the range 0001h to FFFFh. The host may specify a sparse set of stream identifiers (i.e., there is no requirement for the host to use Stream Identifiers in any particular order).

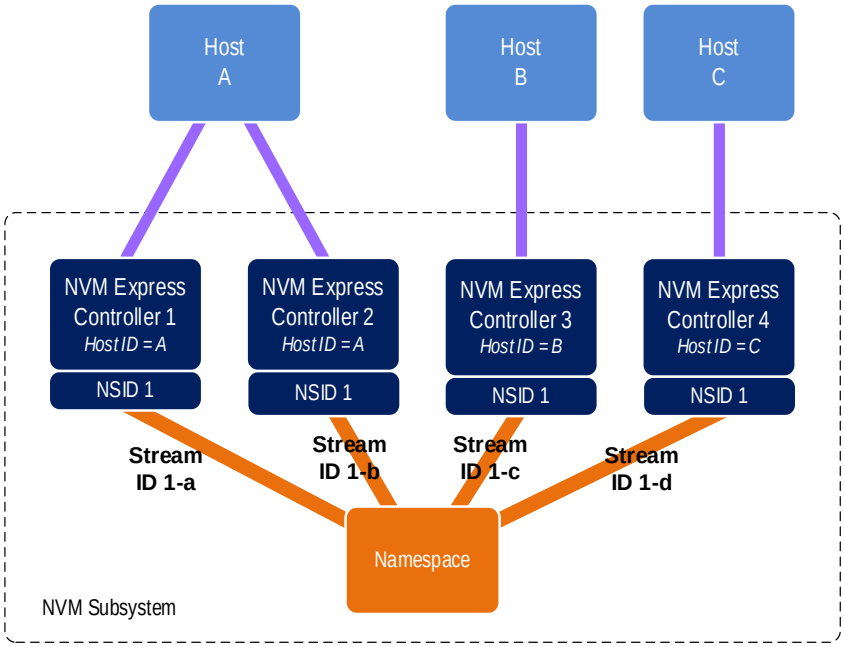
The host may access a namespace through multiple controllers in the NVM subsystem. The controllers in an NVM subsystem indicate in bit 0 of the NSSC field (refer to Figure 519) if a stream identifier is unique based on the Host Identifier (i.e., the same stream identifier used to access the same namespace by a host that has registered a different Host Identifier is referencing a different stream), or if a stream identifier may be used by multiple Host Identifiers (i.e., the same stream identifier used to access the same namespace by a host that has registered a different Host Identifier is referencing the same stream). All controllers in an NVM subsystem shall report the same value in the NSSC field.

If multiple controllers receive a registration of a Host Identifier (refer to section 5.21.1.19) that has the same non-zero value, then that value represents a single host that is accessing the namespace through those controllers and a stream identifier is used across those controllers to access the same stream on the namespace. If a Host Identifier has a unique non-zero value, then each value represents a unique host that is accessing the namespace and:

- if bit 0 of the NSSC field is cleared to '0', then the same stream identifier on controllers with different non-zero Host Identifiers does not have the same meaning for a particular namespace (i.e., the stream identifier is not used across controllers with different non-zero Host Identifiers to access the same stream on the namespace); and
- if bit 0 of the NSSC field is set to '1', then the same stream identifier on any controller with a non-zero Host Identifier has the same meaning for a particular namespace (i.e., the stream identifier is used across controllers to access the same stream on the namespace).

If a Host Identifier is cleared to 0h, then a unique host is accessing the namespace and the stream identifier does not have the same meaning for a particular namespace.

Figure 517: Example Multi-Stream and NSSC



In the example shown in Figure 517, if NSSC bit 0 is cleared to '0', then there are three streams as follows:

- Stream ID 1-a and Stream ID 1-b have the same meaning;
- Stream ID 1-c has a different meaning; and
- Stream ID 1-d has a different meaning.

In the example shown in Figure 517, if NSSC bit 0 is set to '1', then there is one stream as follows:

- Stream ID 1-a, Stream ID 1-b, Stream ID 1-c, and Stream ID 1-d have the same meaning.

The controller(s) recognized by the NVM subsystem as being associated with a specific host or hosts and attached to a specific namespace either:

- utilizes a number of stream resources allocated for exclusive use of that namespace as returned in response to an Allocate Resources operation; or
- utilizes resources from the NVM subsystem stream resources.

The value of Namespace Streams Allocated (NSA) indicates how many resources for individual stream identifiers have been allocated for exclusive use for the specified namespace by the associated controllers. This indicates the maximum number of stream identifiers that may be open at any given time in the specified namespace by the associated controllers. To request a different number of resources than are currently allocated for exclusive use by the associated controllers for a specific namespace, all currently allocated resources are first required to be released using the Release Resources operation. There is no mechanism to incrementally increase or decrease the number of allocated resources for a given namespace.

Streams are opened by the controller when the host issues a Write command that specifies a stream identifier that is not currently open. While a stream is open the controller maintains context for that stream (e.g., buffers for associated data). The host may determine the streams that are open using the Get Status operation.

For a namespace that has a non-zero value of Namespace Streams Allocated (NSA), if the host submits a Write command specifying a stream identifier not currently in use and stream resources are exhausted, then an arbitrary stream identifier for that namespace is released by the controller to free the stream

resources associated with that stream identifier for the new stream. The host may ensure the number of open streams does not exceed the allocated stream resources for the namespace by explicitly releasing stream identifiers as necessary using the Release Identifier operation.

For a namespace that has zero namespace stream resources allocated, if the host submits a Write command specifying a stream identifier not currently in use and:

- NVM subsystem streams available are exhausted, then an arbitrary stream identifier for an arbitrary namespace that is using NVM subsystem stream resources is released by the NVM subsystem to free the stream resources associated with that stream identifier for the new stream; or
- all NVM subsystem stream resources have been allocated for exclusive use for specific namespaces, then the Write command is treated as a normal Write command that does not specify a stream identifier.

The host determines parameters associated with stream resources using the Return Parameters operation. The host may get a list of open stream identifiers using the Get Status operation.

If the Streams Directive becomes disabled for use by a host within a namespace, then all stream resources and stream identifiers shall be released for that host for the affected namespace. If the host issues a Format NVM command, then all stream identifiers for all open streams for affected namespaces shall be released. If the host deletes a namespace, then all stream resources and all stream identifiers for that namespace shall be released. If the write protection state of a namespace changes such that the namespace becomes write protected (refer to section 8.19), then the controller shall release all stream resources and stream identifiers for that namespace.

Streams Directive defines the command specific status values specified in Figure 518.

Figure 518: Streams Directive – Command Specific Status Values

Value	Description
7Fh	**Stream Resource Allocation Failed:** The controller was not able to allocate stream resources for exclusive use of the specified namespace and no NVM subsystem stream resources are available.

9.3.1 Directive Receive

This section defines operations used with the Directive Receive command for the Streams Directive.

9.3.1.1 Return Parameters (Directive Operation 01h)

The Return Parameter operation returns a data structure that specifies the features and capabilities supported by the Streams Directive, including namespace specific values. The DSPEC field in command Dword 11 is not used for this operation. The data structure returned is defined in Figure 519. If an NSID value of FFFFFFFFh is specified, then the controller returns the NVM subsystem specific values, may return any namespace specific values that are the same for all namespaces (e.g., SWS), and clears all other namespace specific fields to 0h.

Figure 519: Streams Directive – Return Parameters Data Structure

Bytes	Description
	NVM Subsystem Specific Fields
01:00	**Max Streams Limit (MSL):** This field indicates the maximum number of concurrently open streams that the NVM subsystem supports. This field returns the same value independent of specified namespace.
03:02	**NVM Subsystem Streams Available (NSSA):** This field indicates the number of NVM subsystem stream resources available. These are the stream resources that are not allocated for the exclusive use by a host in any specific namespace. This field returns the same value independent of specified namespace.

Figure 519: Streams Directive – Return Parameters Data Structure

Bytes	Description
05:04	**NVM Subsystem Streams Open (NSSO):** This field indicates the number of open streams in the NVM subsystem that are not associated with a namespace for which resources were allocated using an Allocate Resources operation. This field returns the same value independent of specified namespace.
06	**NVM Subsystem Stream Capability (NSSC):** This field indicates the stream capabilities of the NVM subsystem. Bits 7:1 are reserved. Bit 0 indicates whether stream identifiers may be shared by multiple Host Identifiers, or if a stream identifier is associated with a single Host Identifier. Bit 0 if cleared to '0', then the stream identifier is associated with a single non-zero Host Identifier. Bit 0 if set to '1', then the stream identifier may be associated with multiple non-zero Host Identifiers.
15:07	Reserved
Namespace Specific Fields	
19:16	**Stream Write Size (SWS):** This field indicates the alignment and size of the optimal stream write as a number of logical blocks for the specified namespace. The size indicated should be less than or equal to Maximum Data Transfer Size **(**MDTS) that is specified in units of minimum memory page size. SWS may change if the namespace is reformatted with a different LBA format. If the NSID value is set to FFFFFFFFh, then this field may be cleared to 0h if a single logical block size cannot be indicated. Refer to section 8.25 for how this field is utilized to optimize performance and endurance.
21:20	**Stream Granularity Size (SGS):** This field indicates the stream granularity size for the specified namespace in Stream Write Size (SWS) units. If the NSID value is set to FFFFFFFFh, then this field may be cleared to 0h. Refer to section 8.25 for how this field is utilized to optimize performance and endurance.
Namespace and Host Identifier Specific Fields	
23:22	**Namespace Streams Allocated (NSA):** This field indicates the number of stream resources allocated for exclusive use of the specified namespace. If bit 0 of the NSSC field is cleared to '0', then those exclusive stream resources are shared by the controller processing the Return Parameters operation and by all other controllers that share the same non-zero Host Identifier, and are attached to the specified namespace. If bit 0 of the NSSC field is set to '1', then those exclusive stream resources are shared by all controllers that are associated with any non-zero Host Identifier and are attached to this namespace. If this value is non-zero, then the namespace may have up to NSA number of concurrently open streams. If this field is cleared to 0h, then no stream resources are currently allocated to this namespace and the namespace may have up to NSSA number of concurrently open streams.
25:24	**Namespace Streams Open (NSO):** This field indicates the number of open streams in the specified namespace. If bit 0 of the NSSC field is cleared to '0', then this field indicates the number of streams that were opened by the controller processing the Return Parameters operation and by all other controllers that share the same non-zero Host Identifier, and are attached to this namespace. If bit 0 of the NSSC field is set to '1', then this field indicates the number of streams that were opened by the controller processing the Return Parameters operation and all other controllers that are associated with any non-zero Host Identifier and are attached to this namespace. NOTE: It is not possible for a host to retrieve the number of open streams using resources allocated to the specified namespace by other hosts.
31:26	Reserved

9.3.1.2 Get Status (Directive Operation 02h)

The Get Status operation returns information about the status of currently open streams for the specified namespace and the host issuing the Get Status operation. The DSPEC field in command Dword 11 is not used for this operation.

If NSSC bit 0 is cleared to '0', then the information returned describes only those resources for the specified namespace that are associated with hosts that are registered with the same non-zero Host Identifier value as the host issuing the Get Status operation. If NSSC bit 0 is set to '1', then the information returned describes the resources for the specified namespace that are associated with hosts that are registered with any non-zero Host Identifier.

If an NSID value of FFFFFFFFh is specified, then the controller shall return information about the status of currently open streams in the NVM subsystem that use resources which are not allocated for the exclusive use of a particular namespace. If a stream identifier value being returned is in use by different namespaces, then that stream identifier shall be returned only once.

Stream Identifier 1 (i.e., returned at offset 03:02) contains the value of the open stream of lowest numerical value. Each subsequent field contains the value of the next numerically greater stream identifier of an open stream.

The data structure returned is defined in Figure 520. All fields are specific to the namespace specified if the NSID value was not set to FFFFFFFFh.

Figure 520: Streams Directive – Get Status Data Structure

Bytes	Description
01:00	**Open Stream Count:** This field specifies the number of streams that are currently open.
03:02	**Stream Identifier 1:** This field specifies the stream identifier of the first (numerically lowest) open stream.
05:04	**Stream Identifier 2:** This field specifies the stream identifier of the second open stream.
…	…
131071: 131070	**Stream Identifier 65,535:** This field specifies the stream identifier of the 65,535th open stream.

9.3.1.3 Allocate Resources (Directive Operation 03h)

The Allocate Resources operation indicates the number of streams that the host requests for the exclusive use for the specified namespace. If bit 0 of the NSSC field is cleared to '0', then those resources are for the exclusive use of hosts that are registered with the same Host Identifier as the host that made the request. If bit 0 of the NSSC field is set to '1', then those resources are for the exclusive use of any host that is registered with any non-zero Host ID. The DSPEC field in command Dword 11 is not used for this operation. The operation returns the number of streams allocated in Dword 0 of the completion queue entry. The value allocated may be less than or equal to the number requested. The allocated resources shall be reflected in the Namespace Streams Allocated field of the Return Parameters data structure.

If the controller is unable to allocate any stream resources for the exclusive use for the specified namespace, then the controller shall:

- return a status value of Stream Resource Allocation Failed; or
- if NVM subsystem stream resources are available, then clear NSA to 0h in the completion queue entry to indicate that the host may use stream resources from the NVM subsystem for this namespace.

If the specified namespace already has stream resources allocated for the exclusive use of the host issuing the Allocate Resources operation, then the controller shall return a status value of Invalid Field in Command. To allocate additional streams resources, the host should release resources and request a complete set of resources.

No data transfer occurs.

Figure 521: Allocate Resources – Command Dword 12

Bits	Description
31:16	Reserved
15:00	**Namespace Streams Requested (NSR):** This field specifies the number of stream resources the host is requesting be allocated for exclusive use by the namespace specified.

Figure 522: Allocate Resources – Completion Queue Entry Dword 0

Bits	Description
31:16	Reserved
15:00	**Namespace Streams Allocated (NSA):** This field indicates the number of streams resources that have been allocated for exclusive use by the namespace specified. The allocated resources are available to all controllers associated with that host.

9.3.2 Directive Send

This section defines operations used with the Directive Send command for the Streams Directive.

9.3.2.1 Release Identifier (Directive Operation 01h)

The Release Identifier operation specifies that the stream identifier specified in the DSPEC field in command Dword 11 is no longer in use by the host. Specifically, if the host uses that stream identifier in a future operation, then that stream identifier is referring to a different stream. If the specified identifier does not correspond to an open stream for the specified namespace, then the command completes successfully. If there are stream resources allocated for the exclusive use of the specified namespace, then those exclusive stream resources remain allocated for this namespace, and may be re-used in a subsequent write command. If there are no stream resources allocated for the exclusive use of the specified namespace, then the stream resources are returned to the NVM subsystem stream resources for future use by a namespace without exclusive allocated stream resources. If an NSID value of FFFFFFFFh is specified, then the controller shall abort the command with a status of Invalid Field in Command.

No data transfer occurs.

9.3.2.2 Release Resources (Directive Operation 02h)

The Release Resources operation is used to release all streams resources allocated for the exclusive use of the namespace attached to all controllers:

- associated with the same non-zero Host Identifier of the controller that processed the operation if bit 0 of the NSSC field is cleared to ‘0’; and
- associated with any non-zero Host Identifier if bit 0 of the NSSC field is set to ‘1’.

On successful completion of this command, the exclusive allocated stream resources are released and the Namespace Streams Allocated (refer to Figure 519) field is cleared to 0h for the specified namespace. If this command is issued when no streams resources are allocated for the exclusive use of the namespace, the command shall complete successfully.

No data transfer occurs.

10 Error Reporting and Recovery

10.1 Command and Queue Error Handling

In the case of serious error conditions, like Completion Queue Invalid, the operation of the associated Submission Queue or Completion Queue may be compromised. In this case, host software should delete the associated Completion Queue and/or Submission Queue. The delete of a Submission Queue aborts all outstanding commands, and deletion of either queue type releases resources associated with that queue. Host software should recreate the Completion Queue and/or Submission Queue to then continue with operation.

In the case of serious error conditions for Admin commands, the entire controller should be reset using a Controller Level Reset. The entire controller should also be reset if a completion is not received for the deletion of a Submission Queue or Completion Queue.

For most command errors, there is not an issue with the Submission Queue and/or Completion Queue itself. Thus, host software and the controller should continue to process commands. It is at the discretion of host software whether to retry the failed command; the Retry bit in the Completion Queue Entry indicates whether a retry of the failed command may succeed.

10.2 Media and Data Error Handling

In the event that the requested operation could not be performed to the NVM media, the particular command is completed with a media error indicating the type of failure using the appropriate status code.

If a read error occurs during the processing of a command, (e.g., End-to-end Guard Check Error, Unrecovered Read Error), the controller may either stop the DMA transfer into the memory or transfer the erroneous data to the memory. The host shall ignore the data in the memory locations for commands that complete with such error conditions.

If a write error occurs during the processing of a command, (e.g., an internal error, End-to-end Guard Check Error, End-to-end Application Tag Check Error), the controller may either stop or complete the DMA transfer. If the write size is less than or equal to the Atomic Write Unit Power Fail size, then subsequent reads for the associated logical blocks shall return data from the previous successful write operation. If the write size is larger than the Atomic Write Unit Power Fail size, then subsequent reads for the associated logical blocks may return data from the previous successful write operation or this failed write operation.

Based on the value of the Limited Retry bit, the controller may apply all available error recovery means to complete the command.

10.3 Memory Error Handling

For PCI Express implementations, memory errors such as target abort, master abort, and parity may cause the controller to stop processing the currently executing command. These are serious errors that cannot be recovered from without host software intervention.

A master/target abort error occurs when host software has provided, to the controller, the address of memory that does not exist. When this occurs, the controller aborts the command with a Data Transfer Error status code.

10.4 Internal Controller Error Handling

Errors such as a DRAM failure or power loss notification indicate that a controller level failure has occurred during the processing of a command. The status code of the completion queue entry should indicate an Internal Error status code. Host software shall ignore any data transfer associated with the command. The host may choose to re-submit the command or indicate an error to the higher level software.

10.5 Controller Fatal Status Condition

If the controller has a serious error condition and is unable to communicate with host software via completion queue entries in the Admin Completion Queue or I/O Completion Queues, then the controller may set the Controller Fatal Status (CSTS.CFS) bit to ‘1’ (refer to section 3.1.6). This indicates to host software that a serious error condition has occurred. When this condition occurs, host software should attempt to reset and then re-initialize the controller.

The Controller Fatal Status condition is not indicated with an interrupt. If host software experiences timeout conditions and/or repeated errors, then host software should consult the Controller Fatal Status (CSTS.CFS) bit to determine if a more serious error has occurred.

If the Controller Fatal Status (CSTS.CFS) bit is set to ‘1’ on any controller in the NVM subsystem, the host should issue a Controller Reset to that controller.

If that Controller Reset does not clear the Controller Fatal Status condition, the host should initiate an NVM Subsystem Reset (refer to section 7.3.1), if supported.

Performing an NVM Subsystem Reset (NSSR) may cause PCI Express links to go down as part of resetting the NVM subsystem. Host software may have undesirable effects related to PCI Express links going down (e.g., some host operating systems or hypervisors may crash).

NVM Subsystem Reset should not be used if the host software has undesirable effects related to PCI Express links going down. This host software includes, but is not limited to, operating systems using Firmware First Error Handling (refer to the ACPI specification). Such operating systems should not use NSSR for recovery from CFS conditions.

Annex A. Sanitize Operation Considerations (Informative)

A.1 Overview

The Sanitize command initiates a sanitize operation that makes all user data previously written to the device inaccessible. To do this a Sanitize command is provided over the device's physical interface that cause the controller to process the requested operation. The actual result of the operation is very difficult to prove as complete. This annex provides some context and considerations for understanding the result of the operation and the practical limitations for auditing the result of the sanitize operation.

A.2 Hidden Storage (Overprovisioning)

Sanitize operations affect all physical storage that is able to hold user data. Many NVMe SSDs contain more physical storage than is addressable through the interface (overprovisioning), which is used for vendor specific purposes that may include providing increasing endurance, improving performance, and providing extra blocks to allow retiring bad or worn-out storage without affecting capacity. This excess capacity as well as any retired storage are not accessible through the interface. Vendor specific innovative use of this extra capacity supports advantages to the end user, but the lack of observability makes it difficult to ensure that all storage within the device has been affected. Only the accessible storage is able to be audited for the results of a sanitization operation.

A.3 Integrity checks and No-Deallocate After Sanitize

Another issue is availability of the data returned through the interface. Some of the sanitize operations (e.g., Block Erase) affect the physical devices in such a way that directly reading the accessible storage may trigger internal integrity checks resulting in error responses instead of returning the contents of the storage. Other sanitize operations (e.g., Crypto Erase) may scramble the internal vendor specific internal format of the data also resulting in error responses instead of returning the contents of the storage.

Some devices compensate for these issues by performing an additional internal write operation on all storage that is able to be allocated for user data. However, this has the side effect of potentially significant additional wear on the device as well as the side effect of obscuring the results of the initial sanitize operation (i.e., the writes forensically destroy the ability to audit the result of the initial sanitize operation). Given this side effect, process audits of sanitize behavior only prove effective results when the No-Deallocate After Sanitize bit is set the same way (e.g., set to '1') for both process audits and the individual device audits.

The Sanitize command introduced in NVM Express Revision 1.3 included a mechanism to specify that sanitized addressable storage not be deallocated, thereby allowing observations of the results of the sanitization operation. However, some architectures and products (e.g., integrity checking circuitry) interact with this capability in such a way as to defeat the sanitize result observability purpose. New features were added to NVM Express Revision 1.4 that include extended information about the sanitization capabilities of devices, a new asynchronous event, and configuration of the response to No-Deallocate After Sanitize requests. These features are intended to both support new systems that understand the new capabilities, as well to help manage legacy systems that do not understand the new capabilities without losing the ability to sanitize as requested.

A.4 Bad Block and Vendor Specific NAND Use

Another audit capability that is not supported by NVM Express is checking that any blocks that could not be sanitized (e.g., bad physical blocks) have been removed from the pool of storage that are able to be used as addressable storage.

An approach that is performed under some circumstances is removing the storage components from the NVM Express device after a sanitize operation and reading the contents in laboratory conditions. However this approach also has multiple difficulties. When physical storage devices are removed from a NVM Express device, much context is lost. This includes:

a) any encoding for zero's/one's balance;

b) identification of which components contain device firmware or other non-data information; and
c) which blocks have been retired and cannot be sanitized.